900 MHz ISM Band Analog RF Front End

Data Sheet

ADF9010

FEATURES

- 840 MHz to 960 MHz ISM bands
- Rx baseband analog low-pass filtering and PGA
- Integrated RF Tx upconverter
- Integrated integer-N PLL and VCO
- Integrated Tx PA preamplifier
- Differential fully balanced architectures
- 3.3 V supply
- Low power mode: <1 mA power-down current
- Programmable Rx LPF cutoff
  - 330 kHz, 880 kHz, 1.76 MHz, and bypass
- Rx PGA gain settings: 3 dB to 24 dB in 3 dB steps
- Low noise BiCMOS technology
- 48-lead, 7 mm × 7 mm LFCSP

APPLICATIONS

- 900 MHz RFID readers
- Unlicensed band 900 MHz applications

FUNCTIONAL BLOCK DIAGRAM

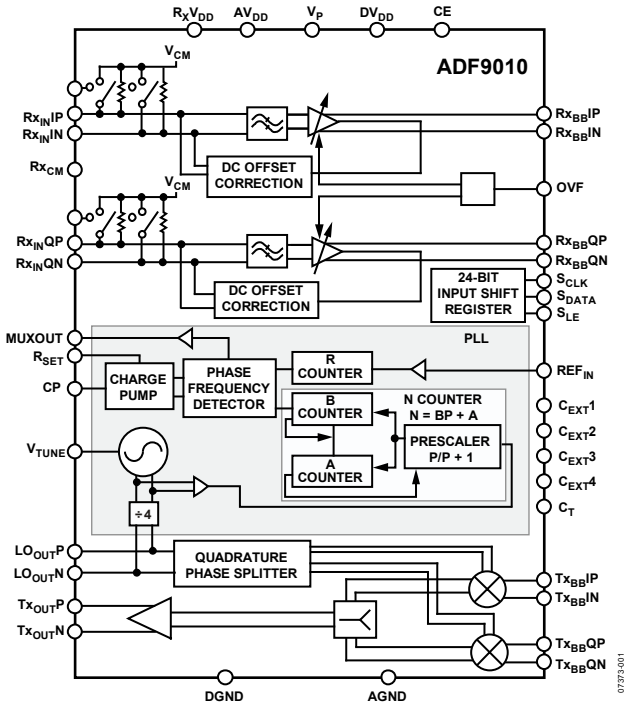

Figure 1.

GENERAL DESCRIPTION

The ADF9010 is a fully integrated RF Tx modulator and Rx analog baseband front end that operates in the frequency range from 840 MHz to 960 MHz. The receive path consists of a fully differential I/Q baseband PGA, low-pass filter, and general signal conditioning before connecting to an Rx ADC for baseband conversion. The Rx LPF gain ranges from 3 dB to 24 dB, programmable in 3 dB steps. The Rx LPF features four programmable modes with cutoff frequencies of 330 kHz, 880 kHz, and 1.76 MHz, or the filter can be bypassed if necessary.

The transmit path consists of a fully integrated differential Tx direct I/Q upconverter with a high linearity PA driver amplifier. It converts a baseband I/Q signal to an RF carrier-based signal between 840 MHz and 960 MHz. The highly linear transmit signal path ensures low output distortion.

Complete local oscillator (LO) signal generation is integrated on chip, including the integer-N synthesizer and VCO, which generate the required I and Q signals for transmit I/Q upconversion. The LO signal is also available at the output to drive an external RF demodulator. Control of all the on-chip registers is via a simple 3-wire serial interface. The device operates with a power supply ranging from 3.15 V to 3.45 V and can be powered down when not in use.

Rev. A
Document Feedback

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REVISION HISTORY

12/2017—Rev. 0 to Rev. A

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Updated Outline Dimensions ... 25
Changes to Ordering Guide ... 25

8/2008—Revision 0: Initial Version

SPECIFICATIONS

TRANSMIT CHARACTERISTICS

AV_{DD} = DV_{DD} = 3.3 V ± 5%, AGND = DGND = GND = 0 V, T_A = 25°C, dBm refers to 50 Ω, 1.4 V p-p differential sine waves in quadrature on a 500 mV dc bias, baseband frequency = 1 MHz, unless otherwise noted.

Table 1.

	B Version[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
TRANSMIT MODULATOR CHARACTERISTICS					
Operating Frequency Range	840		960	MHz	Range over which uncompensated sideband suppression < −30 dBc
Output Power		3		dBm	V_{IQ} = 1.4 V p-p differential
Output P1 dB		10		dBm	
Carrier Feedthrough		−40		dBm	
Sideband Suppression		−46		dBc	
Output IP3		24		dBm	P_{OUT} = −4 dBm per tone, 10 MHz and 12 MHz baseband input frequencies used.
Noise Floor		−158		dBm/Hz	
TRANSMIT BASEBAND CHARACTERISTICS					
Input Impedance of Each Pin		4		kΩ typ	Single-ended frequencies up to 2 MHz
Input Capacitance of Each Pin		3		pF	At 10 MHz
Input Signal Level		1.4		V p-p	Measured differentially at I or Q
Common-Mode Output Level		0.6		V	
Tx Baseband 3 dB Bandwidth		20		MHz	
POWER SUPPLIES					
Voltage Supply	3.15		3.45	V	
I_{DD}					
Digital I_{DD}		5	6	mA	
Rx Baseband		70	80	mA	Maximum gain settings
Tx Modulator		140		mA	Full power, baseband inputs biased at 0.5 V
LO Synthesizer and VCO		140		mA	+ 5 dBm LO power setting selected
Total I_{DD}		360	410	mA	
Power-Down					
Rx V_{DD}			1	mA	
AV_{DD}		1	20	µA	
DV_{DD}		1	20	µA	
LOGIC INPUTS (SERIAL INTERFACE)					
Input High Voltage, V_{INH}	1.4			V	1.8 V logic compatible
Input Low Voltage, V_{INL}			0.4	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}			5	pF	
LOGIC OUTPUTS (MUXOUT)					
Output High Voltage, V_{OH}	DV_{DD} − 0.4			V	I_{OL} = 500 µA
Output Low Voltage, V_{OL}			0.4	V	I_{OH} = 500 µA

[1] Operating temperature range for the B version is −40°C to +85°C.

RECEIVE BASEBAND CHARACTERISTICS

AV_{DD} = DV_{DD} = 3.3 V ± 5%, AGND = DGND = GND = 0 V, T_A = 25°C, dBm refers to 50 Ω, 1.4 V p-p differential sine waves in quadrature on a 500 mV dc bias, baseband frequency = 1 MHz, unless otherwise noted.

Table 2.

	B Version[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
RECEIVE BASEBAND PGA					
Highest Voltage Gain		24		dB	
Lowest Voltage Gain		3		dB	
Gain Control Range		18		dB	Programmable using 3-bit interface
Gain Control Step		3		dB	
Noise Spectral Density (Referred to Input)		3.5		nV/√Hz	At maximum PGA gain
RECEIVE BASEBAND FILTERS					
3 dB Cutoff Frequency (Mode 0)		320		kHz	After filter calibration
Gain Flatness			0.5	dB	Typical from dc to 90 kHz
Differential Group Delay		500		µs	DC to 360 kHz
			150	µs	170 kHz to 310 kHz
Attenuation Template					After filter calibration
At 330 kHz Offset		−3		dB	
At 500 kHz Offset		−8		dB	
At 1 MHz Offset		−28		dB	
3 dB Cutoff Frequency (Mode 1)		880		kHz	After filter calibration
Gain Flatness			0.5	dB	DC to 90 kHz
Differential Group Delay		500		µs	DC to 360 kHz
			150	µs	170 kHz to 310 kHz
Attenuation Template					After filter calibration
At 880 kHz Offset		−3		dB	
At 2 MHz Offset		−17		dB	
At 4 MHz Offset		−38		dB	
3 dB Cutoff Frequency (Mode 2)		1.76		MHz	After filter calibration
Gain Flatness			0.5	dB	DC to 90 kHz
Differential Group Delay		500		µs	DC to 360 kHz
			150	µs	170 kHz to 310 kHz
Attenuation Template					After filter calibration
At 1.76 MHz Offset		−3		dB	
At 4 MHz Offset		−18		dB	
At 8 MHz Offset		−38		dB	
At 16 MHz Offset		−60		dB	
3 dB Cutoff Frequency (Mode 3)		4		MHz	After filter calibration
Gain Flatness			0.5	dB	DC to 90 kHz
Differential Group Delay		500		µs	DC to 360 kHz
At 2 MHz Offset		−0.5		dB	
At 4 MHz Offset		−2		dB	
Input Impedance of Each Pin					
At 24 dB gain		250		Ω	
At 3 dB gain		4		kΩ	
Input Capacitance of Each Pin		3		pF	At 10 MHz
Input Signal Level			2	V p-p	Measured differentially at I or Q
Common-Mode Output Level		1.65		V	On Rx baseband outputs
Maximum Residual DC		150		mV	Baseband gain 0 dB – 27 dB

[1] Operating temperature range for the B version is −40°C to +85°C.

INTEGER-N PLL AND VCO CHARACTERISTICS

Table 3.

Parameter	B Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
VCO OPERATING FREQUENCY	3360		3840	MHz	
LO OUTPUT CHARACTERISTICS					Measured at LO output (900 MHz)
VCO Control Voltage Sensitivity		8		MHz/V	3.6 GHz VCO frequency (taking into account divide by 4)
Harmonic Content (Second)		−27		dBc	
Harmonic Content (Third)		−14		dBc	
Frequency Pushing (Open Loop)		1.2		MHz/V	
Frequency Pulling (Open Loop)		10		Hz	Into 2.00 VSWR load.
Lock Time		1000		µs	10 kHz loop bandwidth
Output Power		−4 to +5		dBm	LO outputs combined in a 1:1 transformer; programmable in 3 dB steps
Output Power Variation		±3		dB	
NOISE CHARACTERISTICS					Measured at LO output (900 MHz)
VCO Phase Noise Performance[2]					
At 100 kHz Offset		−120		dBc/Hz	
At 1 MHz Offset		−141		dBc/Hz	
At 10 MHz Offset		−154		dBc/Hz	
In-Band Phase Noise[3, 4]		−96		dBc/Hz	at 1 kHz offset from carrier
Normalized In-Band Phase Noise Floor[3, 4]		−220		dBc/Hz	
Spurious Frequencies at Output Channel Spacing		−70		dBc	900 MHz offset, 1 MHz PFD frequency, 250 kHz channel spacing; loop bandwidth = 7.5 kHz
PHASE DETECTOR					
Phase Detector Frequency[5]			8	MHz	
Maximum Allowable Prescaler Output Frequency[6]			325	MHz	
CHARGE PUMP					
I_{CP} Sink/Source					With R_{SET} = 4.7 kΩ
High Value		5		mA	
Low Value		0.625		mA	
R_{SET} Range	2.7		10	kΩ	
I_{CP} Three-State Leakage Current		0.2		nA	
Sink and Source Current Matching		2		%	1.25 V ≤ V_{CP} ≤ 2.5 V
I_{CP} vs. V_{CP}		1.5		%	1.25 V ≤ V_{CP} ≤ 2.5 V
I_{CP} vs. Temperature		2		%	V_{CP} = 2.0 V
PLL REFERENCE					
Reference Clock Frequency	10		104	MHz	
Reference Clock Sensitivity	0.7		PLL V_{DD}	V p-p	
Reference Input Capacitance		5		pF	
REF_{IN} Input Current			±100	µA	

[1] Operating temperature range for the B version is −40°C to +85°C.
[2] The noise of the VCO is measured in open-loop conditions.
[3] The phase noise is measured with the EVAL-ADF9010EBZ1 evaluation board and the Agilent E5052A spectrum analyzer. The spectrum analyzer provides the REF_{IN} for the synthesizer; offset frequency = 1 kHz.
[4] f_{REFIN} = 10 MHz; f_{PFD} = 1000 kHz; N = 3600; loop BW = 25 kHz.
[5] Guaranteed by design. Sample tested to ensure compliance.
[6] This is the maximum operating frequency of the CMOS counters. The prescaler value must be chosen to ensure that the RF input is divided down to a frequency that is less than this value.

WRITE TIMING CHARACTERISTICS

AV_{DD} = DV_{DD} = 3.3 V ± 5%; AGND = DGND = GND = 0 V; T_A = 25°C, guaranteed by design, but not production tested.

Table 4.

Parameter	Limit at t_{MIN} to t_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	10	ns min	S_{DATA} to S_{CLK} setup time
t_2	10	ns min	S_{DATA} to S_{CLK} hold time
t_3	25	ns min	S_{CLK} high duration
t_4	25	ns min	S_{CLK} low duration
t_5	10	ns min	S_{CLK} to S_{LE} setup time
t_6	20	ns min	S_{LE} pulse width

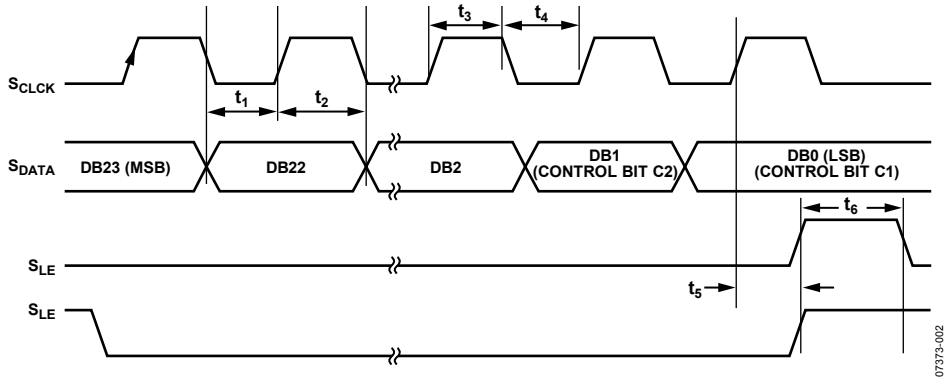


Figure 2. Write Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

Table 5.

Parameter	Rating
DV_{DD}, RxV_{DD}, AV_{DD} to GND[1]	−0.3 V to +3.9 V
RxV_{DD}, AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_P to GND[1]	−0.3 V to +5.5 V
Digital I/O Voltage to GND[1]	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND[1]	−0.3 V to AV_{DD} + 0.3 V
Charge Pump Voltage to GND[1]	−0.3 V to V_P to GND[1]
REF_{IN}, $LO_{EXT}P$, $LO_{EXT}N$ to GND[1]	−0.3 V to V_{DD} + 0.3 V
$LO_{EXT}P$ to $LO_{EXT}N$	±320 mV
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
LCSP θ_{JA} Thermal Impedance	26°C/W
Reflow Soldering	
Peak Temperature	260°C/W
Time at Peak Temperature	40 sec

[1] GND = AGND = DGND = 0 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

This device is a high-performance RF integrated circuit with an ESD rating of <0.5 kV and is ESD sensitive. Proper precautions must be taken for handling and assembly.

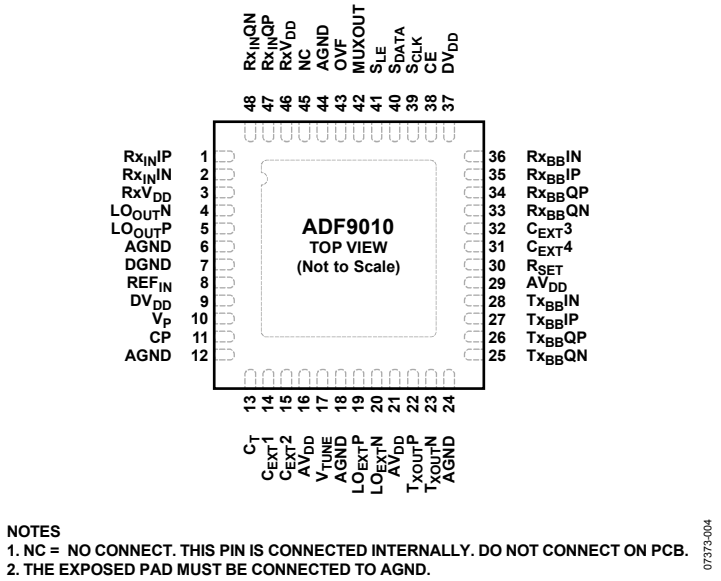
TRANSISTOR COUNT

The ADF9010 transistor count is 40,454 (CMOS) and 994 (bipolar).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. THIS PIN IS CONNECTED INTERNALLY. DO NOT CONNECT ON PCB.
2. THE EXPOSED PAD MUST BE CONNECTED TO AGND.

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2	$Rx_{IN}IP$, $Rx_{IN}IN$	Input/Complementary In-Phase Input to the Receive Filter Stage.
3, 46	RxV_{DD}	Receiver Filter Power Supply. This voltage ranges from 3.15 V to 3.45 V. Decoupling capacitors to the analog ground plane must be placed as close as possible to this pin. RxV_{DD} must be the same value as AV_{DD} and DV_{DD}.
4, 5	$LO_{OUT}N$, $LO_{OUT}P$	Buffered Local Oscillator Output. These outputs are used to provide the LO for the external RF demodulator. These require an RF choke to AV_{DD} and a dc bypass capacitor before connection to a demodulator.
6, 12, 18, 24, 44	AGND	Analog Ground. This is the ground return path of analog circuitry.
7	DGND	Digital Ground.
8	REF_{IN}	PLL Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and a dc equivalent input resistance of 100 kΩ (see Figure 13). This input can be driven from a TTL or CMOS crystal oscillator, or it must be ac-coupled.
9, 37	DV_{DD}	Digital Power Supply. This voltage ranges from 3.15 V to 3.45 V. Decoupling capacitors to the digital ground plane must be placed as close as possible to this pin. DV_{DD} must be the same value as AV_{DD}.
10	V_P	This pin supplies the voltage to the charge pump. If the internal VCO is used, it must equal AV_{DD} and DV_{DD}. If an external VCO is used, the voltage can be $AV_{DD} < V_P < 5.5$ V.
11	CP	Charge Pump Output. When enabled, this pin provides $\pm I_{CP}$ to the external loop filter, which in turn drives the external VCO.
13	C_T	A capacitor connected to this pin is used to roll off noise from the VCO. It must be decoupled to AGND with a value of 10 nF. The output voltage on this part is proportional to temperature. At ambient temperature, the voltage is 2.0 V.
14	$C_{EXT}1$	A capacitor connected to this pin is used to roll off noise from the VCO. It must be decoupled to AGND with a value of 10 nF.
15	$C_{EXT}2$	A capacitor connected to this pin is used to roll off noise from the VCO. It must be decoupled to AGND with a value of 10 nF.
16, 21, 29	AV_{DD}	Analog Power Supply. This voltage ranges from 3.15 V to 3.45 V. Decoupling capacitors to the analog ground plane must be placed as close as possible to this pin. AV_{DD} must be the same value as DV_{DD}.

Pin No.	Mnemonic	Description
17	V_{TUNE}	Control Input to the VCO. This input determines the VCO frequency and is derived from filtering the CP output.
19, 20	$LO_{EXT}P$, $LO_{EXT}N$	Single-Ended External VCO Input of 50 Ω. This is used if the ADF9010 utilizes an optional external VCO. These pins are internally dc-biased and must be ac-coupled. AC-couple $LO_{EXT}N$ to ground with 100 pF and ac-couple the VCO signal with 100 pF through $LO_{EXT}P$.
22, 23	$Tx_{OUT}P$, $Tx_{OUT}N$	Buffered Tx Output. These pins contain the Tx output signal, which can be combined in a balun for best results.
25, 26	$Tx_{BB}QN$, $Tx_{BB}QP$	Baseband Quadrature Phase Input/Complementary Input to the Transmit Modulator.
27, 28	$Tx_{BB}IP$, $Tx_{BB}IN$	Baseband In-Phase Input/Complementary to the Transmit Modulator.
30	R_{SET}	Connecting a resistor between this pin and AGND sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.66 V. The relationship between I_{CP} and R_{SET} is $I_{CPMAX} = 25.5/R_{SET}$ where: R_{SET} is 5.1 kΩ. I_{CPMAX} is 5 mA.
31	$C_{EXT}4$	A capacitor connected to this pin is used to roll off noise from the VCO. It must be decoupled to AGND with a value of 10 nF.
32	$C_{EXT}3$	A capacitor connected to this pin is used to roll off noise from the VCO. It must be decoupled to AGND with a value of 10 nF.
33, 34	$Rx_{BB}QN$, $Rx_{BB}QP$	Output/Complementary Filtered Quadrature Signals from the Receive Filter Stage. The filtered output is passed to the baseband MxFE chip.
35, 36	$Rx_{BB}IP$, $Rx_{BB}IN$	Output/Complementary Filtered In-Phase from the Receive Filter Stage. The filtered output is passed to the baseband MxFE chip.
38	CE	Chip Enable. A Logic 0 on this pin powers down the device. A Logic 1 on this pin enables the device depending on the status of the power-down bits.
39	S_{CLK}	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the S_{CLK} rising edge. This is a high impedance CMOS input.
40	S_{DATA}	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This is a high impedance CMOS input.
41	S_{LE}	Load Enable, CMOS Input. When LE goes high, the data stored in the shift register is loaded into one of the four latches; the latch uses the control bits.
42	MUXOUT	This multiplexer output allows either the PLL lock detect, the scaled VCO frequency, or the scaled PLL reference frequency to be accessed externally.
43	OVF	A rising edge on this pin drops the gain of the Rx path by 6 dB. This is used to rapidly drop the gain if the ADC detects an overload.
45	NC	No Connect. This pin is connected internally. Do not connect on printed circuit board (PCB).
47, 48	$Rx_{IN}QP$, $Rx_{IN}QN$	Input/Complementary Quadrature Input to the Receive Filter Stage.
	EPAD	Exposed Pad. The exposed pad must be connected to AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

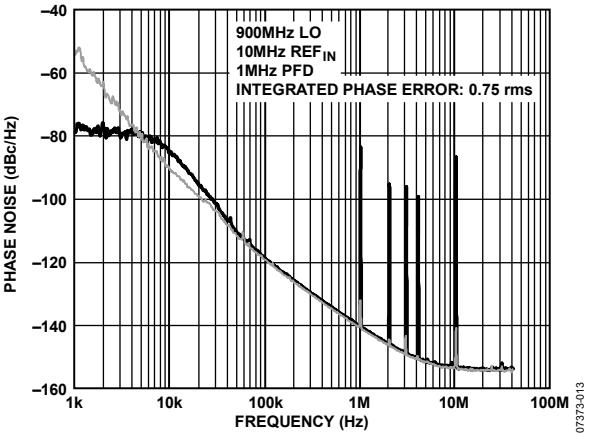


Figure 4. LO Phase Noise (900 MHz, Including Open-Loop VCO Noise)

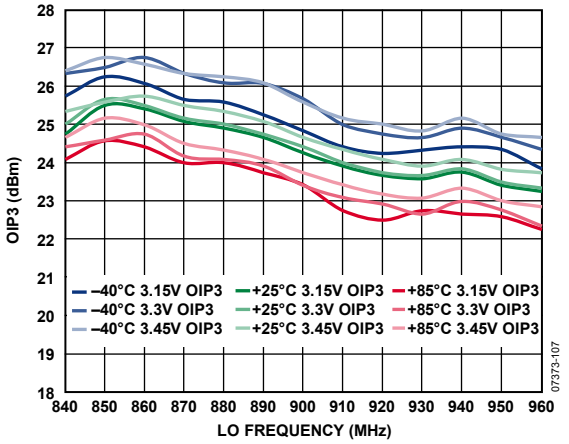


Figure 7. Output IP3 (dBm) vs. LO Frequency (Hz), with Supply and Temperature Variations; Two-Tone Test (10 MHz and 12 MHz Baseband Input Frequencies)

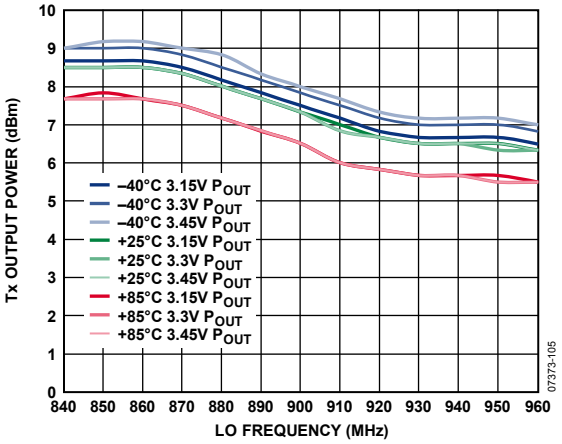


Figure 5. Single Sideband Tx Power Output (dBm) vs. LO frequency (Hz) with Supply and Temperature Variations; Outputs Combined in 50:100 Balun

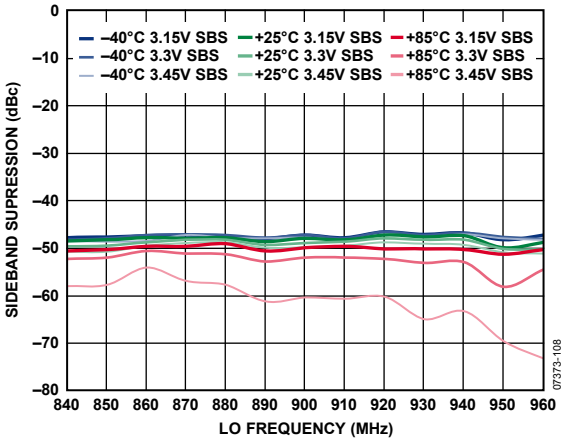


Figure 8. Unwanted Sideband Suppression (dBc) vs. LO Frequency (Hz) with Supply and Temperature Variations

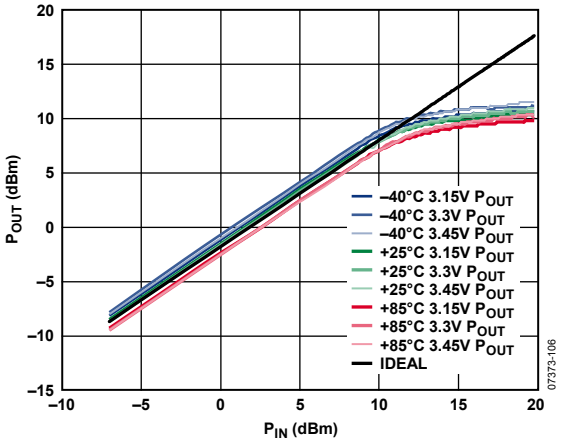


Figure 6. Power Output vs. Baseband Input Power with Supply and Temperature Variations

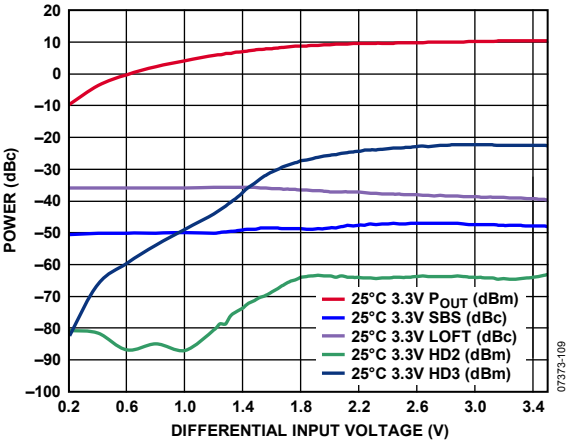


Figure 9. Second- and Third-Order Distortion, Sideband Suppression (dBc), Carrier Feedthrough (dBm) and SBS P_{OUT} vs. Baseband Differential Input Level; LO Frequency = 900 MHz

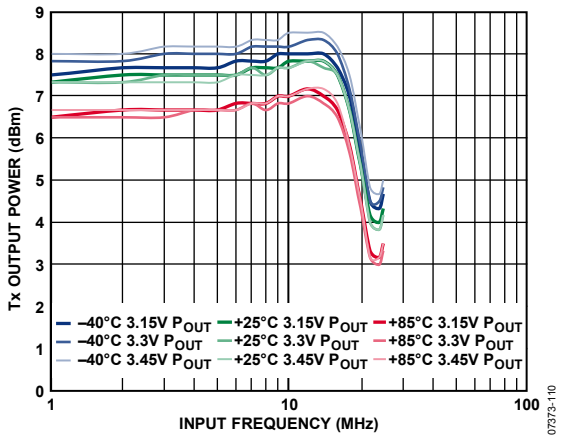


Figure 10. Single Sideband Power vs. Baseband Input Frequency, with Supply and Temperature Variations; Maximum Gain Setting Selected; LO Frequency = 900 MHz

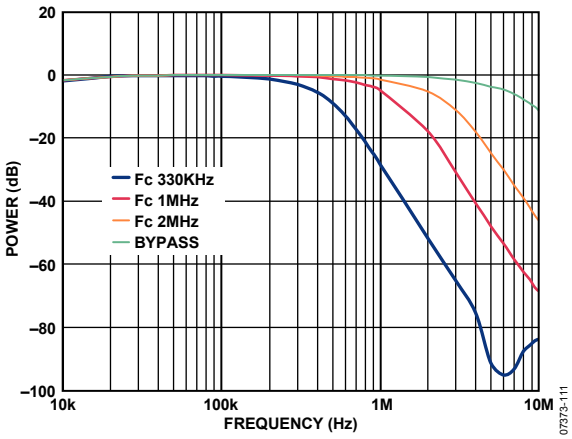


Figure 11. Rx Filter Performance, Power vs. Input Frequency

CIRCUIT DESCRIPTION

Rx SECTION

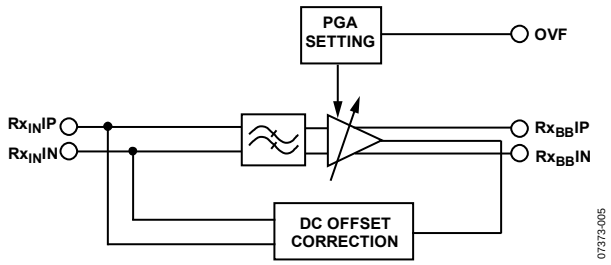


Figure 12. Rx Filter

The Rx section of the ADF9010 features programmable baseband low-pass filters. These are used to amplify the desired Rx signal from the demodulator while removing the unwanted portion to ensure no antialiasing occurs in the Rx ADC.

These filters have a programmable gain stage, allowing gain to be selected from 3 dB to 24 dB in steps of 3 dB. The bandwidth of these filters is also programmable, allowing 3 dB cutoff frequencies of 330 kHz, 880 kHz, and 1.76 MHz, along with a bypass mode. The filters utilize a fourth-order Bessel transfer function (see the Specifications section for more information). If desired, the filter stage can be bypassed.

Additionally, a rising edge on the OVF pin reduces the gain of the Rx amplifiers by 6 dB. This is to correct a potential overflow of the input to the ADC.

Updating the Rx calibration latch with the calibration bit enabled calibrates the filter to remove any dc offset. The 3 dB cutoff frequency (f_C) of the filters is calibrated also.

LO SECTION

LO Reference Input Section

The LO input stage is shown in Figure 13. SW1 and SW2 are normally closed switches; SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

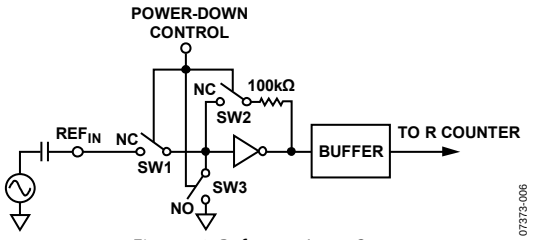


Figure 13. Reference Input Stage

R COUNTER

The 14-bit R counter allows the input clock frequency to be divided down to produce the input clock to the phase frequency detector (PFD). Division ratios from 1 to 8191 are allowed.

A AND B COUNTERS

The A and B CMOS counters combine with the dual modulus prescaler to allow a wide range of division ratios in the PLL feedback counter. The counters are specified to work when the prescaler output is 300 MHz or less.

Pulse Swallow Function

The A and B counters, in conjunction with the dual-modulus prescaler (see Figure 14), make it possible to generate large divider ratios. The equation for N is as follows:

$$N = BP + A$$

where:
N is the overall divider ratio of the signal from the external RF input.
P is the preset modulus of the dual-modulus prescaler.
B is the preset divide ratio of the binary 13-bit counter (3 to 8191).
A is the preset divide ratio of the binary 5-bit swallow counter (0 to 31).

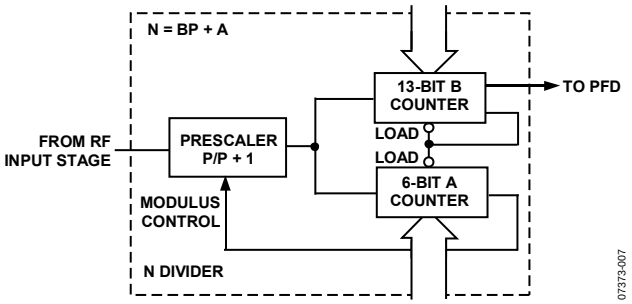


Figure 14. A and B Counters

Prescaler (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with the A and B counters, enables the large division ratio, N, to be realized (N = BP + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the A and B CMOS counters. The prescaler is programmable. The prescaler can be set in software to 8/9, 16/17, or 32/33. For the ADF9010, however, use the 16/17 and 32/33 settings. It is based on a synchronous 4/5 core. A minimum divide ratio is possible for fully contiguous output frequencies. This minimum is determined by P, the prescaler value, and is given by ($P^2 - P$).

PFD and Charge Pump

The phase frequency detector (PFD) takes inputs from the R counter and N counter ($N = BP + A$) and produces an output proportional to the phase and frequency difference between them (see Figure 15).

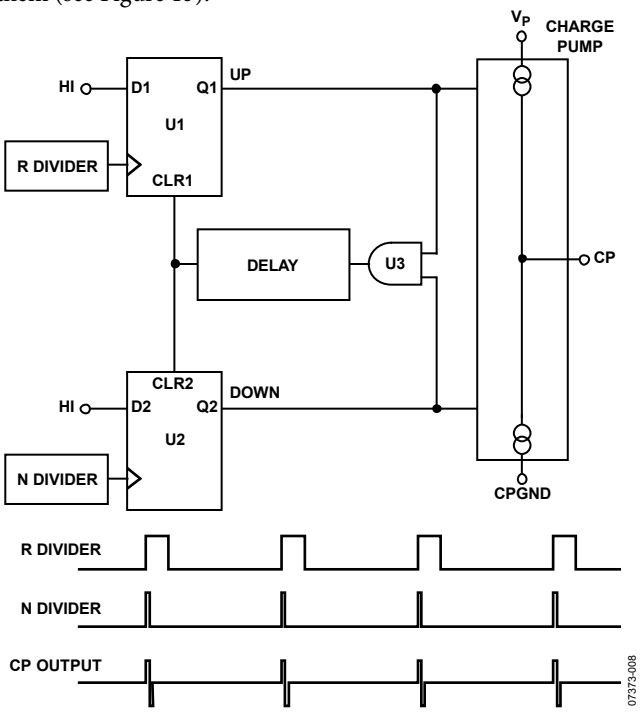


Figure 15. PFD Simplified Schematic and Timing (In Lock)

MUXOUT

The output multiplexer on the ADF9010 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the control latch. The full truth table is shown in Figure 22. Figure 16 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed for two types of lock detect: digital and analog. Digital lock detect is active high. If the LDP in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector cycles is less than 15 ns.

With the LDP set to 1, five consecutive cycles of less than 15 ns phase error are required to set the lock detect. It stays set high until a phase error of greater than 25 ns is detected on any subsequent PD cycle.

Operate the N-channel open-drain analog lock detect with an external pull-up resistor of 10 kΩ nominal. When a lock has been detected, this output is high with narrow low-going pulses.

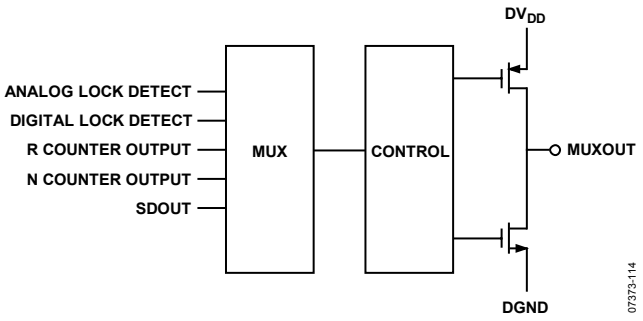


Figure 16. MUXOUT Circuit

Voltage-Controlled Oscillator (VCO)

The VCO core in the ADF9010 uses 16 overlapping bands, as shown in Figure 17, to allow a wide frequency range to be covered with a low VCO sensitivity (K_V) and to result in good phase noise and spurious performance. The VCO operates at 4× the LO frequency, providing an output range of 840 MHz to 960 MHz.

The correct band is chosen automatically by the band select logic at power-up or whenever the LO latch is updated. During band select, which takes five PFD cycles, the VCO V_{TUNE} is disconnected from the output of the loop filter and connected to an internal reference voltage.

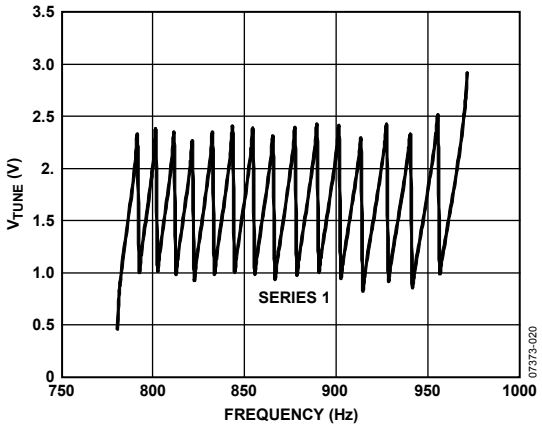


Figure 17. VCO Bands

The R counter output is used as the clock for the band select logic and must not exceed 1 MHz. A programmable divider is provided at the R counter input to allow division by 1, 2, 4, or 8 and is controlled by Bit BSC1 and Bit BSC2 in the Tx latch. Where the required PFD frequency exceeds 1 MHz, set the divide ratio to allow enough time to select the correct band.

After the band is selected, normal PLL action resumes. The nominal value of K_V is 32 MHz/V or 8 MHz/V, taking into account the divide by 4.

The output from the VCO is divided by 4 for the LO inputs to the mixers, and for the LO output drive to the demodulator.

LO Output

The $LO_{OUT}P$ and $LO_{OUT}N$ pins are connected to the collectors of an NPN differential pair driven by buffered outputs from the VCO, as shown in Figure 18. To allow optimal power dissipation vs. the output power requirements, the tail current of the differential pair is programmable via Bit TP1 and Bit TP2 in the control latch. The four current levels that can be set are 6 mA, 8.5 mA, 11.5 mA, and 17.5 mA. These levels give output power levels of −4 dBm, −1 dBm, +2 dBm, and +5 dBm, respectively, if both outputs are combined in a 1 + 1:1 transformer or a 180° microstrip coupler.

If the outputs are used individually, the optimum output stage consists of a shunt inductor to V_{DD}.

Another feature of the ADF9010 is that the supply current to the RF output stage is shut down until the part achieves lock as measured by the digital lock detect circuitry. This is enabled by the mute Tx until lock detect (F4) bit in the control latch.

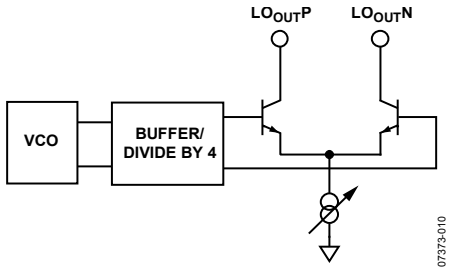


Figure 18. LO Output Section

Tx SECTION

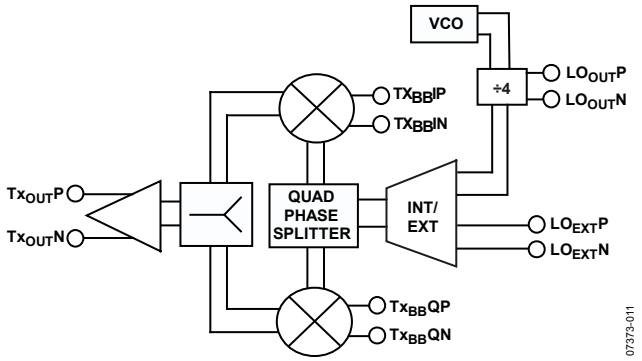


Figure 19. Tx Section

Tx Baseband Inputs

Differential in-phase (I) and quadrature baseband (Q) inputs are high impedance inputs that must be dc-biased to approximately 500 mV dc and e driven from a low impedance source. Nominal characterized ac signal swing is 700 mV p-p on each pin. This results in a differential drive of 1.4 V p-p with a 500 mV dc bias.

Mixers

The ADF9010 has two double-balanced mixers, one for the in-phase channel (I channel) and one for the quadrature channel (Q channel). Both mixers are based on the Gilbert cell design of four cross-connected transistors.

Tx Output

The $Tx_{OUT}P$ and $Tx_{OUT}N$ pins of the ADF9010 are connected to the collectors of four NPN differential pairs driven by the baseband signals, as shown in Figure 20. To allow the user optimal power dissipation vs. the output power requirements, the tail current of the differential pair is programmable via Bit TP1 and Bit TP2 in the control latch. Two levels can be set; these levels give output power levels of −3 dBm and, +3 dBm, respectively, using a 50 Ω resistor to V_{DD} and ac coupling into a 50 Ω load. Alternatively, both outputs can be combined in a 1 + 1:1 transformer or a 180° microstrip coupler. This buffer can be powered off if desired.

Another feature of the ADF9010 is that the supply current to the Tx output stage is shut down until the part achieves lock as measured by the digital lock detect circuitry. This is enabled by the mute LO until lock detect bit (F5) in the control latch.

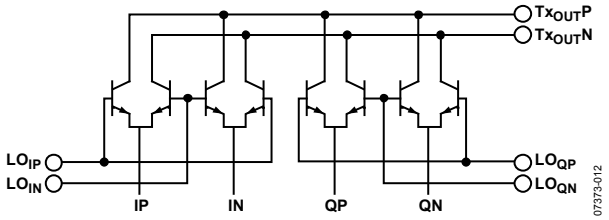


Figure 20. Tx Section

INTERFACING

Input Shift Register

The digital section of the ADF9010 includes a 24-bit input shift register. Data is clocked into the 24-bit shift register on each rising edge of S_{CLK}. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of S_{LE}. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in Figure 21.

The truth table for Bit C3, Bit C2, and Bit C1 is shown in Table 7. It displays a summary of how the latches are programmed. Note that some bits are used for factory testing and must not be programmed by the user.

Table 7. Truth Table

Control Bits			
C3	**C2**	**C1**	**Data Latch**
X	0	0	Control latch
0	0	1	Tx latch
1	0	1	Rx calibration
X	1	0	LO latch
X	1	1	Rx filter

LATCH STRUCTURE

Figure 21 shows the three on-chip latches for the ADF9010. The two LSBs determine which latch is programmed.

CONTROL LATCH

RESERVED	PD Rx	PD PLL	PD VCO	PD Tx	Tx OUTPUT POWER		CHARGE PUMP CURRENT			LO OUTPUT POWER		MUTE LO UNTIL LD	MUTE Tx UNTIL LD	CP THREE-STATE	PD POLARITY	MUXOUT			COUNTER RESET	RESERVED		CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RES	PD4	PD3	PD2	PD1	TP2	TP1	CPI3	CPI2	CPI1	P2	P1	F5	F4	F3	F2	M3	M2	M1	F1	RES	RES	C2 (0)	C1 (0)

Tx LATCH

LO PHASE SELECT			Tx MOD LO PHASE SELECT			BAND SELECT CLOCK		13-BIT REFERENCE COUNTER													CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P3	P2	P1	T3	T2	T1	BSC2	BSC1	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C3 (0)	C2 (0)	C1 (1)

Rx CALIBRATION

LO PHASE SELECT			Tx MOD LO PHASE SELECT			BAND SELECT CLOCK		Rx FILTER CAL	Rx CALIBRATION DIVIDER						HIGH-PASS FILTER BOOST TIMEOUT COUNTER						CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P3	P2	P1	T3	T2	T1	BSC2	BSC1	R13	RC6	RC5	RC4	RC3	RC2	RC1	HP6	HP5	HP4	HP3	HP2	HP1	C3 (1)	C2 (0)	C1 (1)

LO LATCH

PRESCALER		CP GAIN	N DIV MUX	13-BIT B COUNTER													5-BIT A COUNTER					CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	G1	M1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A5	A4	A3	A2	A1	C2 (1)	C2 (0)

Rx LATCH

TEST MODES																HPF BOOST	Rx FILTER BANDWIDTH		Rx FILTER GAIN STEPS			CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
T16	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	HP	BW2	BW1	G3	G2	G1	C2 (1)	C1 (1)

07373-014

Figure 21. Latch Summary

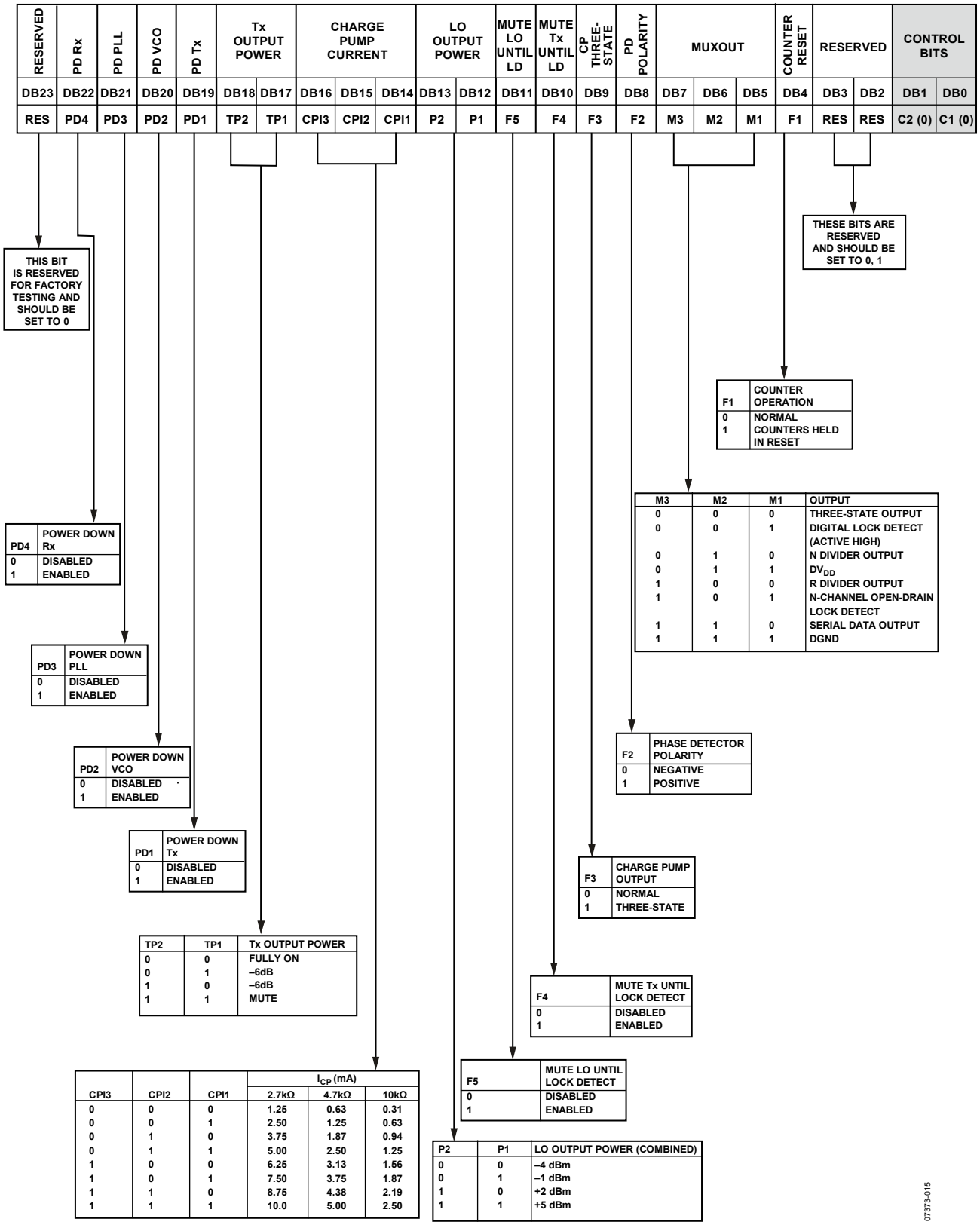


Figure 22. Control Latch

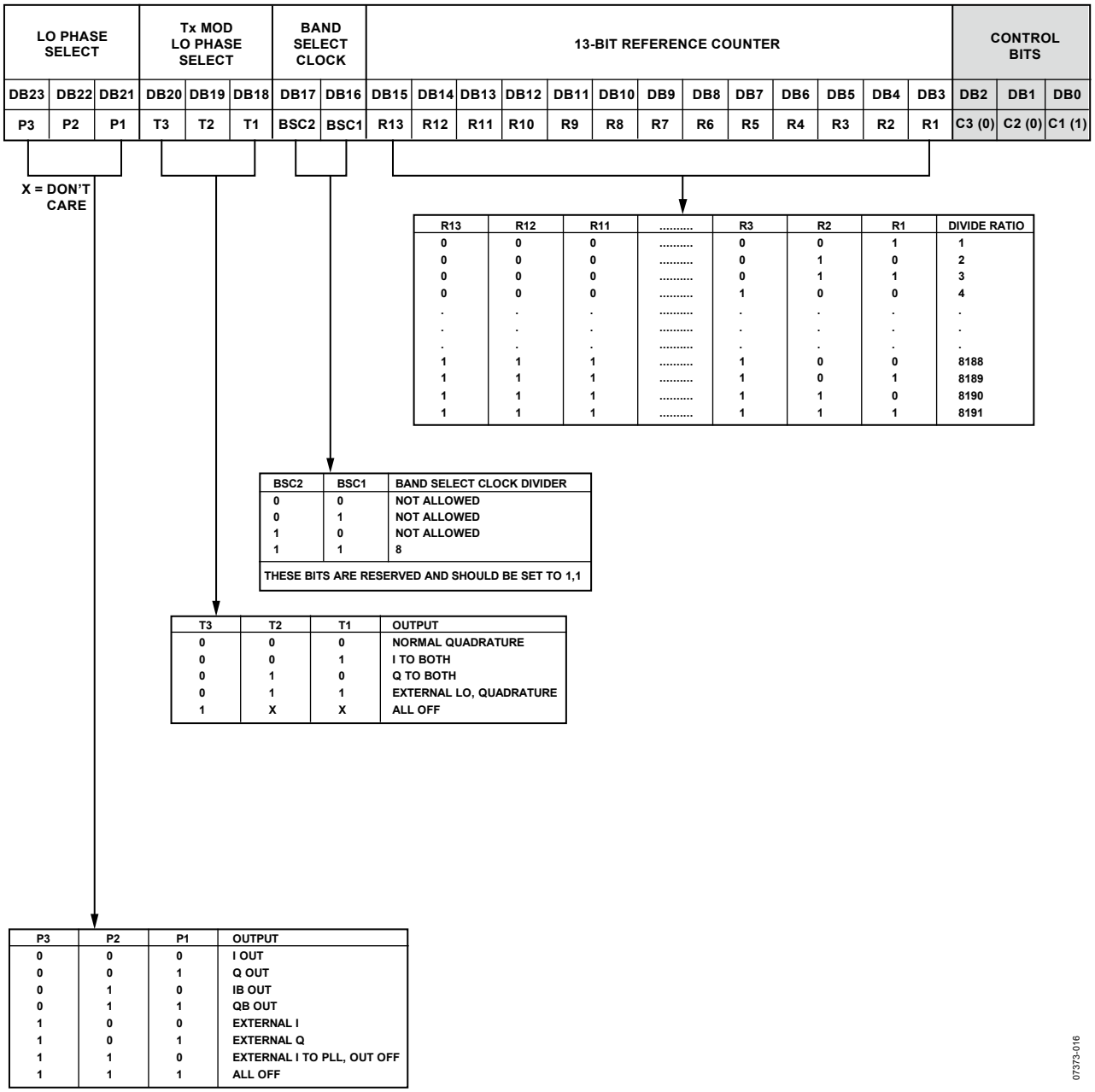


Figure 23. Tx Latch

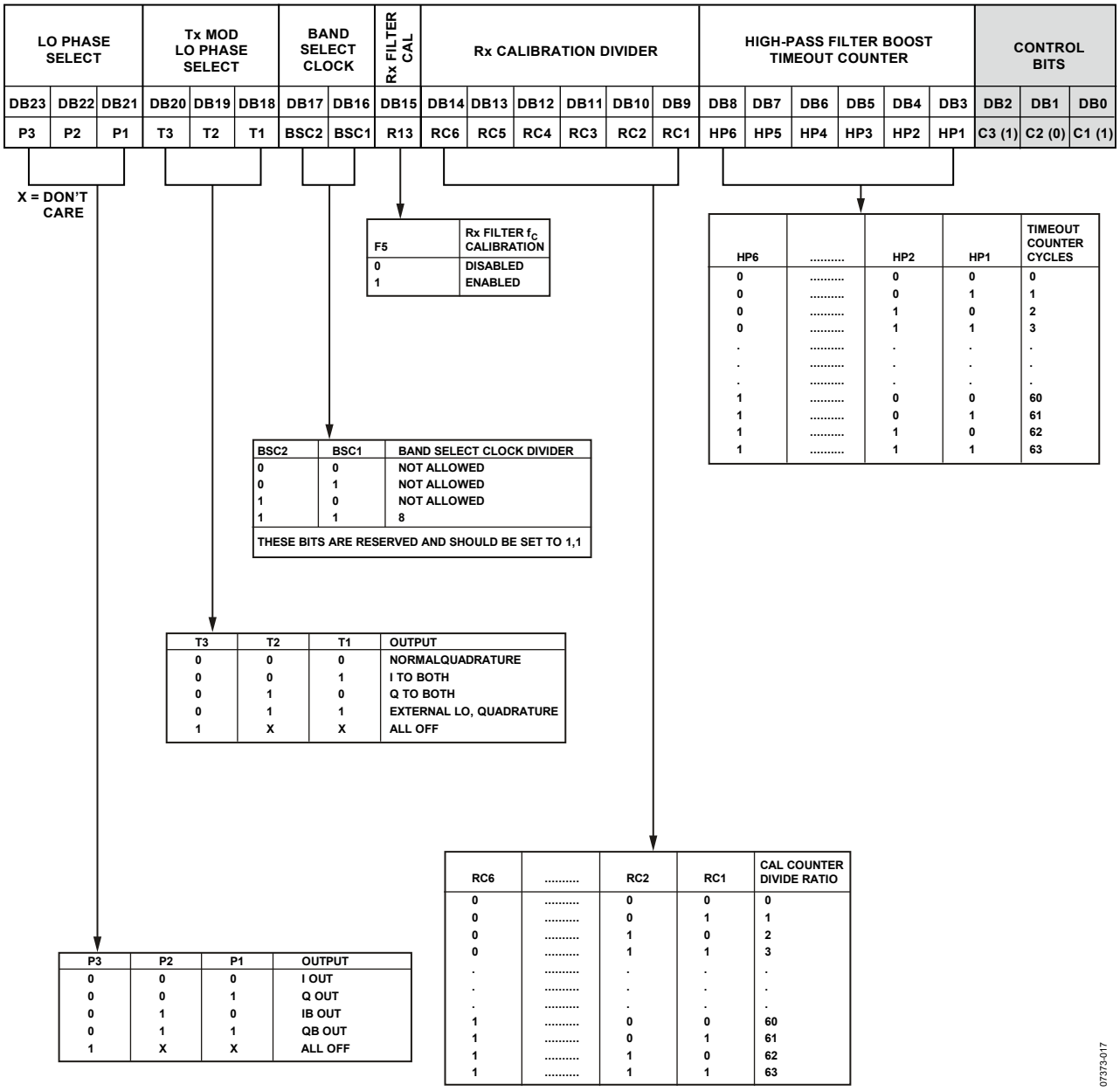


Figure 24. Rx Calibration Latch

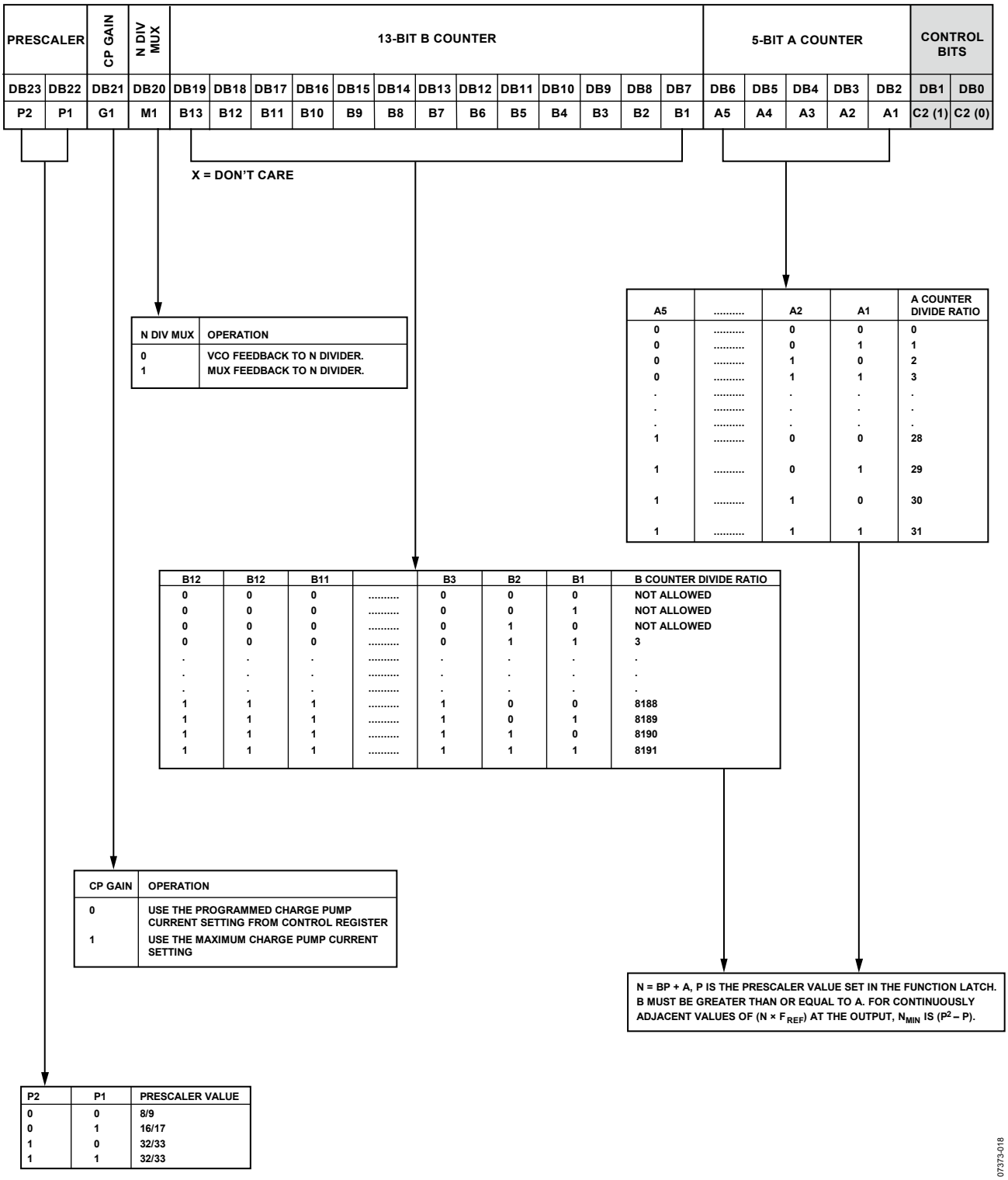


Figure 25. LO Latch

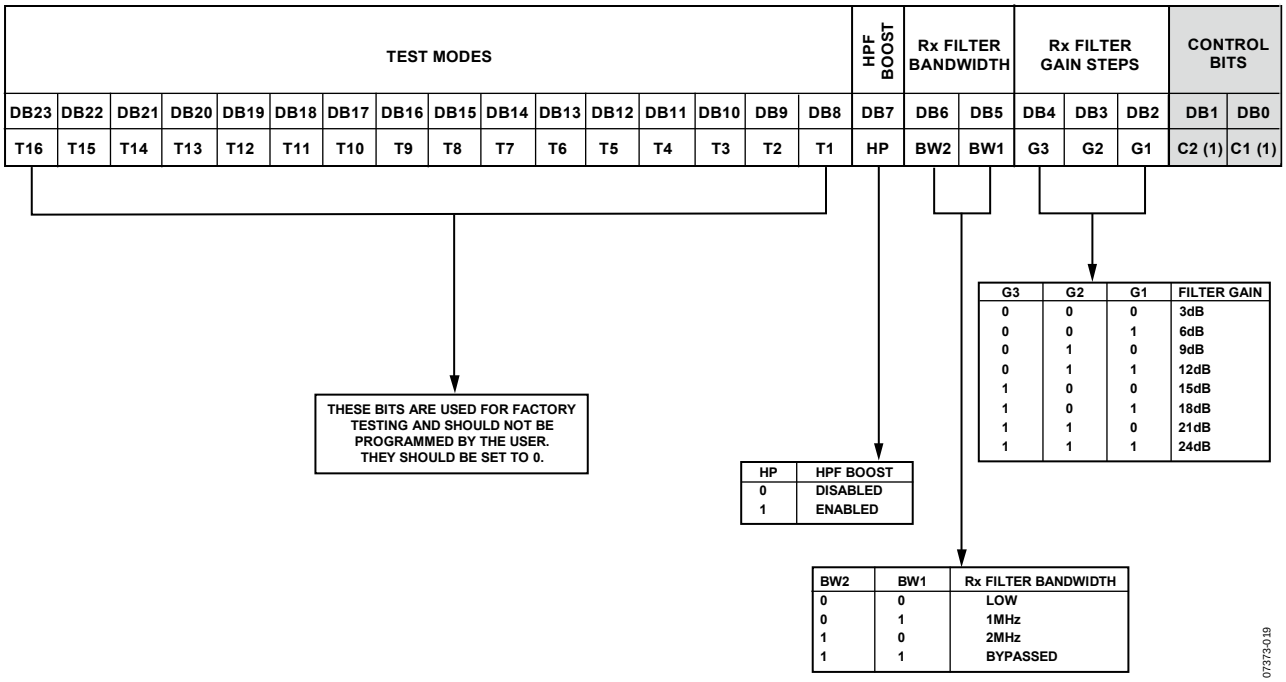


Figure 26. Rx Latch

CONTROL LATCH

With (C2, C1) = (0, 0), the control latch is programmed. Figure 22 shows the input data format for programming the control latch.

Power-Down

Programming a 1 to PD4, PD3, PD2, or PD1 powers down the circuitry for the Rx filters, PLL, VCO, and Tx sections, respectively. Programming a 0 enables normal operation for each section.

Tx Output Power

Bit TP1 and Bit TP2 set the output power level of the VCO. See the truth table in Figure 22.

Charge Pump Current

Bit CPI3, Bit CPI2, and Bit CPI1 determine Current Setting 2. See the truth table in Figure 22.

LO Output Power

Bit P1 and Bit P2 set the output power level of the LO. See the truth table in Figure 22.

Mute LO Until Lock Detect

Bit F5 is the mute until lock detect bit. This function, when enabled, ensures that the LO outputs are not switched on until the PLL is locked.

Mute Tx Until Lock Detect

Bit F4 is the mute Tx until lock detect bit. This function, when enabled, ensures that the Tx outputs are not switched on until the PLL is locked.

Charge Pump Three-State

Bit F3 puts the charge pump into three-state mode when programmed to a 1. Set this bit to 0 for normal operation.

Phase Detector Polarity

Bit F2 sets the phase detector polarity. The positive setting enabled by programming a 1 is used when using the on-chip VCO with a passive loop filter or with an active noninverting filter. It can also be set to 0. This is required if an active inverting loop filter is used.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, and M1. See the truth table in Figure 22.

Counter Reset

Bit F1 is the counter reset bit for the PLL of the ADF9010. When this bit is set to 1, the R, A, and B counters are held in reset. For normal operation, set this bit to 0.

Reserved Bits

DB3 and DB2 are spare bits that are reserved. Program these bits to 0 and 1, respectively.

Tx LATCH

With (C3, C2, C1) = (0, 0, 1), the Tx latch is programmed. Figure 23 shows the input data format for programming the Tx latch.

LO Phase Select

Bit P3, Bit P2, and Bit P1 set the phase of the LO output to the demodulator. This enables the user to select the phase delay of the Rx LO signal to the demodulator in 90° steps. See the truth table in Figure 23. The Rx LO output can be disabled if desired.

Tx Modulation LO Phase Select

Bit T3, Bit T2, and Bit T1 set the input modulation of the VCO. Normal quadrature to each mixer can be replaced by choosing one LO phase to both mixers if desired. The normal (I) or quadrature (Q) phase can be chosen. See the truth table in Figure 23.

Band Select Clock

Bits BSC2 and Bit BSC1 set a divider for the band select logic clock input. The recommended setting is 1, 1, which programs a value of 8 to the divider. No other setting is allowed.

Reference Counter

R13 to R1 set the counter divide ratio. The divide range is 1 (00 … 001) to 8191 (111 … 111).

Rx CALIBRATION LATCH

With (C3, C2, C1) = (1, 0, 1), the Rx calibration latch is programmed. Figure 24 shows the input data format for programming the Rx calibration latch.

LO Phase Select

Bit P3, Bit P2, and Bit P1 set the phase of the LO output to the demodulator. This enables the user to select the phase delay of the Rx LO signal to the demodulator in 90° steps. See the truth table in Figure 24. The Rx LO output can be disabled if desired.

Tx Modulation LO Phase Select

Bit T3, Bit T2, and Bit T1 set the input modulation of the VCO. Normal quadrature to each mixer can be replaced by choosing one LO phase to both mixers if desired. The normal (I) or quadrature (Q) phase can be chosen. See the truth table in Figure 24.

Band Select Clock

Bit BSC2 and Bit BSC1 set a divider for the band select logic clock input. The recommended setting is 1, 1, which programs a value of 8 to the divider. No other setting is allowed.

Rx Filter Calibration

Setting Bit R13 high performs a calibration of the Rx filters' cutoff frequency, f_C. Setting this bit to 0 ensures the filter cutoff frequency calibration sequence is not initiated if this latch is programmed.

Rx Calibration Divider

Bit RC6 to Bit RC1 program a 6-bit divider, which outputs a divided REF_{IN} signal to assist calibration of the cutoff frequency, f_C, of the Rx filters. The calibration circuit uses this divided down PLL reference frequency to ensure an accurate cutoff frequency in the Rx filter. Choose the divider value to ensure that the frequency of the divided down signal is exactly 2 MHz, that is, if a 32 MHz crystal is used as the PLL REF_{IN} frequency, then a value of 16 is programmed to the counter to ensure accurate calibration.

High-Pass Filter Boost Timeout Counter

In most applications of the ADF9010, a high-pass filter is placed between the demodulator outputs and the ADF9010 Rx inputs. The capacitors used in these filters may require a long charge up time, and to address this, a filter boost function exists that charges up the capacitor to ~1.6 V. The duration for this boost is set by the product of the period of the Rx calibration signal, (REF_{IN} divided by the Rx calibration divider) and the 6-bit value programmed to these registers. This value can be as large as 63. Programming a value of 000000 leads to the calibration time being manually set by the HPF boost in the Rx latch. It becomes necessary in such cases to program this bit to 0 for normal Rx operation.

LO LATCH

Program the LO latch with (C2, C1) = (1, 0). Figure 25 shows the input data format for programming the LO latch.

Prescaler

Bit P2 and Bit P1 in the LO latch set the prescaler values.

CP Gain

Setting G1 to 0 chooses the programmed charge pump current setting from the control latch. Setting this bit to 1 chooses the maximum possible setting.

N Div Mux

Setting M1 to 0 feeds the VCO signals back to the N divider. Setting this bit to 1 allows the mux signal to be fed back instead.

B Counter Latch

Bit B13 to Bit B1 program the B counter. The divide range is 3 (00 … 0011) to 8191 (11 … 111).

A Counter Latch

Bit A5 to Bit A1 program the 5-bit A counter. The divide range is 0 (00000) to 31 (11111).

Rx LATCH

Program the Rx latch with (C2, C1) = (1, 1). Figure 26 shows the input data format for programming the LO latch.

High-Pass Filter Boost

This function is enabled by setting the HP bit to 1. A 0 disables this function. This is used to reduce settling time on the high-pass filter from the Rx demodulator. This is usually used in conjunction with the high-pass filter boost counter (See the RX Calibration Latch section).

Rx Filter Bandwidth

The Rx filter bandwidth is programmable and is controlled by Bit BW2 and Bit BW1. See the truth table in Figure 26.

Rx Filter Gain Steps

Bit G3 to Bit G1 set the gain of the Rx filters. The gain can vary from 3 dB to 24 dB in 3 dB steps. See the truth table in Figure 26.

INITIALIZATION

The correct initialization sequence for the ADF9010 is as follows:

1. Power-down all blocks: Tx, Rx, PLL, and VCO. Set the Tx output power off control latch to (1, 1). Set the LO phase select off (P1, P2, P3) in Tx latch to (1, 1, 1).
2. Program the R1 latch with the desired R counter and Tx values.
3. Program R5 with Rx calibration data for frequency calibration and high-pass filter boost.
4. Program R0 to power up all LO and Tx/Rx blocks.
5. Program R2 to encode correct LO frequency.
6. Program R3 to power up Rx filter.

INTERFACING

The ADF9010 has a simple SPI®-compatible interface for writing to the device. S_{CLK}, S_{DATA}, and S_{LE} control the data transfer. See Figure 2 for the timing diagram.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 833 kHz or one update every 1.2 µs. This is certainly more than adequate for systems that have typical lock times in hundreds of microseconds.

APPLICATIONS INFORMATION

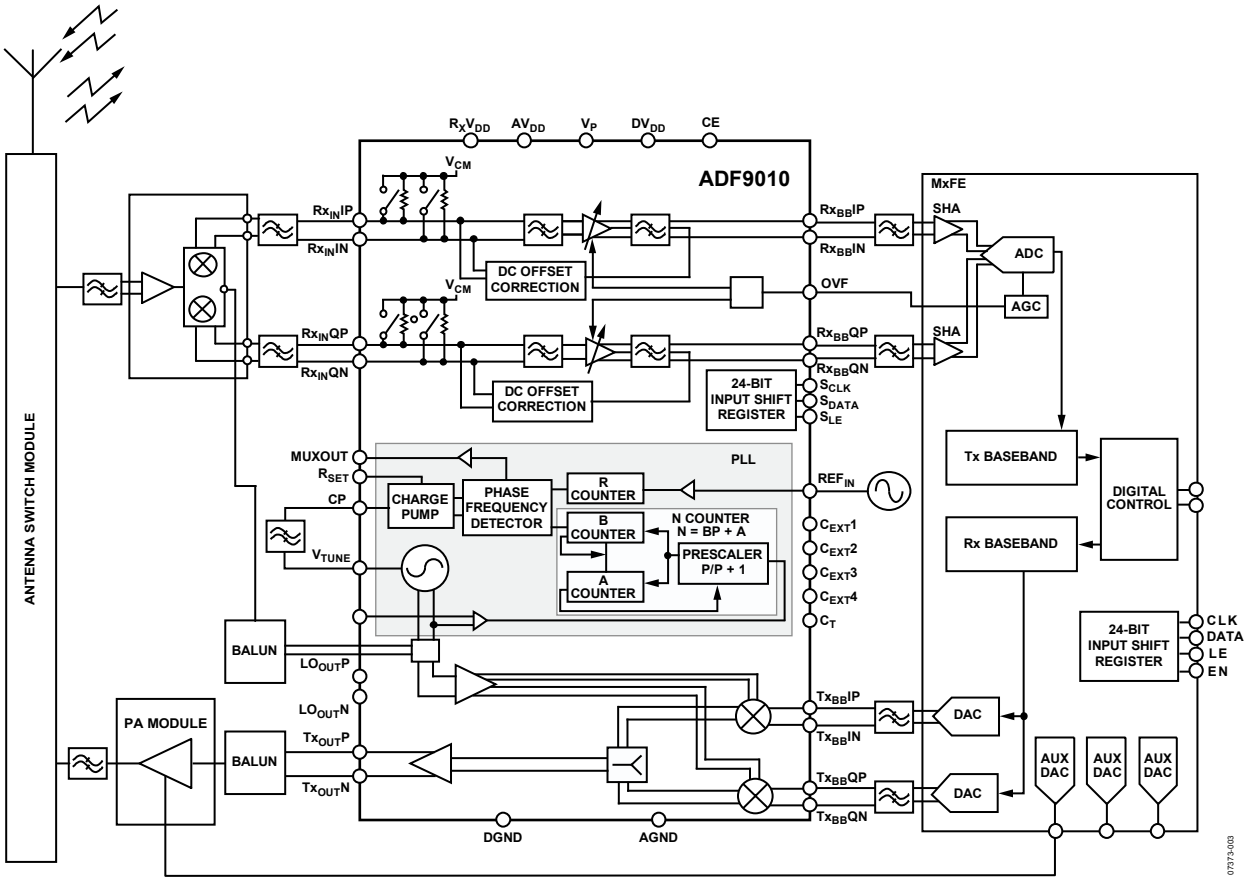


Figure 27. Applications Diagram

The diagram in Figure 27 shows the ADF9010 in an RFID application. The demodulator is driven by the $LO_{OUT}x$ pins of the ADF9010. This demodulator produces quadrature baseband signals that are gained up in the ADF9010 Rx filters. These filtered analog baseband signals are then digitized by the ADC on a mixed signal front-end (MxFE) part. The digital signals are then processed by DSP.

On the transmit side, the MxFE generates quadrature analog baseband signals, which are upconverted to RF using the integrated PLL and VCO. The modulated RF signals are combined using a balun and gained up to 30 dBm by a power amplifier.

DEMODULATOR CONNECTION

To receive the back-scattered signals from an RFID tag, the ADF9010 needs to be used with a high dynamic range demodulator, such as the ADL5382 that is suitable for RFID applications. Some extra filtration is provided by the optional shunt capacitors and series inductors. Due to the large self-blocker, a 100 nF capacitor removes the dc generated by the self-blocker inherent to RFID systems. This system is used on the EVAL-ADF9010EBZ1 evaluation board.

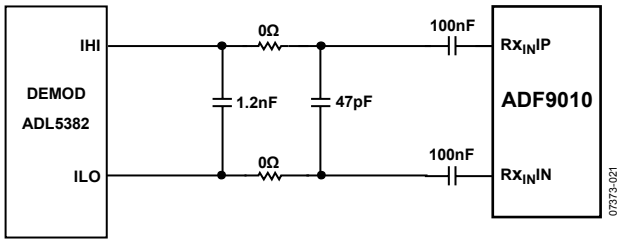


Figure 28. ADL5382 to ADF9010 Rx Interface

LO AND Tx OUTPUT MATCHING

The LO and Tx output stages are each connected to the collectors of an NPN differential pair driven by buffered outputs from the VCO or mixer outputs, respectively.

The recommended matching for each of these circuits consists of a 7.5 nH shunt inductor to V_{DD}, a 100 pF series capacitor, and in the case of the Tx output a 50:100 balun to combine the Tx outputs. The Anaren BD0810J50100A00 is ideally suited to this task.

PCB DESIGN GUIDELINES

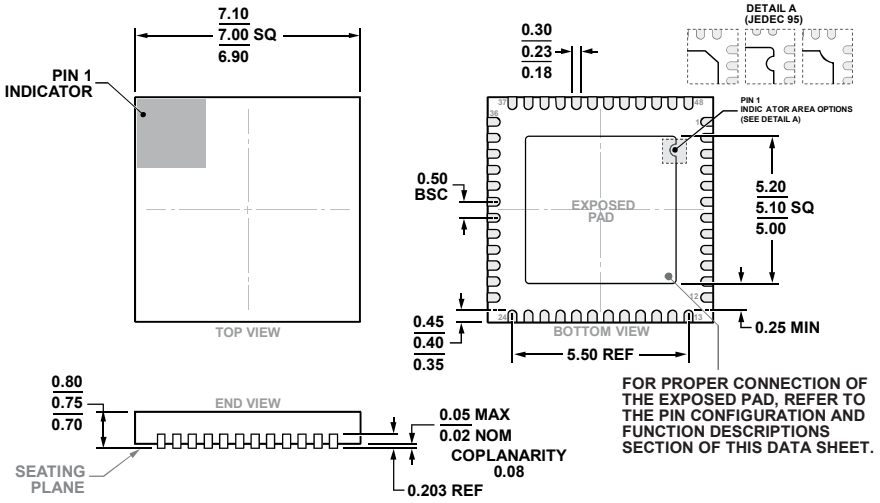
The lands on the chip scale package (CP-48-4) are rectangular. The printed circuit board pad for these must be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land must be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the chip scale package has a central thermal pad.

The thermal pad on the printed circuit board must be at least as large as this exposed pad. On the printed circuit board, there must be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias can be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they must be incorporated in the thermal pad at a 1.2 mm pitch grid. The via diameter must be between 0.3 mm and 0.33 mm, and the via barrel must be plated with 1 oz. copper to plug the via.

The user must connect the printed circuit board thermal pad to AGND.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WKKD-4

Figure 29. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF9010BCPZ	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package (LFCSP)	CP-48-4
ADF9010BCPZ-RL	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package (LFCSP)	CP-48-4
ADF9010BCPZ-RL7	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package (LFCSP)	CP-48-4
EVAL-ADF9010EBZ1		Evaluation Board	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).