

LTC2175-14/-12,  
 LTC2174-14/-12, LTC2173-14/-12, LTC2172-14/-12,  
 LTC2171-14/-12, LTC2170-14/-12  
 12-Bit/14-Bit, 25Msps to 125Msps Quad ADCs

## DESCRIPTION

Demonstration circuit 1525A supports a family of 14-Bit/12-Bit 25Msps to 125Msps ADCs. Each assembly features one of the following devices: LTC<sup>®</sup>2175-14, LTC2175-12, LTC2174-14, LTC2174-12, LTC2173-14, LTC2173-12, LTC2172-14, LTC2172-12, LTC2171-14, LTC2171-12, LTC2170-14, LTC2170-12 high speed, quad ADCs.

The versions of the 1525A demo board are listed in Table 1. Depending on the required resolution and sample rate,

the DC1525A is supplied with the appropriate ADC. The circuitry on the analog inputs is optimized for analog input frequencies from 5MHz to 140MHz. Refer to the data sheet for proper input networks for different input frequencies.

**Design files for this circuit board are available at <http://www.linear.com/demo>**

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**Table 1. DC1525A Variants**

DC1525A VARIANTS	ADC PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
1525A-A	LTC2175-14	14-Bit	125Msps	5MHz to 140MHz
1525A-B	LTC2174-14	14-Bit	105Msps	5MHz to 140MHz
1525A-C	LTC2173-14	14-Bit	80Msps	5MHz to 140MHz
1525A-D	LTC2172-14	14-Bit	65Msps	5MHz to 140MHz
1525A-E	LTC2171-14	14-Bit	40Msps	5MHz to 140MHz
1525A-F	LTC2170-14	14-Bit	25Msps	5MHz to 140MHz
1525A-G	LTC2175-12	12-Bit	125Msps	5MHz to 140MHz
1525A-H	LTC2174-12	12-Bit	105Msps	5MHz to 140MHz
1525A-I	LTC2173-12	12-Bit	80Msps	5MHz to 140MHz
1525A-J	LTC2172-12	12-Bit	65Msps	5MHz to 140MHz
1525A-K	LTC2171-12	12-Bit	40Msps	5MHz to 140MHz
1525A-L	LTC2170-12	12-Bit	25Msps	5MHz to 140MHz

# DEMO MANUAL DC1525A

## PERFORMANCE SUMMARY $(T_A = 25^\circ\text{C})$

PARAMETER	CONDITION	VALUE
Supply Voltage: DC1525A	Depending on Sampling Rate and the A/D Converter Provided, this Supply Must Provide Up to 500mA.	Optimized for 3V [3V ↔ 6.0V Min/Max]
Analog Input Range	Depending on SENSE Pin Voltage	1V <sub>p-p</sub> to 2V <sub>p-p</sub>
Logic Input Voltages	Minimum Logic High	1.3V
	Maximum Logic Low	0.6V
Logic Output Voltages (Differential)	Nominal Logic Levels (100Ω Load, 3.5mA Mode)	350mV/1.25V Common Mode
	Minimum Logic Levels (100Ω Load, 3.5mA Mode)	247mV/1.25V Common Mode
Sampling Frequency (Convert Clock Frequency)	See Table 1	
Encode Clock Level	Single-ended Encode Mode (ENC <sup>-</sup> Tied to GND)	0V to 3.6V
Encode Clock Level	Differential Encode Mode (ENC <sup>-</sup> Not Tied to GND)	0.2V to 3.6V
Resolution	See Table 1	
Input Frequency Range	See Table 1	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

## QUICK START PROCEDURE

Demonstration circuit 1525A is easy to set up to evaluate the performance of the LTC2175 A/D converters. Refer to Figure 1 for proper measurement equipment setup and follow this procedure.

### Setup

If a DC1371 QuikEval™ II Data Acquisition and Collection System was supplied with the DC1525A demonstration circuit, follow the DC1371 Quick Start Guide to install the required software and for connecting the DC1371 to the DC1525A and to a PC.

### DC1525A Demonstration Circuit Board Jumpers

The DC1525A demonstration circuit board should have the following jumper settings as default positions: (as per Figure 1).

J13: PAR/SER: Selects Parallel or Serial programming mode. (Default – Serial)

Optional Jumpers:

J8: Term: Enables/Disable optional output termination. (Default – Removed)

J5: ILVDS: Selects either 1.75mA or 3.5mA of output current for the LVDS drivers. (Default – Removed)

J14: LANE: Selects either 1 lane or 2 lane output modes (Default – Removed) NOTE: The DC1371 does not support 1 lane operation.

J15: SHDN: Enables and disables the LTC2175. (Default – Removed)

J2: WP: Enable/Disables write protect for the EEPROM. (Default – Removed)

Note: optional jumper should be left open to ensure proper serial configuration.

### Applying Power and Signals to the DC1525A Demonstration Circuit

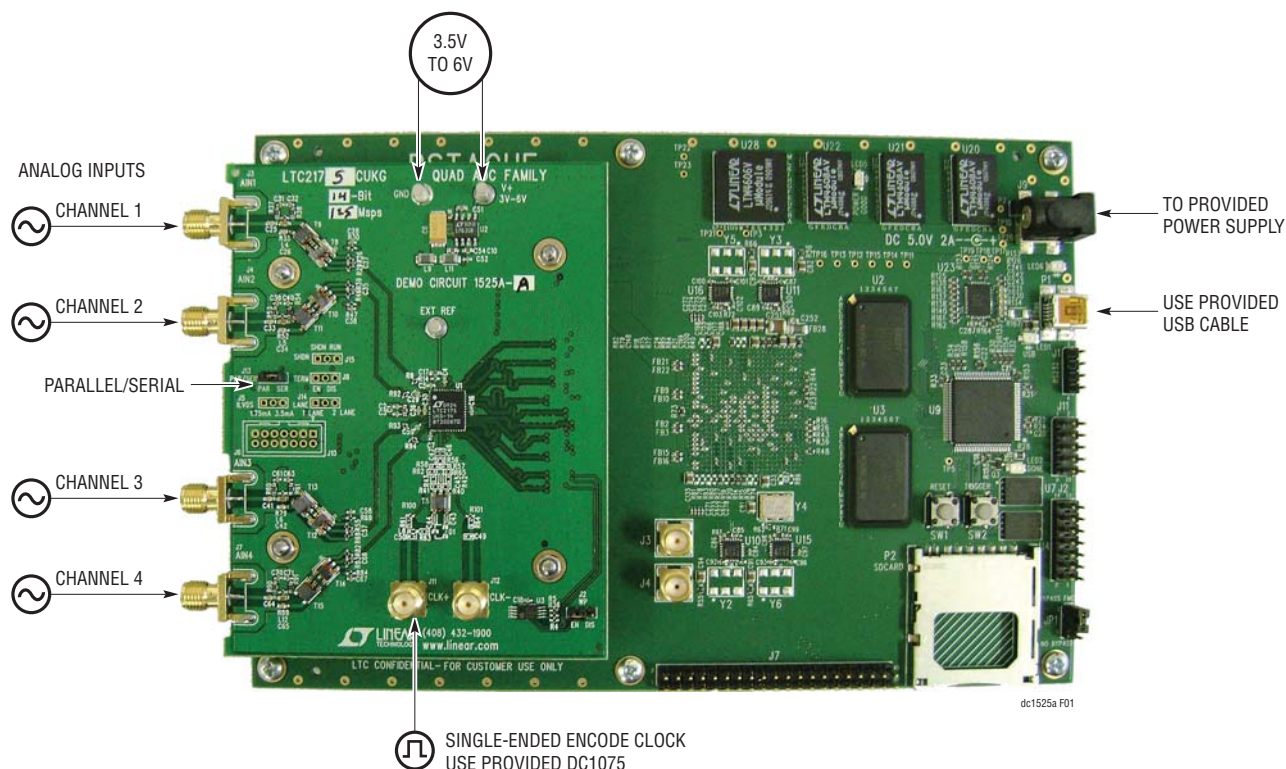
The DC1371 is used to acquire data from the DC1525A, the DC1371 must FIRST be connected to a powered USB port and have equal to 5V applied power BEFORE applying 3.6V to 6V across the pins marked V<sup>+</sup> and GND on the DC1525A. DC1525A requires 3.6V for proper operation.

Regulators on the board produce the voltages required for the ADC. The DC1525A demonstration circuit requires up to 500mA depending on the sampling rate and the A/D converter supplied.

The DC1525A should not be removed, or connected to the DC1371 while power is applied.

dc1525af

**QUICK START PROCEDURE**



**Figure 1. DC1525A Setup**

**Analog Input Network**

For optimal distortion and noise performance the RC network on the analog inputs may need to be optimized for different analog input frequencies. For input frequencies above 140MHz, refer to the LTC2175 data sheet for a proper input network. Other input networks may be more appropriate for input frequencies less than 5MHz.

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR.

The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

If your generator cannot deliver full-scale signals without distortion, you may benefit from a medium power amplifier based on a Gallium Arsenide Gain block prior to the final filter. This is particularly true at higher frequencies where IC based operational amplifiers may be unable to deliver

the combination of low noise figure and High IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively lower Q filter used between the amplifier and the demo circuit.

Apply the analog input signal of interest to the SMA connectors on the DC1525A demonstration circuit board marked J3 AIN1, J4 AIN2, J6 AIN3, J7 AIN4. These inputs correspond with channels 1 to 4 of the ADC respectively. These inputs are capacitive coupled to Balun transformers ETC1-1-13.

**Encode Clock**

**NOTE:** Apply an encode clock to the SMA connector on the DC1525A demonstration circuit board marked J11 CLK+. As a default the DC1525A is populated to have a single-ended input.

For the best noise performance, the ENCODE INPUT must be driven with a very low jitter, square wave source. The amplitude should be large, up to 3V<sub>P-P</sub> or 13dBm. When

## QUICK START PROCEDURE

using a sinusoidal signal generator a squaring circuit can be used. Linear Technology also provides demo board DC1075A that divides a high frequency sine wave by four, producing a low jitter square wave for best results with the LTC2175.

Using bandpass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. In the case of the DC1525A a bandpass filter used for the clock should be used prior to the DC1075A. Data sheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used for both the Clock input and the Analog input.

### Digital Outputs

Data outputs, data clock, and frame clock signals are available on J1 of the DC1525A. This connector follows the VITA-57/FMC standard, but all signals should be verified when using an FMC carrier card other than the DC1371.

### Software

The DC1371 is controlled by the PScope™ System Software provided or downloaded from the Linear Technology website at <http://www.linear.com/software/>.

To start the data collection software if PScope.exe is installed (by default) in \Program Files\LTC\PScope\, double click the PScope icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1525A demonstration circuit is properly connected to the DC1371, PScope should automatically detect the DC1525A, and configure itself accordingly.

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the Collect button should result in time and frequency plots displayed in the PScope window. Additional information and help for

PScope is available in the DC1371 Quick Start Guide and in the online help available within the PScope program itself.

### Serial Programming

PScope has the ability to program the DC1525A board serially through the DC1371. There are several options available in the LTC2175 family that are only available through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the Set Demo Bd Options icon on the PScope toolbar (Figure 3).

This will bring up the menu shown in Figure 4.

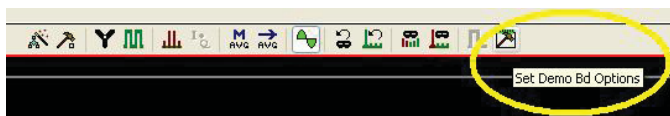


Figure 3. PScope Toolbar

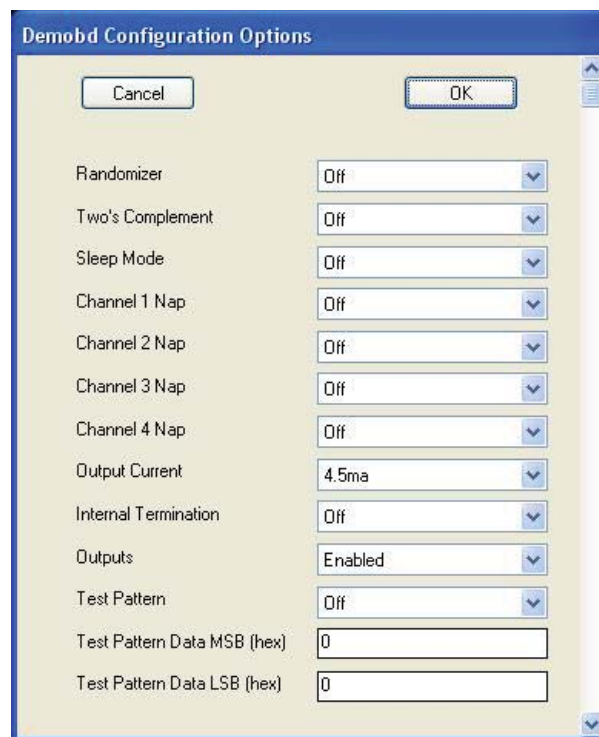


Figure 4. Demobd Configuration Options

## QUICK START PROCEDURE

This menu allows any of the options available for the LTC2175 family to be programmed serially. The LTC2175 family has the following options:

Randomizer: Enables Data Output Randomizer

- Off (Default): Disables data output randomizer
- On: Enables data output randomizer

Two's Complement: Enables two's complement mode

- Off (Default): Selects offset binary mode
- On: Selects two's complement mode

Sleep Mode: Selects between normal operation, sleep mode:

- Off (Default): Entire ADC is powered, and active
- On: The entire ADC is powered down.

Channel 1 Nap: Selects between normal operation and putting channel 1 in nap mode.

- Off (Default): Channel one is active
- On: Channel one is in nap mode

Channel 2 Nap: Selects between normal operation and putting channel 2 in nap mode.

- Off (Default): Channel two is active
- On: Channel two is in nap mode

Channel 3 Nap: Selects between normal operation and putting channel 3 in nap mode.

- Off (Default): Channel three is active
- On: Channel three is in nap mode

Channel 4 Nap: Selects between normal operation and putting channel 4 in nap mode.

- Off (Default): Channel four is active
- On: Channel four is in nap mode

Output Current: Selects the LVDS output drive current

- 1.75mA (Default): LVDS output driver current
- 2.1mA: LVDS output driver current
- 2.5mA: LVDS output driver current
- 3.0mA: LVDS output driver current
- 3.5mA: LVDS output driver current
- 4.0mA: LVDS output driver current
- 4.5mA: LVDS output driver current

Internal Termination: Enables LVDS internal termination

- Off (Default): Disables internal termination
- On: Enables internal termination

Outputs: Enables Digital Outputs

- Enabled (Default): Enables digital outputs
- Disabled: Disables digital outputs

Test Pattern: Selects Digital output test patterns. The desired test pattern can be entered into the text boxes provided.

- Off(default): ADC input data is displayed
- On: Test pattern is displayed.

Once the desired settings are selected hit OK and PScope will automatically update the register of the device on the DC1525A demo board.



# DEMO MANUAL DC1525A

## PARTS LIST

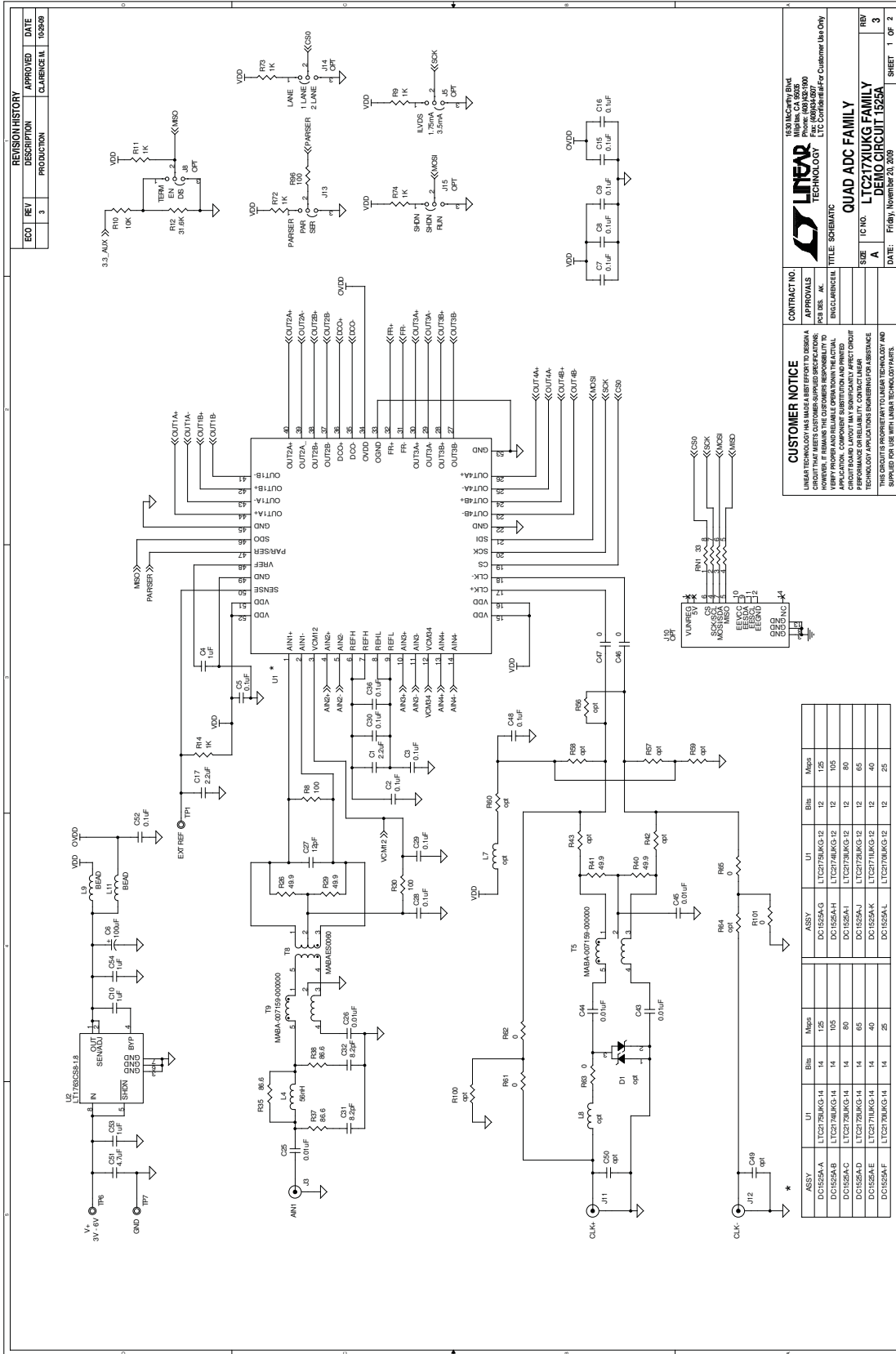
ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
<b>Required Circuit Components</b>				
1	2	C1, C17	CAP., X5R, 2.2 $\mu$ F, 10V, 10% 0603	NIC, NMC0603X5R225K10TRPF
2	19	C2, C3, C5, C7-C9, C15, C16, C18, C28, C29, C30, C36, C38, C48, C52, C58, C59, C67	CAP., X5R, 0.1 $\mu$ F, 10V, 10% 0402	AVX, 0402ZD104KAT2A
3	1	C4	CAP., X5R, 1 $\mu$ F, 10V, 10% 0402	MURATA, GRM155R61A105ME15
4	1	C6	CAP., TANT, 100 $\mu$ F, 10V% 6032	AVX, TAJW107K010R
5	3	C10, C53, C54	CAP., X7R, 1 $\mu$ F, 10V, 10% 0603	AVX, 0603ZC105KAT2A
6	8	C25, C26, C33, C34, C41, C42, C64, C65	CAP., X7R, 0.01 $\mu$ F, 50V, 10% 0603	AVX, 06035C103KAT2A
7	4	C27, C35, C57, C66	CAP., NPO, 12pF, 16V, 10% 0402	AVX, 0402YA120KAT2A
8	8	C31, C32, C39, C40, C61, C63, C70, C71	CAP., COG, 8.2pF, 50V, 5% 0402	AVX, 04025A8R2JAT2A
9	3	C43, C44, C45	CAP., X7R, 0.01 $\mu$ F, 16V, 10% 0402	AVX, 0402YC103KAT2A
10	0	C49, C50 OPT		
11	1	C51	CAP., X5R, 4.7 $\mu$ F, 6.3V 20% 0603	AVX, 06036D475MAT2A
12	0	D1 OPT		
13	1	J1	BGA CONNECTOR, 40 x 10	SAMTEC, SEAM-40-02.0-S-10-2-A
14	2	J2, J13	3 PIN 0.079 SINGLE ROW HEADER	SAMTEC, TMM103-02-L-S
15	2	XJ2, XJ13	SHUNT, 0.079" CENTER	SAMTEC, 2SN-BK-G
16	4	J3, J4, J6, J7	CON., SMA 50 $\Omega$ EDGE-LANCH	E. F. JOHNSON, 142-0701-851
17	0	J5, J8, J14, J15 OPT		
18	0	J10 OPT	HEADER, 2X7 PIN, 0.079CC	MOLEX, 87831-1420
19	2	J11, J12	CON., SMA 50 $\Omega$ STRAIGHT MOUNT	CONNEX., 132134
20	4	L4, L5, L6, L12	INDUCTOR, 56nH 0603	MURATA, LQP18MN56NG02D
21	0	L7, L8 OPT		
22	2	L11, L9	FERRITE BEAD, 1206	MURATA, BLM31PG330SN1L
23	1	RN1	RES 2X4 ARRAY, CHIP, 33 $\Omega$ , ISO	VISHAY, CRA06E08333R0JTA
24	4	R4, R5, R10, R36	RES., CHIP, 10k, 1/16W, 5% 0402	VISHAY, CRCW040210K0JNED
25	13	R8, R30, R47, R69, R84, R92, R93, R94, R95, R96, R97, R98, R99	RES., CHIP, 100 $\Omega$ , 1/16W, 5% 0402	VISHAY, CRCW0402100RJNED
26	6	R9, R11, R14, R72, R73, R74	RES., CHIP, 1k, 1/16W, 5% 0402	VISHAY, CRCW04021K00JNED
27	1	R12	RES., CHIP, 31.6k, 1/16W, 1% 0402	VISHAY, CRCW040231K6FKED
28	10	R26, R29, R39, R40, R41, R46, R55, R68, R82, R83	RES., CHIP, 49.9 $\Omega$ , 1/16W, 1% 0402	VISHAY, CRCW040249R9FKED
29	4	R35, R52, R79, R89	RES., CHIP, 86.6 $\Omega$ , 1/16W, 1% 0402	VISHAY, CRCW040286R6FKED
30	8	R37, R38, R53, R54, R80, R81, R90, R91	RES., CHIP, 86.6 $\Omega$ , 1/16W, 1% 0603	VISHAY, CRCW060386R6FNEA
31	8	R1, R61, R62, R63, R65, R101, C46, C47	RES., 0 $\Omega$ , 0402	VISHAY, CRCW04020000Z0ED
32	0	R2, R42, R43, R56, R57, R58, R59, R60, R64, R100, R110, R111, R112, R113, R114, R115, R116, R117	RES., OPT	
33	8	R102, R103, R104, R105, R106, R107, R108, R109	RES., CHIP, 33k, 1/16W, 5% 0402	VISHAY, CRCW040233K0JNED
34	3	TP1, TP6, TP7	TESTPOINT, TURRET, 0.094" PBF	MILL-MAX, 2501-2-00-80-00-00-07-0
35	5	T5, T9, T11, T13, T15	TRANSFORMER, MABA-007159-000000	M/A-COM, MABA-007159-000000
36	4	T8, T10, T12, T14	TRANSFORMER, MABAES0060	M/A-COM, MABAES0060

## PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
37	1	U2	I.C., LT1763CS8-1.8, S08	LINEAR, LT1763CS8-1.8#TRPBF
38	1	U3	I.C., 24LC32A, TSSOP-8	MICROCHIP, 24LC32A I /ST
1	1	DC1525A	GENERAL BOM	
2	1	U1 (DC1525A-A)	I.C., LTC2175-14, 7mm × 8mm QFN	LINEAR., LTC2175IUKG-14#PBF
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1525A
1	1	DC1525A	GENERAL BOM	
2	1	U1 (DC1525A-B)	I.C., LTC2174-14, 7mm × 8mm QFN	LINEAR., LTC2174IUKG-14#PBF
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1525A
1	1	DC1525A	GENERAL BOM	
2	1	U1 (DC1525A-C)	I.C., LTC2173-14, 7mm × 8mm QFN	LINEAR., LTC2173IUKG-14#PBF
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1525A
1	1	DC1525A	GENERAL BOM	
2	1	U1 (DC1525A-D)	I.C., LTC2172-14, 7mm × 8mm QFN	LINEAR., LTC2172IUKG-14#PBF
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1525A
1	1	DC1525A	GENERAL BOM	
2	1	U1 (DC1525A-E)	I.C., LTC2171-14, 7mm × 8mm QFN	LINEAR., LTC2171IUKG-14#PBF
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1525A
1	1	DC1525A	GENERAL BOM	
2	1	U1 (DC1525A-F)	I.C., LTC2170-14, 7mm × 8mm QFN	LINEAR., LTC2170IUKG-14#PBF
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1525A
1	1	DC1525A	GENERAL BOM	
2	1	U1 (DC1525A-G)	I.C., LTC2175-12, 7mm × 8mm QFN	LINEAR., LTC2175IUKG-12#PBF
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1525A
1	1	DC1525A	GENERAL BOM	
2	1	U1 (DC1525A-H)	I.C., LTC2174-12, 7mm × 8mm QFN	LINEAR., LTC2174IUKG-12#PBF
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1525A
1	1	DC1525A	GENERAL BOM	
2	1	U1 (DC1525A-I)	I.C., LTC2173-12, 7mm × 8mm QFN	LINEAR., LTC2173IUKG-12#PBF
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1525A
1	1	DC1525A	GENERAL BOM	
2	1	U1 (DC1525A-J)	I.C., LTC2172-12, 7mm × 8mm QFN	LINEAR., LTC2172IUKG-12#PBF
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1525A
1	1	DC1525A	GENERAL BOM	
2	1	U1 (DC1525A-K)	I.C., LTC2171-12, 7mm × 8mm QFN	LINEAR., LTC2171IUKG-12#PBF
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1525A
1	1	DC1525A	GENERAL BOM	
2	1	U1 (DC1525A-L)	I.C., LTC2170-12, 7mm × 8mm QFN	LINEAR., LTC2170IUKG-12#PBF
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1525A

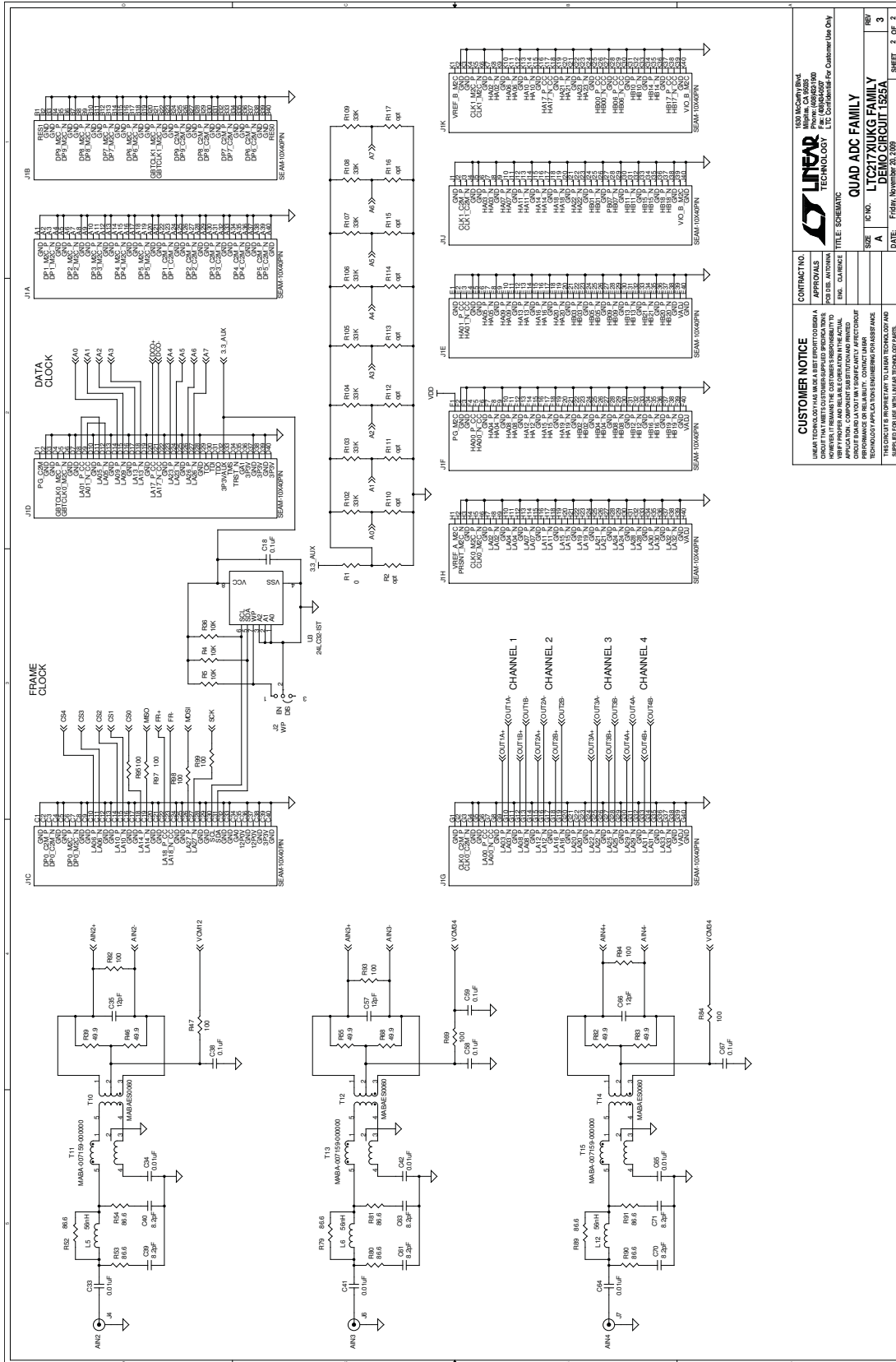
# DEMO MANUAL DC1525A

## SCHEMATIC DIAGRAM





## SCHEMATIC DIAGRAM



<b>CUSTOMER NOTICE</b>		LTC2171X1UG FAMILY DEMO CIRCUIT 1525A	
LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A SCHEMATIC THAT REPRESENTS THE CUSTOMER'S REQUIREMENTS. HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY THE SCHEMATIC REPRESENTS THE ACTUAL CIRCUIT AS BUILT AND TO TAKE NECESSARY PRECAUTIONS TO AVOID DAMAGE TO THE DEVICE OR TO THE BOARD. THE SCHEMATIC IS PROVIDED AS A GUIDE ONLY AND IS NOT A SUBSTITUTE FOR THE ACTUAL BOARD. SUPPLY FOR USE WITH LINEAR TECHNOLOGY PARTS.		DATE: Friday, November 20, 2009	
<b>CONTRACT NO.</b>		APPROVALS	
JOB NO. AN7000000		DESIGNER: AN7000000	
CHK. CURRANCE		TITLE: SCHEMATIC	
SIZE: A		REV: 3	
DATE: Friday, November 20, 2009		SHEET: 2 OF 2	

LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A SCHEMATIC THAT REPRESENTS THE CUSTOMER'S REQUIREMENTS. HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY THE SCHEMATIC REPRESENTS THE ACTUAL CIRCUIT AS BUILT AND TO TAKE NECESSARY PRECAUTIONS TO AVOID DAMAGE TO THE DEVICE OR TO THE BOARD. THE SCHEMATIC IS PROVIDED AS A GUIDE ONLY AND IS NOT A SUBSTITUTE FOR THE ACTUAL BOARD. SUPPLY FOR USE WITH LINEAR TECHNOLOGY PARTS.

# DEMO MANUAL DC1525A

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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