LTM2885
Isolated RS485/RS422
µModule Transceiver + Power

DESCRIPTION

Demonstration circuit 1794A is an isolated RS485/RS422 µModule® transceiver + power featuring the LTM®2885. The demo circuit is a 6500V_{RMS} galvanically isolated RS485/RS422 transceiver interface. The demo circuit features an EMI optimized circuit configuration and printed circuit board layout. The demo circuit operates from a single external supply on V_{CC}. The part generates the output voltage V_{CC2} and communicates all necessary signaling across the isolation barrier using LTC's isolator µModule technology.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY (T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Input Supply Range	LTM2885	4.5	5	5.5	V
V_{CC2}	Output Voltage	I_{LOAD} = 0mA to 100mA, DE = 0V	4.75	5		V
f_{MAX}	Maximum Data rate	$\overline{SLO}$ = V_{CC2}	20			Mbps
V_{IORM}	Maximum Working Insulation Voltage	GND to GND2	890 600			V_{DC} V_{RMS}
	Common Mode Transient Immunity		50			kV/µs

OPERATING PRINCIPLES

The LTM2885 contains an isolated DC/DC converter, delivering power to V_{CC2} at 5V from the input supply, V_{CC}. Isolation is maintained by the separation of GND and GND2, which significant operating voltages and transients can exist without affecting the operation of the LTM2885. The logic side ON pin enables or shuts down the LTM2885. RS485/RS422 signaling is controlled by the logic inputs DE, DI, TE and $\overline{RE}$. Connection to the transceiver pins (A, B, Y and Z) allows full- or half-duplex operation on the isolated side of the demo circuit. A full-/half-duplex jumper is included on the demo circuit to ease setting the system configuration. The $\overline{SLO}$ pin configures the slew rate of the driver output pins Y and Z.

Data is transmitted out the driver pins Y and Z from the input DI with DE set on. Data is received through the difference in A and B to the output RO with $\overline{RE}$ set on.

The LTM2885 µModule and demo circuit has been designed and optimized for low RF emissions. To this end some features of the LTM2885 are not available for evaluation on the demo circuit, primarily to minimize the size of the demo board and to limit the number of I/O connections. The logic supply voltage, V_L, is tied to V_{CC} on the demo circuit. All control signals are selectable by jumper programming only, including ON, $\overline{RE}$, DE, TE and $\overline{SLO}$. The spare logic channel D_{IN} to D_{OUT} is not available.

OPERATING PRINCIPLES

EMI mitigation techniques used include the following:

1. Board/ground plane size has been minimized. This reduces the dipole antenna formed between the logic side and isolated side ground planes.
2. Top signal routing and ground floods have been optimized to reduce signal loops, minimizing differential mode radiation.
3. A high ESR tantalum capacitor is included to minimize board resonances and prevent voltage spikes due to hot plugging of the input supply voltage.
4. Optional discrete bridge capacitors (C3, C4) can be mounted between GND2 and GND. The discrete capacitors provide additional attenuation at frequencies below 300MHz as shown in Figure 1. Capacitors are safety rated type Y1, manufactured by Vishay, part # VY115K31Y5SQ63V0.

EMI performance is shown in Figure 1, measured using a Gigahertz Transverse Electromagnetic (GTEM) cell and method detailed in IEC 61000-4-20, “Testing and Measurement Techniques—Emission and Immunity Testing in Transverse Electromagnetic Waveguides”.

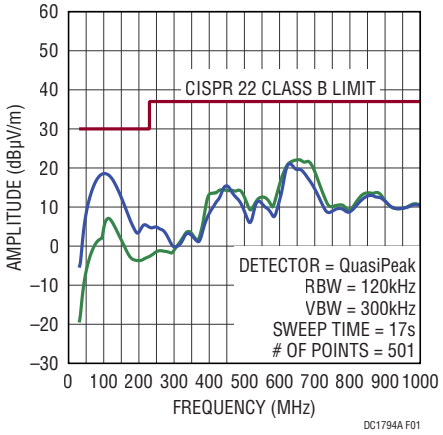


Figure 1. DC1794A Radiated Emissions

QUICK START PROCEDURE

Demonstration circuit 1794A is easy to set up and evaluate the performance of the LTM2885. Refer to Figure 2 for proper measurement equipment setup and follow the procedure below.

NOTE: When measuring the input or output voltage ripple or high speed signals, care must be taken to avoid a long ground lead on the oscilloscope probe.

1. Install jumpers in following positions: (all are default except JP5 and JP6)

   JP1 (TE pin) place in ON position

   JP2 (DE pin) place in ON position

   JP3 ($\overline{RE}$ pin) place in ON position

   JP4 (ON pin) place in ON position

   JP5 ($\overline{SLO}$ pin) place in OFF position

   JP6 (Duplex header) place in HALF DUPLEX position

2. With power off, connect the input power supply to V_{CC} and GND turrets.

3. Turn on the power at the input.

   NOTE: Make sure that the input voltage does not exceed 6V.

4. Check for the proper output voltage. V_{CC2} = 5V, this can be measured between probe points V_{CC2} and GND2.

5. Once the proper output voltage is established, connect a function generator to TXD turret and set to square wave with a low of 0V, high = V_{CC}. Set frequency to 10MHz (20Mbps). Enable output of function generator.

6. Connect oscilloscope to RXD turret and observe 10MHz waveform. This demonstration shows data that is transmitted from TXD, loops back through half-duplex connection, and out of RXD.

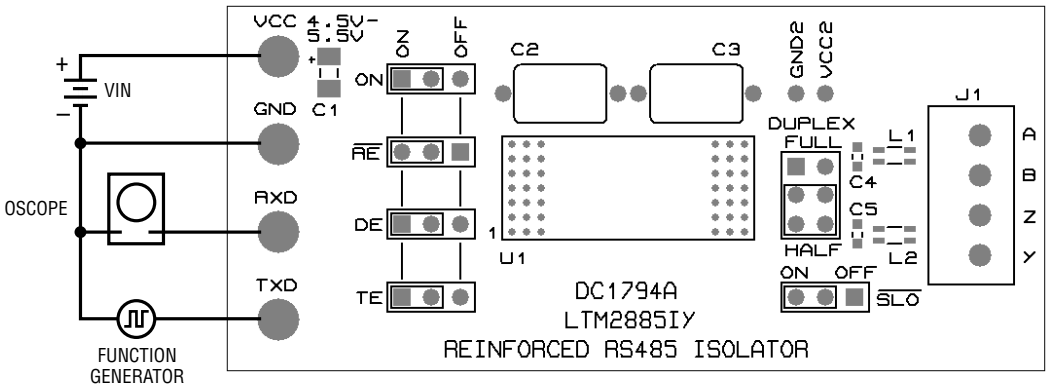
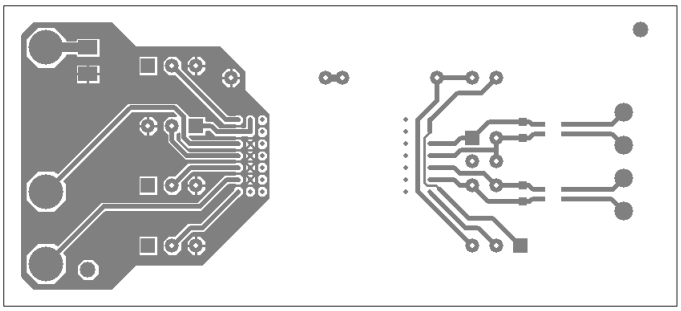
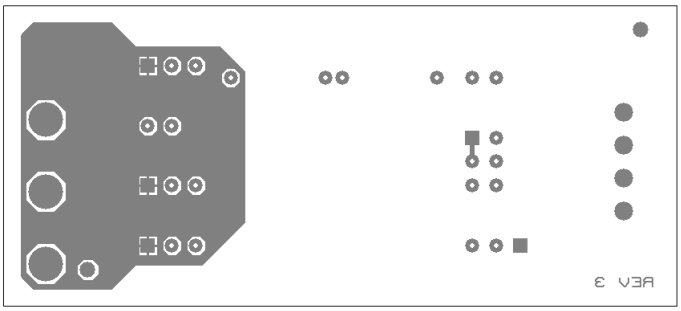


Figure 2. Demo Board Setup

PCB LAYOUT



Layer 1. Top Layer

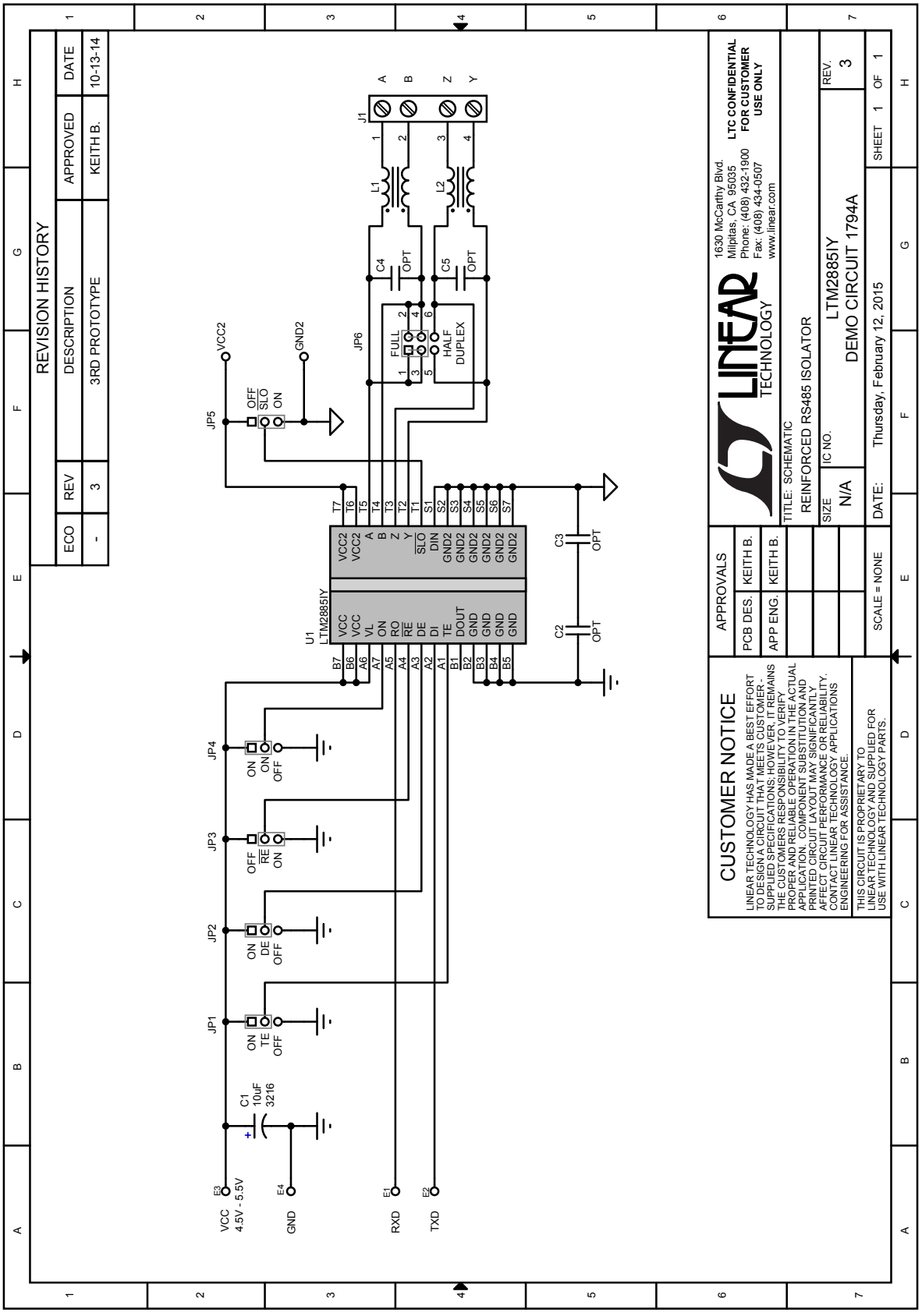


Layer 2. Bottom Layer

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	U1	I.C., LTM2885IY	LINEAR LTM2885IY#PBF
Hardware/Components (For Demo Board Only)				
2	1	C1	CAP., TANT 10µF 16V 10% 3216	AVX TAJA106K016RNJ
3	4	E1-4	TURRET	MILL-MAX 2501-2-00-80-00-00-07-0
4	2	J1	TERMINAL BLOCK, 2 POSITION, 3.5mm, HEADER	WÜRTH 691214110002
5	5	JP1-5	HEADER, 1×3 0.1"	WÜRTH 61300311121
6	1	JP6	HEADER, 2×3 0.1"	WÜRTH 61300621121
7	5	JP1-5	SHUNT, 1×2 0.1", BLACK	WÜRTH 60900213421
8	1	JP6	SHUNT, 2×2 0.1", BLACK	WÜRTH 60910213421
9	2	L1-2	COMMON MODE CHOKE	WÜRTH 744232222
10	0	C2-3	OPTIONAL, CAP., X1Y1, 150pF 10% 760VAC	VISHAY VY1151K31Y5SQ63V0
11	0	C4-5	OPTIONAL	

SCHEMATIC DIAGRAM



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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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