QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 1369
12/14 BIT, 25 TO 150 MSPS ADC

LTC2261-14, LTC2261-12, LTC2260-14, LTC2260-12, LTC2259-14, LTC2259-12, LTC2258-14, LTC2258-12, LTC2257-14, LTC2257-12, LTC2256-14, LTC2256-12, LTC2262-14, LTC2262-12

DESCRIPTION

Demonstration circuit 1369 supports a family of 14/12 BIT 125 MSPS ADCs. Each assembly features one of the following devices: LTC2261-14, LTC2261-12, LTC2260-14, LTC2260-12, LTC2259-14, LTC2259-12, LTC2258-14, LTC2258-12, LTC2257-14, LTC2257-12, LTC2256-14, LTC2256-12, LTC2262-14, or LTC2262-12 high speed, high dynamic range ADCs.

Demonstration circuit 1369 supports the LTC2261 family DDR LVDS output mode. This family of ADCs is also supported by demonstration circuit 1370A, which is compatible with CMOS and DDR CMOS output modes.

Several versions of the 1369A demo board supporting the LTC2261 12/14-BIT series of A/D converters are listed in Table 1. Depending on the required resolution and sample rate, the DC1369 is supplied with the appropriate ADC. The circuitry on the analog inputs is optimized for analog input frequencies from 5 MHz to 170MHz. Refer to the datasheet for proper input networks for different input frequencies.

Design files for this circuit board are available. Call the LTC factory.

Table 1. DC1369Variants

DC1369 VARIANTS	ADC PART NUMBER	RESOLUTION*	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
1369A-A	LTC2261-14	14-BIT	125 Msps	5MHz-170MHz
1369A-B	LTC2260-14	14-BIT	105 Msps	5MHz-170MHz
1369A-C	LTC2259-14	14-BIT	80 Msps	5MHz-170MHz
1369A-D	LTC2258-14	14-BIT	65 Msps	5MHz-170MHz
1369A-E	LTC2257-14	14-BIT	40 Msps	5MHz-170MHz
1369A-F	LTC2256-14	14-BIT	25 Msps	5MHz-170MHz
1369A-G	LTC2261-12	12-BIT	125 Msps	5MHz-170MHz
1369A-H	LTC2260-12	12-BIT	105 Msps	5MHz-170MHz
1369A-I	LTC2259-12	12-BIT	80 Msps	5MHz-170MHz
1369A-J	LTC2258-12	12-BIT	65 Msps	5MHz-170MHz
1369A-K	LTC2257-12	12-BIT	40 Msps	5MHz-170MHz
1369A-L	LTC2256-12	12-BIT	25 Msps	5MHz-170MHz
1369A-M	LTC2262-14	14-BIT	150Msps	5MHz-170MHz
1369A-N	LTC2262-12	12-BIT	150Msps	5MHz-170MHz

Table 2. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage – DC1369A	Depending on sampling rate and the A/D converter provided, this supply must provide up to 250mA.	Optimized for 3.6V [3.5V ⇔6.0V min/max]
Analog input range	Depending on SENSE Pin Voltage	1 V_{PP} to 2V_{PP}
Logic Input Voltages	Minimum Logic High	1.3V
	Maximum Logic Low	0.6V
Logic Output Voltages (differential)	Nominal Logic levels (100Ω load, 3.5mA Mode)	350mV/1.25V common mode
	Minimum Logic levels (100Ω load, 3.5mA Mode)	247mV/1.25V common mode
Sampling Frequency (Convert Clock Frequency)	See Table 1	
Convert Clock Level	Single ended Encode Mode (ENC- tied to GND)	0-3.6V
Convert Clock Level	Differential Encode Mode (ENC- not tied to GND)	0.2V-3.6V
Resolution	See Table 1	
Input frequency range	See Table 1	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

QUICK START PROCEDURE

Demonstration circuit 1369 is easy to set up to evaluate the performance of the LTC2261 A/D converters. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

SETUP

If a DC890 FastDAACS Data Acquisition and Collection System was supplied with the DC1369 demonstration circuit, follow the DC890 Quick Start Guide to install the required software and for connecting the DC890 to the DC1369 and to a PC running Windows98, 2000 or XP.

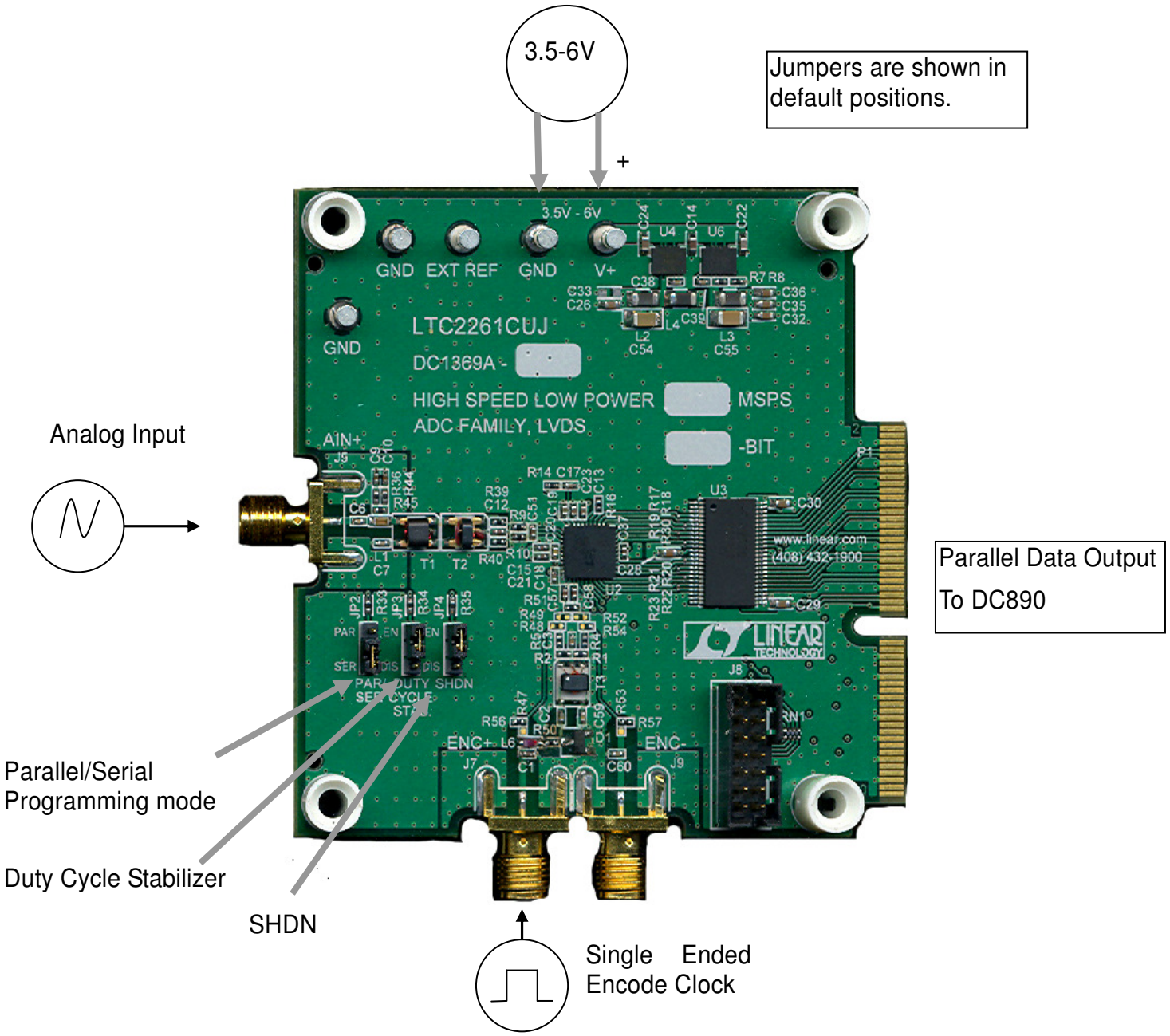


Figure 1. DC1369 Setup (zoom for detail)

DC1369 DEMONSTRATION CIRCUIT BOARD JUMPERS

The DC1369 demonstration circuit board should have the following jumper settings as default positions: (as per Figure 1)

JP2: PAR/SER : Selects Parallel or Serial programming mode. (Default - Serial)

JP3: Duty Cycle Stabilizer: Enables/ Disable Duty Cycle Stabilizer. (Default - Enable)

JP4: SHDN: Enables and disables the LTC2261. (Default - Enable)

APPLYING POWER AND SIGNALS TO THE DC996 DEMONSTRATION CIRCUIT

If a DC890 is used to acquire data from the DC1369, the DC890 must FIRST be connected to a powered USB port or provided an external 6-9V BEFORE applying +3.6V to +6.0V across the pins marked "V+" and "GND" on the DC1369. DC1369 requires 3.6V for proper operation. Regulators on the board produce the voltages required for the ADC. The DC1369 demonstration circuit requires up to 250mA depending on the sampling rate and the A/D converter supplied.

The DC890 data collection board is powered by the USB cable and does not require an external power supply unless it must be connected to the PC through an un-powered hub, in which case it must be supplied an external 6-9V on turrets G7(+) and G1(-) or the adjacent 2.1mm power jack.

ANALOG INPUT NETWORK

For optimal distortion and noise performance the RC network on the analog inputs may need to be optimized for different analog input frequencies. For input frequencies above 170 MHz, refer to the LTC2261 datasheet for a proper input network. Other input networks may be more appropriate for input frequencies less that 5MHz.

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR. In the case of the DC1369 a band pass filter used for the clock should be used prior to the DC1075A.

The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

If your generator cannot deliver full scale signals without distortion, you may benefit from a medium power amplifier based on a Gallium Arsenide Gain block prior to the final filter. This is particularly true at higher frequencies where IC based operational amplifiers may be unable to deliver the combination of low noise figure and High IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively lower Q filter used between the amplifier and the demo circuit.

ENCODE CLOCK

NOTE: Apply an encode clock to the SMA connector on the DC1369 demonstration circuit board marked "J7". As a default the DC1369 is populated to have a single ended input.

For the best noise performance, the ENCODE INPUT must be driven with a very low jitter, square wave source. The amplitude should be large, up to $3V_{P-P}$ or 13dBm. When using a sinusoidal signal generator a squaring circuit can be used. Linear Technology also provides demo board DC1075A that divides a high frequency sine wave by four, producing a low jitter square wave for best results with the LTC2261.

Using band pass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. In the case of the DC1369 a band pass filter used for the clock should be used prior to the DC1075A. Datasheet FFT

plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used with TTE band pass filters for both the Clock input and the Analog input.

Apply the analog input signal of interest to the SMA connectors on the DC1369 demonstration circuit board marked "J5 AIN+". These inputs are capacitive coupled to Balun transformers ETC1-1-13.

An internally generated conversion clock output is available on J1 which could be collected via a logic analyzer, or other data collection system if populated with a SAMTEC MEC8-150 type connector or collected by the DC890 QuickEval-II Data Acquisition Board using PScope software.

SOFTWARE

The DC890B is controlled by the PScope System Software provided or downloaded from the Linear Technology website at http://www.linear.com/software/. If a DC890B was provided, follow the DC890 Quick Start Guide and the instructions below.

To start the data collection software if "PScope.exe", is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1369 demonstration circuit is properly connected to the DC890, PSCOPE should automatically detect the DC1369, and configure itself accordingly. If necessary the procedure below explains how to manually configure PSCOPE.

Under the "Configure" menu, go to "ADC Configuration...." Check the "Config Manually" box and use the following configuration options, see Figure 2:

Manual Configuration settings:

Bits: 14

Alignment: 14

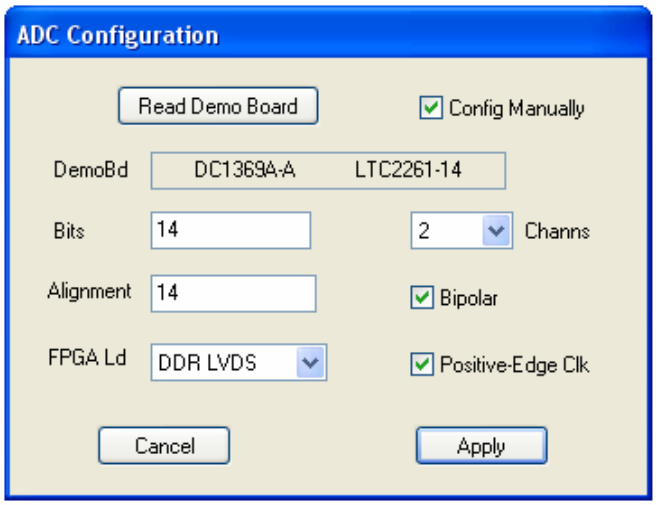
FPGA Ld: DDR LVDS

Channs: 2

Bipolar: Checked

Positive-Edge Clk: Checked

Figure 2: ADC configuration



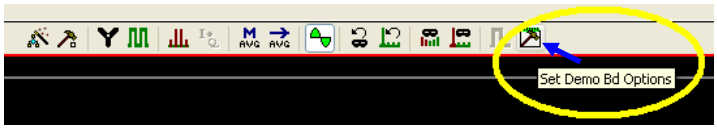
If everything is hooked up properly, powered and a suitable convert clock is present, clicking the "Collect" button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC890B Quick Start Guide and in the online help available within the PScope program itself.

SERIAL PROGRAMMING

PScope has the ability to program the DC1369 board serially through the DC890. There are several options available in the LTC2261 family that are only available through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the "Set Demo Bd Options" icon on the PScope toolbar (Figure 3).

Figure 3: PScope Toolbar



This will bring up the menu shown in figure 4.

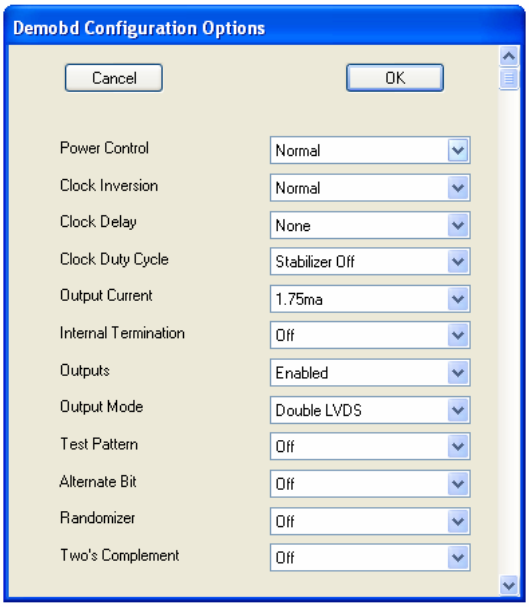


Figure 4: Demobd Configuration Options.

This menu allows any of the options available for the LTC2261 family to be programmed serially. The LTC2261 family has the following options:

Power Control – Selects between normal operation, nap, and sleep modes:

- Normal (Default) – Entire ADC is powered, and active

- Nap – ADC core powers down while references stay active.

- Shutdown – The entire ADC is powered down.

Clock Inversion – Selects the polarity of the CLKOUT signal:

- Normal (Default) – Normal CLKOUT polarity

- Inverted – CLKOUT polarity is inverted

Clock Delay - Selects the phase delay of the CLKOUT signal:

- None (Default) – No CLKOUT delay

- 45 deg – CLKOUT delayed by 45 degrees

- 90 deg – CLKOUT delayed by 90 degrees

- 135 deg – CLKOUT delayed by 135 degrees

Clock Duty Cycle – Enable or disables Duty Cycle Stabilizer

- Stabilizer off (Default) – Duty Cycle Stabilizer Disabled

- Stabilizer on – Duty Cycle Stabilizer Enabled

Output Current – Selects the LVDS output drive current

- 1.75mA (Default) - LVDS output driver current

- 2.1mA - LVDS output driver current

- 2.5mA - LVDS output driver current

- 3.0mA - LVDS output driver current

- 3.5mA - LVDS output driver current

- 4.0mA - LVDS output driver current

- 4.5mA - LVDS output driver current

Internal Termination – Enables LVDS internal termination

- Off (Default) – Disables internal termination

- On – Enables internal termination

Outputs – Enables Digital Outputs

- Enabled (Default) – Enables digital outputs

- Disabled – Disables digital outputs

Output Mode – Selects Digital output mode

- Full Rate – Full rate CMOS output mode (This mode is not supported by the DC1369A, please use the DC1370)

- Double LVDS (Default) – double data rate LVDS output mode

- Double CMOS – double data rate CMOS output mode (This mode is not supported by the DC1369A, please use the DC1370)

Test Pattern – Selects Digital output test patterns

- Off (Default) – ADC data presented at output

- All out =1 – All digital outputs are 1

- All out = 0 – All digital outputs are 0

- Checkerboard - OF, and D13-D0 Alternate between 101 0101 1010 0101 and 010 1010 0101 1010 on alternating samples.

- Alternating – Digital outputs alternate between all 1's and all 0's on alternating samples.

Alternate Bit – Alternate Bit Polarity (ABP) Mode

- Off (Default) – Disables alternate bit polarity

- On – Enables alternate bit polarity (Before enabling ABP, be sure the part is in offset binary mode)

Randomizer – Enables Data Output Randomizer

- Off (Default) – Disables data output randomizer

- On – Enables data output randomizer

Two's complement – Enables two's complement mode

- Off (Default) – Selects offset binary mode

- On – Selects two's complement mode

Once the desired settings are selected hit OK and PScope will automatically update the register of the device on the DC1369 demo board.