LT8337/LT8337-1

28V, 5A Low I_Q Synchronous Step-Up Silent Switcher with PassThru

FEATURES

- **Silent Switcher® Architecture**
  - **Ultralow EMI Emissions**
  - **Optional Spread Spectrum Frequency Modulation**
- **Integrated 28V, 5A Power Switches**
- **Wide Input Voltage Range: 2.7V to 28V**
- **Output Voltage Programmable Up to 26V**
- **Low V_{IN} Pin Quiescent Current**
  - **0.3µA in Shutdown**
  - **4µA in Burst Mode® Operation (LT8337)**
  - **15µA in PassThru™ (LT8337)**
- **100% Duty Cycle Capability for Synchronous MOSFET**
- **External Compensation: Fast Transient Response (LT8337-1)**
- Power Good Monitor (LT8337)
- Adjustable and Synchronizable: 300kHz to 3MHz
- Pulse-Skipping or Burst Mode Operation at Light Load
- Small 16-Lead (3mm × 3mm) LQFN Package

APPLICATIONS

- Battery-Powered Systems
- General Purpose Step-Up

DESCRIPTION

The LT®8337/LT8337-1 is a low I_Q, synchronous step-up DC/DC converter. It features Silent Switcher architecture and optional spread spectrum frequency modulation (SSFM) to minimize EMI emissions while delivering high efficiencies at high switching frequencies.

The wide input/output voltage range, low V_{IN} pin quiescent current in Burst Mode operation, and 100% duty-cycle capability for the synchronous MOSFET in PassThru operation ($V_{IN} > V_{OUT}$) makes the LT8337/LT8337-1 ideally suited for battery-powered systems and general purpose step-up applications.

The LT8337/LT8337-1 integrates 28V, 5A power switches, operating at a fixed switching frequency programmable between 300kHz and 3MHz and synchronizable to an external clock. The LT8337/LT8337-1 features output soft-start and output overvoltage lockout.

The LT8337-1 allows external compensation via the V_C pin for fast transient response. The LT8337 offers an output power good flag via the PG pin.

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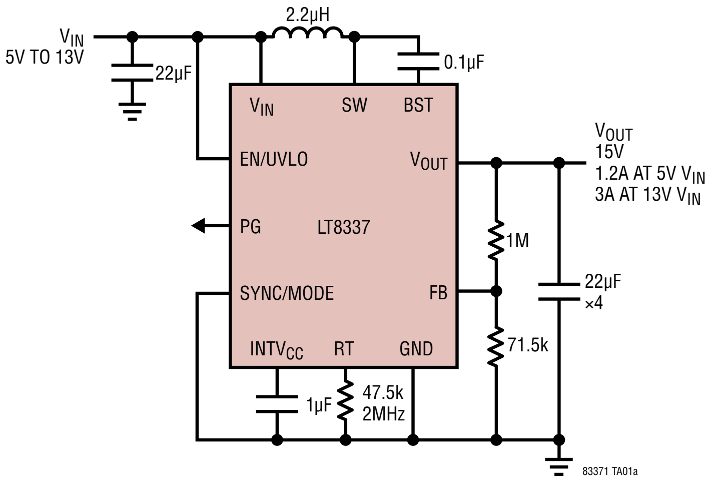
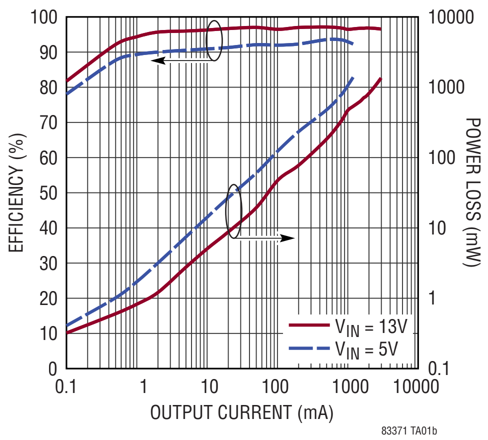
TYPICAL APPLICATION

High Efficiency 5V to 13V Input, 2MHz, 15V Output Boost Converter



Efficiency

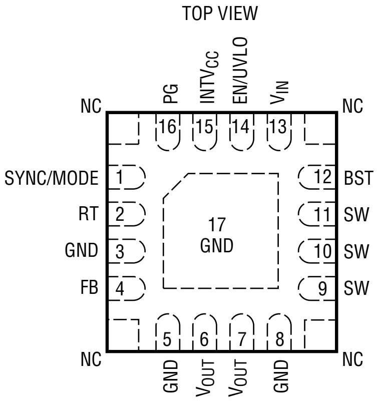


ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN}, V_{OUT}, EN/UVLO	28V
SYNC/MODE, FB	6V
PG (LT8337)	10V
V_C (LT8337-1)	2.5V
Operating Junction Temperature Range (Notes 2, 3)	
LT8337EV/LT8337EV-1	–40°C to 125°C
LT8337JV/LT8337JV-1	–40°C to 150°C
Storage Temperature Range	–65°C to 150°C
Maximum Reflow (Package Body) Temperature	260°C

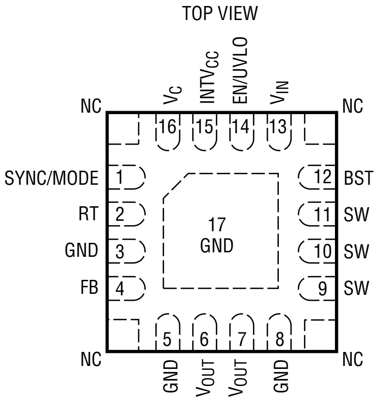
PIN CONFIGURATION

LT8337


TOP VIEW
PG
INTV_CC
EN/UVLO
V_IN
NC
NC
16
15
14
13
SYNC/MODE 1
RT 2
GND 3
FB 4
12 BST
11 SW
10 SW
9 SW
17
GND
5
6
7
8
NC
NC
GND
V_OUT
V_OUT
GND

LQFN PACKAGE
16-LEAD (3mm × 3mm) LQFN
θ_{JA} = 42.8°C/W, θ_{JCtop} = 45.2°C/W,
$\theta_{JCbottom}$ = 8.2°C/W (NOTE 4)
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

LT8337-1


TOP VIEW
V_C
INTV_CC
EN/UVLO
V_IN
NC
NC
16
15
14
13
SYNC/MODE 1
RT 2
GND 3
FB 4
12 BST
11 SW
10 SW
9 SW
17
GND
5
6
7
8
NC
NC
GND
V_OUT
V_OUT
GND

LQFN PACKAGE
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ORDER INFORMATION

PART NUMBER	PART MARKING		PAD FINISH	PACKAGE* TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
	DEVICE	FINISH CODE				
LT8337EV#PBF	LHKR	e4	Au (RoHS)	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 125°C
LT8337JV#PBF						–40°C to 150°C
LT8337EV-1#PBF	LHNW					–40°C to 125°C
LT8337JV-1#PBF						–40°C to 150°C

- Contact the factory for parts specified with wider operating temperature ranges. Pad or ball finish code is per IPC/JEDEC J-STD-609.

*The LT8337/LT8337-1 package has the same dimensions as a standard 3mm × 3mm QFN.

- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

Rev. 0

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $V_{IN} = 5V$, EN/UVLO = 2V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operation Voltage		●	2.7		28	V
V_{IN} Quiescent Current in Shutdown	EN/UVLO = 0.15V EN/UVLO = 0.15V	 ●		0.3 0.3	1 10	µA µA
LT8337 V_{IN} Quiescent Current	SYNC/MODE = 0V, Not Switching			4	8	µA
	SYNC/MODE = Open, Not Switching			0.9	1.5	mA
	$V_{IN} = 10.1V$, $V_{OUT} = 10V$, FB = 1.05V (In PassThru Mode)			15	25	µA
LT8337-1 V_{IN} Quiescent Current	SYNC/MODE = 0V, Not Switching			23	35	µA
	SYNC/MODE = Open, Not Switching			0.9	1.5	mA
	$V_{IN} = 10.1V$, $V_{OUT} = 10V$, FB = 1.05V (In PassThru Mode)			30	60	µA
FB Regulation Voltage	 E-Grade J-Grade	 ● ●	0.994 0.983 0.980	1.000 1.000 1.000	1.006 1.010 1.012	V V V
FB Line Regulation	$2.7V < V_{IN} < 28V$	●		0.005	0.03	%/V
FB Pin Input Current	FB = 1.0V		–20		20	nA
Switching Frequency	$R_T = 357kΩ$ $R_T = 102kΩ$ $R_T = 47.5kΩ$ $R_T = 30.1kΩ$	●	270 0.93 1.85 2.7	300 1 2 3	330 1.07 2.15 3.3	kHz MHz MHz MHz
Spread Spectrum Modulation Frequency as Percentage of f_{SW}				0.45		%
Spread Spectrum Modulation Frequency Range as Percentage of f_{SW}				20		%
Synchronizable Frequency	SYNC/MODE = External Clock	●	0.3		3	MHz
SYNC/MODE Pin Input Logic Level for Frequency Synchronization	SYNC Logic Low SYNC Logic High	● ●	 1.7		0.4 	V V
Soft-Start Time	$R_T = 47.5kΩ$			1.4		ms
EN/UVLO Threshold Voltage	Falling Hysteresis	●	0.94	1.0 90	1.06	V mV
EN/UVLO Input Bias Current	EN/UVLO = 2V		–40		40	nA
LT8337 PG Upper Threshold Offset from Regulated FB	FB Falling Hysteresis	●	5	8 1	12	% %
LT8337 PG Lower Threshold Offset from Regulated FB	FB Rising Hysteresis	●	–12	–8 1	–5	% %
LT8337 PG Leakage Current	PG = 3.5V		–40		40	nA
LT8337 PG Pull-Down Resistance	PG = 0.1V			700	2000	Ω
LT8337-1 Error Amp Transconductance	$V_C = 1.25V$			0.4		mS
LT8337-1 Error Amp Gain				400		V/V
LT8337-1 V_C Source Current	FB = 0.8V, $V_C = 1.25V$			–75		µA
LT8337-1 V_C Sink Current	FB = 1.2V, $V_C = 1.25V$			70		µA
LT8337-1 V_C Pin to Switch Current Gain				6.0		A/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, EN/UVLO = 2V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Bottom Switch On-Resistance	I_{SW} = 1A			32		mΩ
Bottom Switch Current Limit		●	5	6	6.6	A
Bottom Switch Minimum Off-time			20		50	ns
Bottom Switch Minimum On-time	V_{IN} = 9.5V, V_{OUT} = 10V		20		80	ns
Top Switch On-Resistance	I_{SW} = 1A			35		mΩ
SW Leakage Current	V_{OUT} = 28V, SW = 0V, 28V		–1.5		1.5	µA
V_{OUT} Pin Current	SYNC/MODE = 0V, V_{OUT} = 10V, Not Switching			1		µA
	V_{IN} = 10.1V, V_{OUT} = 10V , FB = 1.05V (In PassThru Mode)			30		µA
PassThru Mode V_{IN} to V_{OUT} Threshold (V_{IN} – V_{OUT})	V_{IN} Rising V_{IN} Falling			0 –0.6		V V
PassThru Mode Top Switch Reverse Current Limit	V_{IN} = 9.9V, V_{OUT} = 10V, FB = 1.05V (Top Switch Turns Off)			1.5		A

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8337EV/LT8337EV-1 are guaranteed to meet performance specifications from the 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8337JV/LT8337JV-1 are guaranteed to meet performance specifications over the –40°C to 150°C operating junction temperature ranges. High junction temperatures degrade operating lifetimes; operating lifetime is de-rated for junction temperatures greater than 125°C.

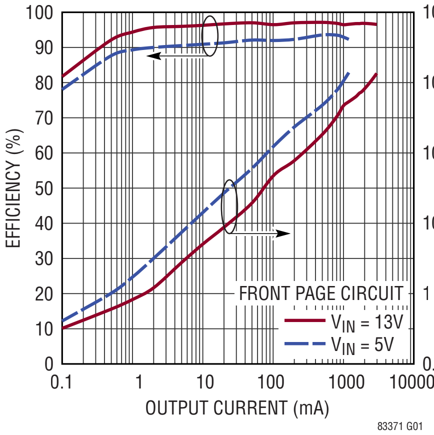
Note 3: These ICs include overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: θ values are determined by simulation per JESD51 conditions.

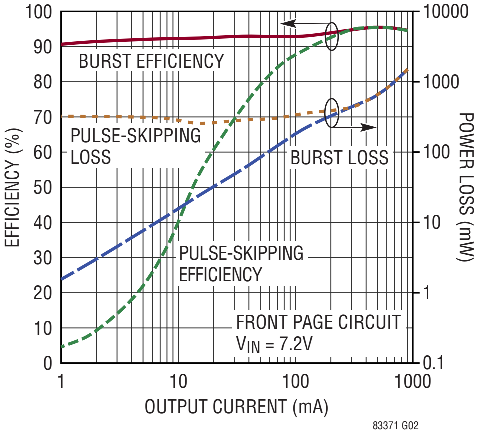
TYPICAL PERFORMANCE CHARACTERISTICS

T_A ≈ T_J = 25°C, unless otherwise noted.

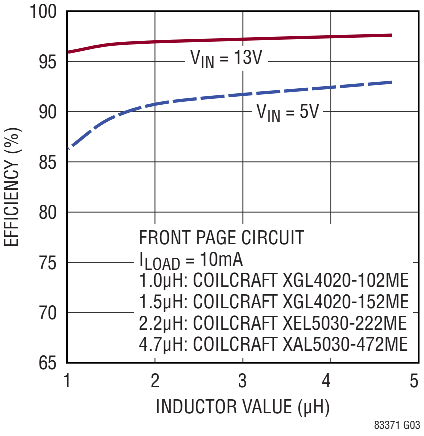
Efficiency and Power Loss vs Output Current



Efficiency and Power Loss vs Output Current



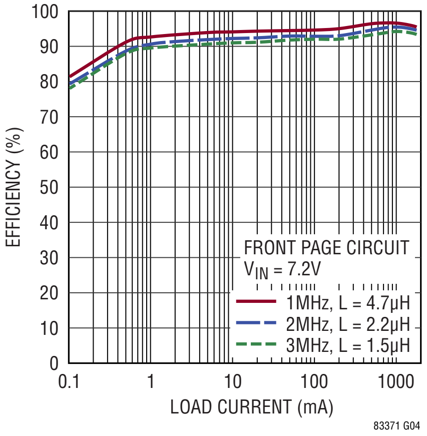
Burst Mode Efficiency vs Inductor Value



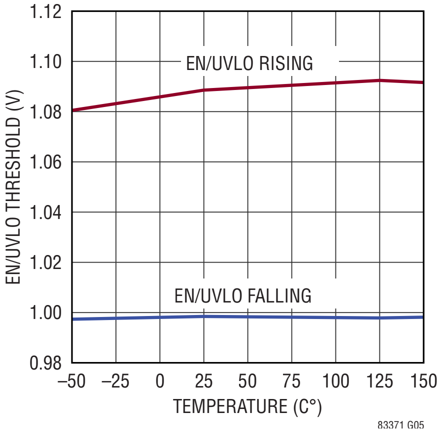
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A \approx T_J = 25°C$, unless otherwise noted.

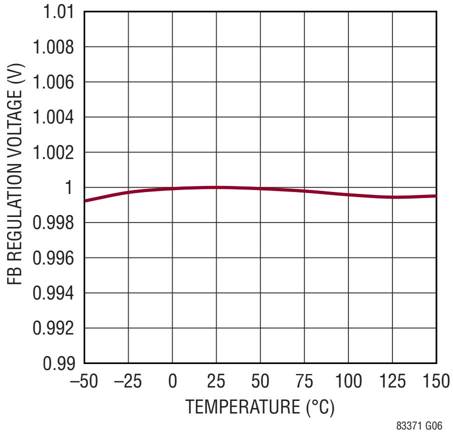
Efficiency vs Output Current at Different Switching Frequencies



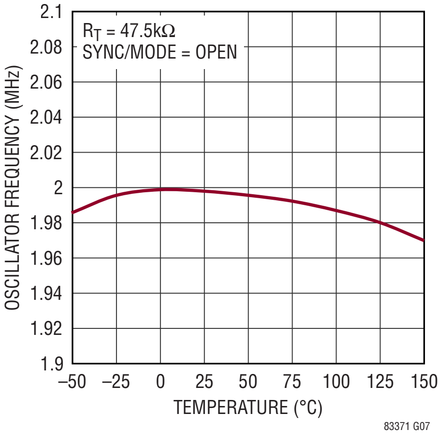
EN/UVLO Thresholds vs Temperature



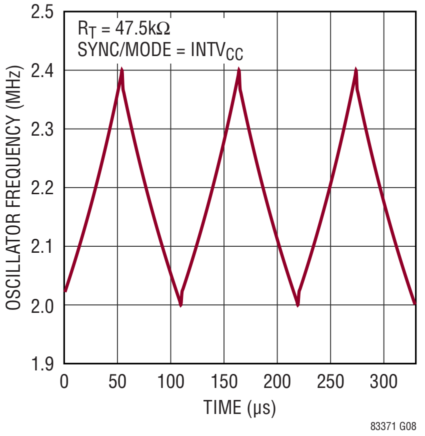
FB Regulation Voltage vs Temperature



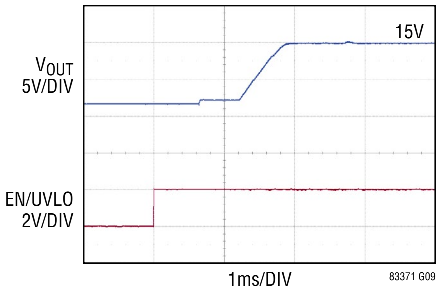
Oscillator Frequency vs Temperature



Oscillator Frequency with Spread Spectrum Modulation

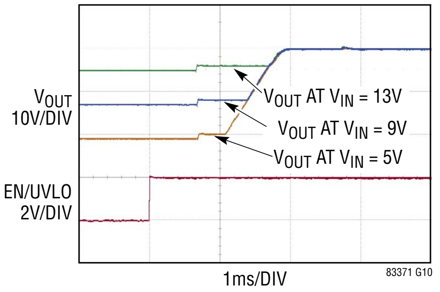


Switching Waveforms, Soft-Start



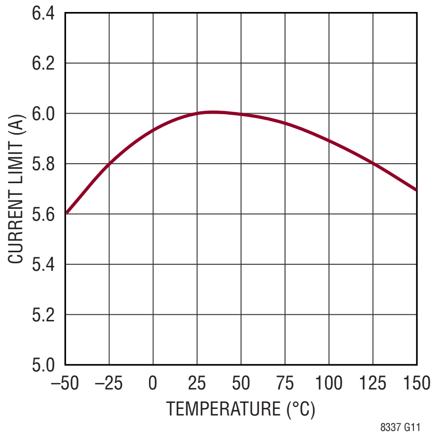
V_{IN} = 7.2V
FRONT PAGE CIRCUIT

Switching Waveforms, Soft-Start at Different V_{IN} Voltages

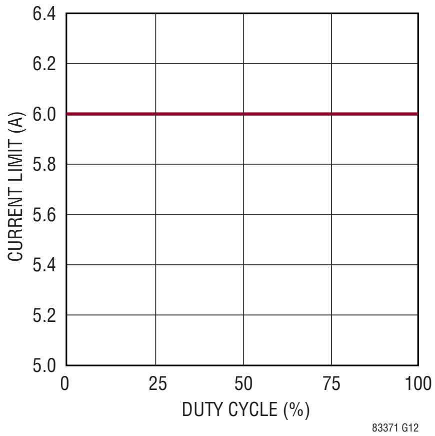


V_{IN} = 13V
FRONT PAGE CIRCUIT

Bottom Switch Current Limit vs Temperature



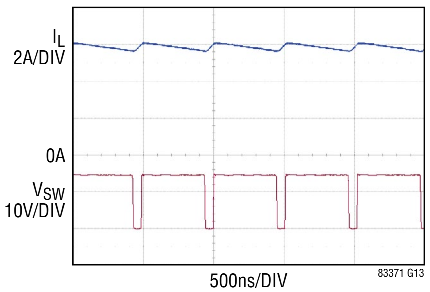
Bottom Switch Current Limit vs Duty Cycle



TYPICAL PERFORMANCE CHARACTERISTICS

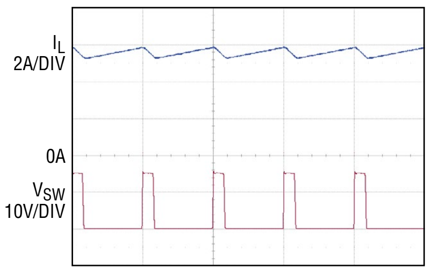
$T_A \approx T_J = 25°C$, unless otherwise noted.

Switching Waveforms, Current Limit at 15% Duty Cycle



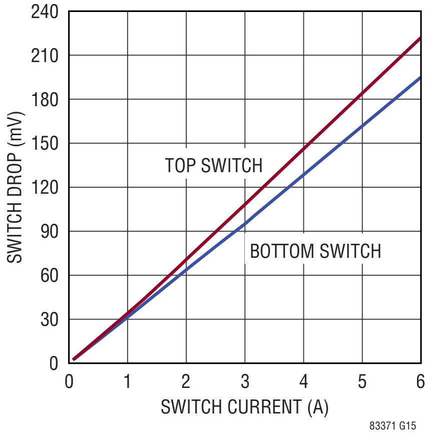
V_{IN} = 13V
FRONT PAGE CIRCUIT

Switching Waveforms, Current Limit at 82% Duty Cycle

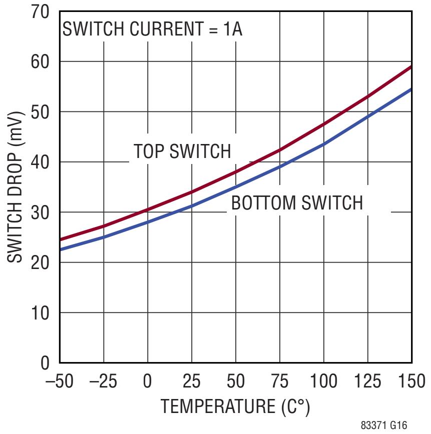


V_{IN} = 2.8V
FRONT PAGE CIRCUIT

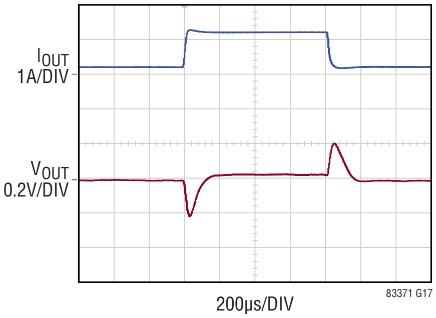
Power Switch Voltage Drop vs Switch Current



Power Switch Voltage Drop vs Temperature

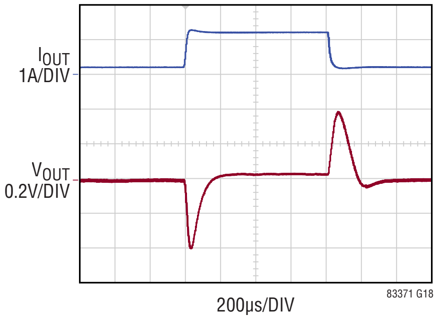


LT8337 Transient Response, Pulse-Skipping Mode Operation



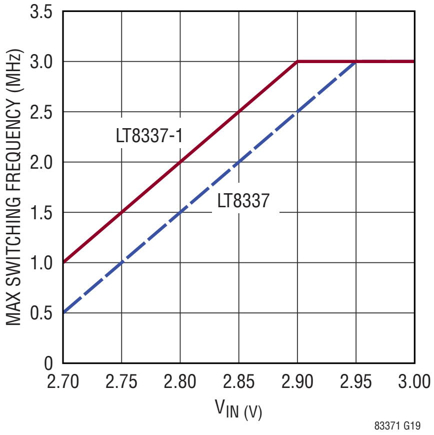
V_{IN} = 7.2V
FRONT PAGE CIRCUIT

LT8337 Transient Response, Burst Mode Operation

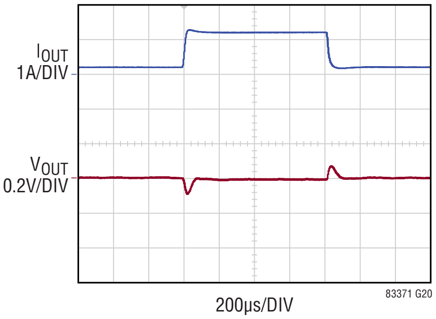


V_{IN} = 7.2V
FRONT PAGE CIRCUIT

Max Programmable Switching Frequency vs Input Voltage

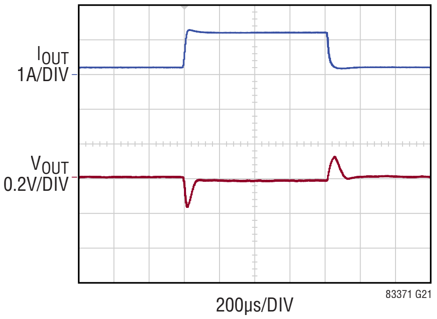


LT8337-1 Transient Response, Pulse-Skipping Mode Operation



V_{IN} = 7.2V
FRONT PAGE CIRCUIT WITH LT8337-1
C_C = 220pF, R_C = 100k

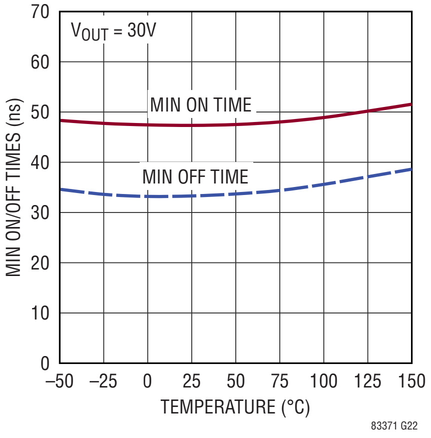
LT8337-1 Transient Response, Burst Mode Operation



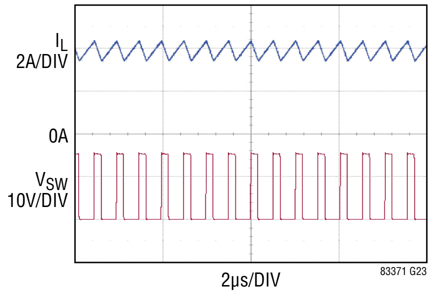
V_{IN} = 7.2V
FRONT PAGE CIRCUIT WITH LT8337-1
C_C = 220pF, R_C = 100k

TYPICAL PERFORMANCE CHARACTERISTICS $T_A \approx T_J = 25°C$, unless otherwise noted.

Minimum On/Off Times vs Temperature

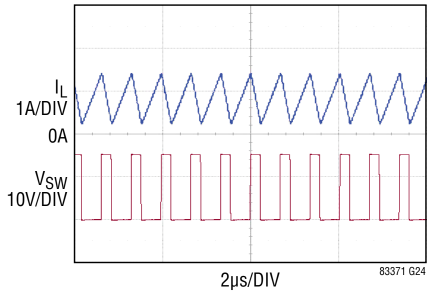


Switching Waveforms, Full Frequency PWM Operation



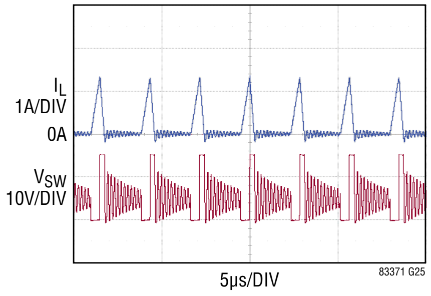
V_{IN} = 5V
I_{LOAD} = 1.2A
FRONT PAGE CIRCUIT

Switching Waveforms, Continuous Burst Mode Operation



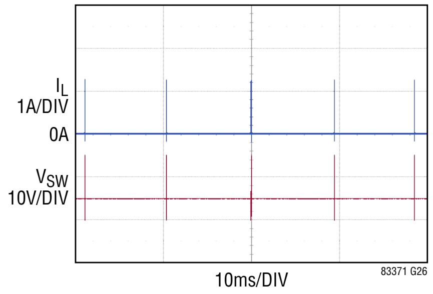
V_{IN} = 5V
I_{LOAD} = 250mA
FRONT PAGE CIRCUIT

Switching Waveforms, Discontinuous Burst Mode Operation



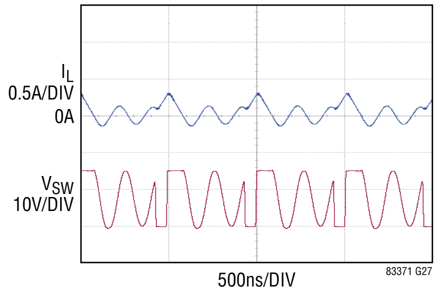
V_{IN} = 5V
I_{LOAD} = 50mA
FRONT PAGE CIRCUIT

Switching Waveforms, Light Load Low I_Q Burst Mode Operation



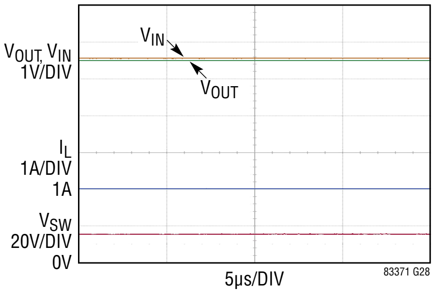
V_{IN} = 5V
I_{LOAD} = 0mA
FRONT PAGE CIRCUIT

Switching Waveforms, Discontinuous Pulse-Skipping Mode



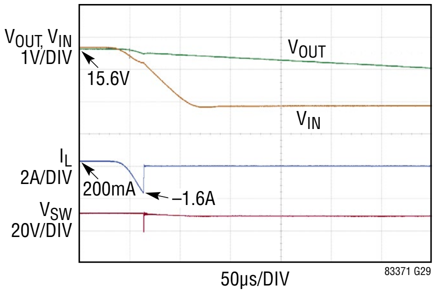
V_{IN} = 7.2V
I_{LOAD} = 10mA
FRONT PAGE CIRCUIT

Waveforms, PassThru Mode Operation



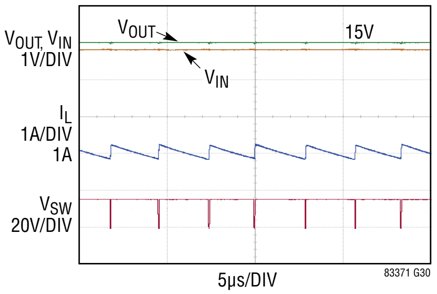
I_{LOAD} = 1A
V_{IN} = 15.5V
FRONT PAGE CIRCUIT

Waveforms, Reverse Current Protection in PassThru Mode



FRONT PAGE CIRCUIT

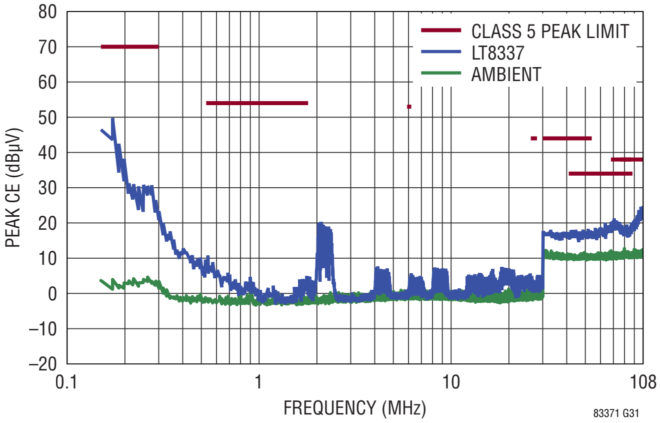
Switching Waveforms, Frequency Foldback when V_{IN} is close to V_{OUT}



I_{LOAD} = 1A
FRONT PAGE CIRCUIT

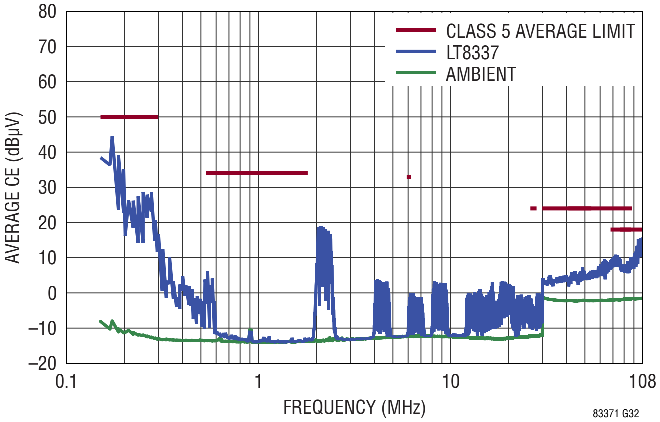
TYPICAL PERFORMANCE CHARACTERISTICS $T_A \approx T_J$ = 25°C, unless otherwise noted.

Conducted EMI Performance (CISPR25 Class 5 Peak)



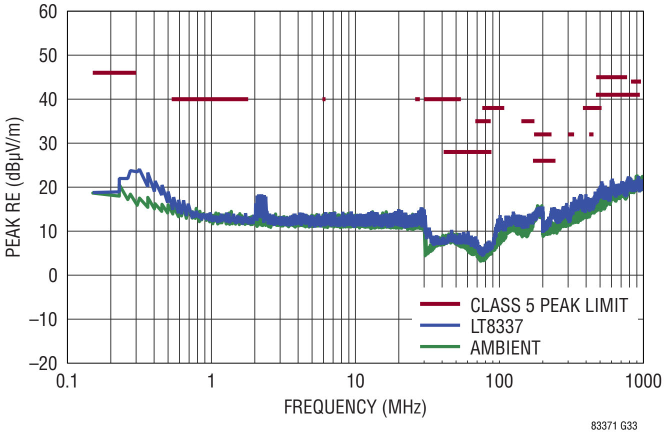
PAGE 20 CIRCUIT,
5V INPUT TO 12V OUTPUT AT 1.5A,
SSFM = ON, f_{SW} = 2MHz TO 2.4MHz

Conducted EMI Performance (CISPR25 Class 5 Average)



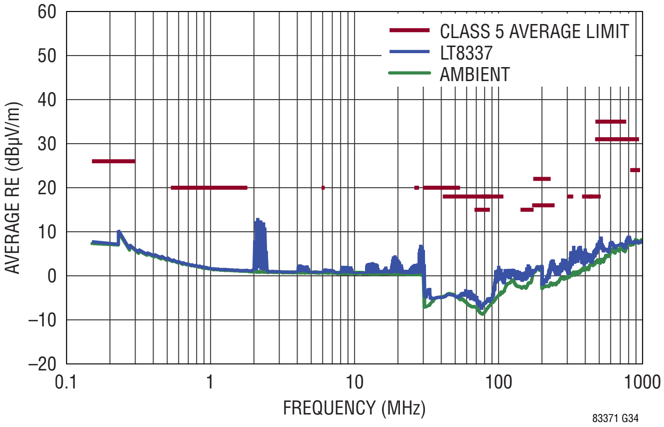
PAGE 20 CIRCUIT,
5V INPUT TO 12V OUTPUT AT 1.5A,
SSFM = ON, f_{SW} = 2MHz TO 2.4MHz

Radiated EMI Performance (CISPR25 Class 5 Peak)



PAGE 20 CIRCUIT,
5V INPUT TO 12V OUTPUT AT 1.5A,
SSFM = ON, f_{SW} = 2MHz TO 2.4MHz

Radiated EMI Performance (CISPR25 Class 5 Average)



PAGE 20 CIRCUIT,
5V INPUT TO 12V OUTPUT AT 1.5A,
SSFM = ON, f_{SW} = 2MHz TO 2.4MHz

PIN FUNCTIONS

SYNC/MODE (Pin 1): External Synchronization Input and Mode Selection Pin. This pin allows five selectable modes for optimization of performance:

SYNC/MODE PIN INPUT	CAPABLE MODE(S) OF OPERATION
(1) GND or <0.1V	Burst
(2) 50k Resistor to GND	Burst/SSFM
(3) Float (Pin Open)	Pulse-Skipping
(4) $INTV_{CC}$ or > ($INTV_{CC}$–0.2V)	Pulse-Skipping/SSFM
(5) External Clock	Pulse-Skipping/Sync

where the selectable modes of operation are:

Burst = low I_Q, (low output ripple operation at light loads)
Pulse-Skipping = skipped pulse(s) at light load (aligned clock)
SSFM = spread spectrum frequency modulation for low EMI
Sync = switching frequency synchronized to external clock.

The LT8337/LT8337-1 automatically selects pulse-skipping mode with no spread spectrum frequency modulation during start-up, and The SYNC/MODE pin input configurations (1) through (4) are ignored.

The LT8337/LT8337-1 automatically select low I_Q operation in the PassThru mode operation, and all the SYNC/MODE pin input configurations are ignored.

RT (Pin 2): Switching Frequency Adjustment Pin. The LT8337/LT8337-1 switching frequency is programmed by connecting a resistor of the appropriate value from the RT pin to GND at Pin 3. See the Applications Information section for more detail. Do not leave the RT pin open.

GND (Pins 3, 5, 8, Exposed Pad Pin 17): Ground. The exposed pad should be soldered to the PCB ground plane for good thermal and electrical performance. See the Applications Information section for sample layout.

FB (Pin 4): Feedback Input Pin. This pin receives the feedback voltage from the external resistor divider between V_{OUT} and Pin 3 GND. FB pin is one input to the error amplifier of the output voltage control loop. See the Applications Information section for sample layout.

V_{OUT} (Pins 6, 7): Output Pins. Connect one 1µF capacitor between V_{OUT} at Pin 6 and GND at Pin 5 only, and a matching 1µF capacitor between V_{OUT} at Pin 7 and GND at Pin 8 only. These two capacitors complete the Silent Switcher configuration and must be placed as close to the IC as possible to achieve lowest EMI. Additional bulk capacitors of 2.2µF or more should be placed close to the IC with the positive terminals connected to V_{OUT}, and negative terminals connected to ground plane. See the Applications Information section for a sample layout.

SW (Pins 9, 10, 11): The SW pins are the outputs of the internal power switches. Tie these pins together and connect them to the inductor and one side of the boost capacitor C_{BST}.

BST (Pin 12): Top Switch Gate Driver Supply Pin. Place a 0.1µF capacitor (C_{BST}) between the BST and SW pins and close to the IC.

V_{IN} (Pin 13): Input Supply Pin. This pin must be connected to the input of the power stage (the inductor's input terminal).

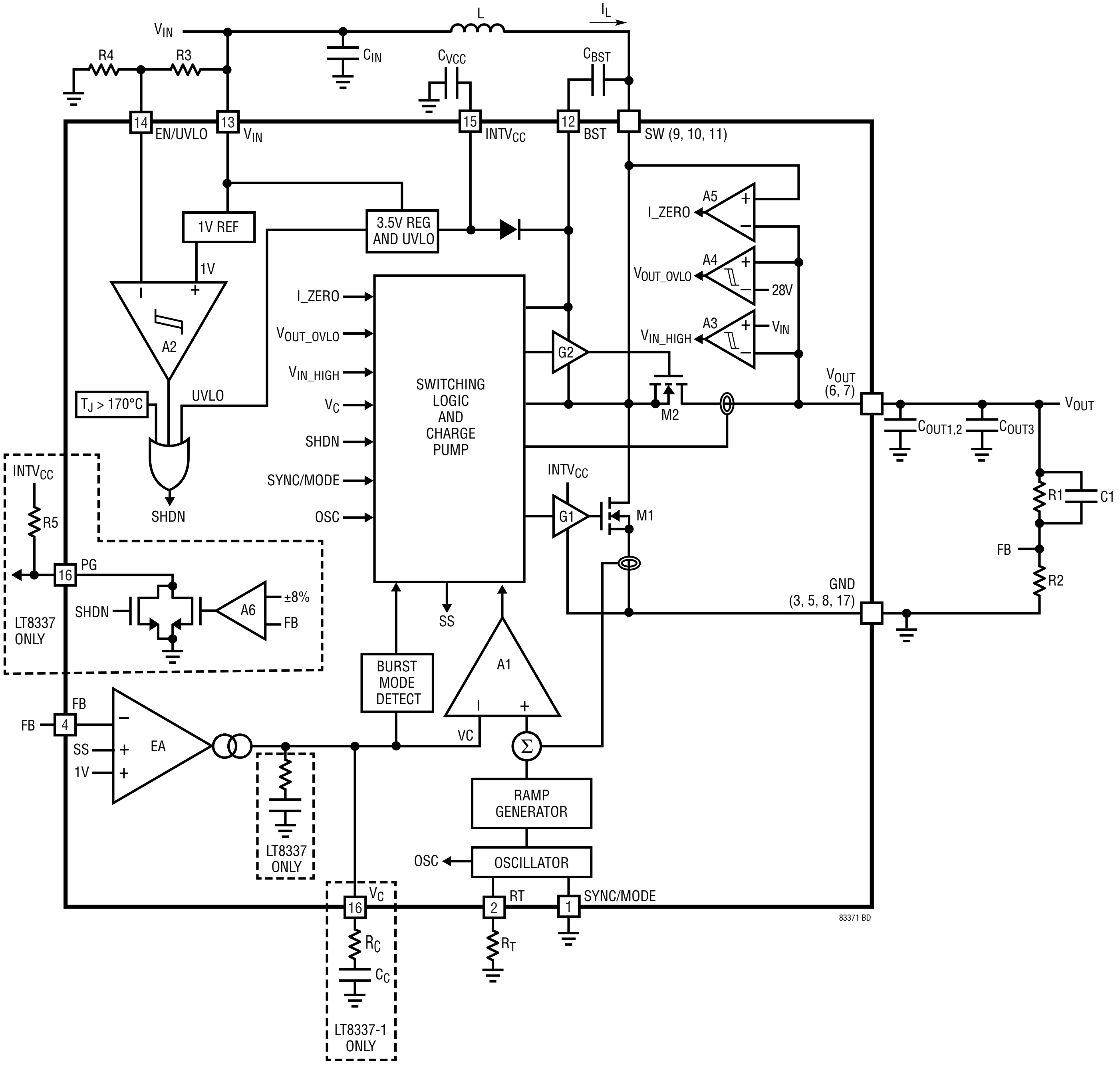
EN/UVLO (Pin 14): Enable and Input Undervoltage Lockout Pin. The IC is shut down when this pin is below 1V (typical). The IC draws a low V_{IN} current of 0.3µA (typical) when this pin is below 0.15V. The IC is enabled when this pin is above 1.0V (typical). A resistor divider from V_{IN} to GND can be used to program a V_{IN} threshold below which the IC is shut down. See the Applications Information section for further details. Tie EN/UVLO to V_{IN} if the shutdown feature is not used.

$INTV_{CC}$ (Pin 15): Internal 3.5V Regulator Bypass Pin. This pin provides supply for internal drivers and control circuits. The bypass capacitor for $INTV_{CC}$ should be connected to the ground plane. Do not load the $INTV_{CC}$ pin with external circuitry. This pin must be bypassed with a 1µF or larger low ESR ceramic capacitor placed close to the pin.

PG (Pin 16, LT8337 Only): Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is greater than ±8% outside the regulated voltage. PG is also pulled to ground when EN/UVLO is below 1V, $INTV_{CC}$ has fallen too low, or the IC enters thermal shutdown.

V_C (Pin 16, LT8337-1 Only): Error Amplifier Output and Switch Regulator Compensation Pin. Connect this pin to appropriate external RC network to compensate the regulator loop frequency response.

BLOCK DIAGRAM


VIN
L
IL
R4
R3
CIN
CVCC
CBST
14 EN/UVLO
13 VIN
15 INTVCC
12 BST
SW (9, 10, 11)
1V REF
3.5V REG AND UVLO
1V
A2
TJ > 170°C
UVLO
SHDN
A5
I_ZERO
A4
VOUT_OVLO
28V
A3
VIN_HIGH
VIN
I_ZERO
VOUT_OVLO
VIN_HIGH
VC
SHDN
SYNC/MODE
OSC
SWITCHING LOGIC AND CHARGE PUMP
G2
M2
VOUT (6, 7)
VOUT
COUT1,2
COUT3
R1
C1
FB
R2
INTVCC
G1
M1
GND (3, 5, 8, 17)
INTVCC
R5
16 PG
SHDN
A6
±8%
FB
LT8337 ONLY
BURST MODE DETECT
SS
A1
VC
Σ
FB
4 FB
SS
1V
EA
LT8337 ONLY
RAMP GENERATOR
OSC
OSCILLATOR
16 VC
2 RT
1 SYNC/MODE
RC
CC
RT
LT8337-1 ONLY
83371 BD

OPERATION

The LT8337/LT8337-1 uses a fixed frequency, current mode control scheme to provide excellent line and load regulation. Referring to the Block Diagram, the Switching Logic and Charge Pump block turns on the power switch M1 through driver G1 at the start of each oscillator cycle. During the M1 switch on-phase, the inductor current I_L flows through M1. A current proportional to the M1 switch current is added to a stabilizing slope compensation ramp and the resulting sum is fed into the positive terminal of the PWM comparator A1. The voltage at the negative input of A1, labeled "V_C", is set by the error amplifier EA and is an amplified version of the difference between the feedback voltage FB and the reference voltage. During the M1 on-phase, I_L increases. When the signal at the positive input of A1 exceeds V_C, A1 sends out a signal to the Switching Logic and Charge Pump block to turn off M1. When M1 turns off, the synchronous power switch M2 turns on until the next clock cycle begins or inductor current I_L falls to zero. During the M1 off-phase, I_L decreases. Through this repetitive action, the EA sets the correct I_L peak current level to keep the output in regulation. V_{IN} and V_{OUT} are constantly monitored by the IC. When V_{IN} rises above V_{OUT} (causing A3's output high) and at the same time V_{OUT} is higher than its regulation voltage programmed by the FB resistor network, the IC enters PassThru operation, where M2 is kept on continuously and M1 is kept off continuously, and the V_{OUT} is essentially shorted to V_{IN} by the inductor and M2. See Applications Information section for further details.

The IC features Silent Switcher architecture to minimize EMI emissions while delivering high efficiency. The Silent Switcher EMI cancellation loops are completed by placing one 1µF capacitor between V_{OUT} at pin 6 and GND at pin 5 and a matching 1µF capacitor between V_{OUT} at pin 7 and GND at pin 8 (see Applications Information section for further details).

The EN/UVLO pin controls whether the IC is enabled or is in shutdown state. A 1.0V reference and a comparator A2 with 90mV hysteresis (Block Diagram) allow the user to accurately program the supply voltage at which the IC turns on and off. See the Applications Information section for further details.

The LT8337/LT8337-1 features a variety of operation modes which can be selected by SYNC/MODE pin to optimize the converter performance based on the application requirements. The low ripple Burst Mode operation can be selected to optimize the efficiency at light loads. The spread spectrum frequency modulation function can be selected to minimize the EMI emissions.

Pulling SYNC/MODE pin to ground selects Burst Mode operation. Connecting this SYNC/MODE to ground through a 50k resistor selects Burst Mode operation with spread spectrum frequency modulation. Floating SYNC/MODE pin selects pulse-skipping operation. Connecting SYNC/MODE pin to $INTV_{CC}$ selects pulse-skipping operation with spread spectrum frequency modulation. If a clock is applied to the SYNC/MODE pin, the IC synchronizes to an external clock frequency and operates in pulse-skipping mode. See the Applications Information section for further details.

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Programming V_{IN} Turn-On and Turn-Off Thresholds with the EN/UVLO Pin

The falling threshold voltage and rising hysteresis voltage of the EN/UVLO pin can be calculated by Equation 1.

$$V_{VIN,FALLING} = 1.0V \bullet \frac{(R3 + R4)}{R4}$$
$$V_{VIN,RISING} = 90mV \bullet \frac{(R3 + R4)}{R4} + V_{VIN,FALLING} \tag{1}$$

When in Burst Mode operation with light load currents, the current through the resistor network R3 and R4 can easily be greater than the supply current consumed by the IC. Therefore, large resistors can be used for R3 and R4 to minimize their effect on efficiency at light loads.

EN/UVLO pin can be tied to V_{IN} if the shutdown feature is not used, or alternatively, the pin may be tied to a logic level if shutdown control is required. The IC draws a low V_{IN} quiescent current of 0.3μA (typical) When EN/UVLO is below 0.15V.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 3.5V supply from V_{IN} that powers the drivers and the internal bias circuitry. The $INTV_{CC}$ pin must be bypassed to ground with a minimum of 1μF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. Applications with high V_{IN} voltage and high switching frequency increase die temperature because of the higher power dissipation across the LDO. When V_{IN} is lower than 2.95V for LT8337 or 2.90V for LT8337-1, the maximum programmable switching frequency is lower due to the voltage drop across the LDO. See the Max Programmable Switching Frequency vs Input Voltage curve in the Typical Performance Characteristics section for more information. Do not connect an external load to the $INTV_{CC}$ pin.

Light Load Current Operation—Burst Mode Operation or Pulse-Skipping

To enhance the efficiency at light loads, the LT8337/LT8337-1 features operate in low ripple Burst Mode operation. When the IC is enabled for Burst Mode operation, the minimum peak inductor current is set to approximately 1.2A even though the V_C node Block Diagram) indicates a lower value. In this condition, the IC maintains the output regulation voltage by reducing the switching frequency instead of reducing the inductor peak current. In light load Burst Mode operation the IC delivers single pulses of current to the output capacitor followed by sleep periods during which the output power is supplied by the output capacitor. This low ripple Burst Mode operation minimizes the input quiescent current and minimizes output voltage ripple.

As the output load decreases, the frequency of single current pulses decreases and the percentage of time the IC is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. By maximizing the time between pulses, the converter V_{IN} pin quiescent current approaches 4μA (LT8337) or 23μA (LT8337-1) for a typical application when there is no output load. To optimize the quiescent current performance at light loads, the current in the feedback resistor divider should be minimized as it appears to the output as load current.

In order to achieve higher light load efficiency, more energy should be delivered to the output during the single small pulses in Burst Mode operation such that the IC can stay in sleep mode longer between each pulse. This can be achieved by using a larger value inductor. For example, while a smaller inductor value would typically be used for a high switching frequency application, if high light load efficiency is desired, a larger inductor value should be chosen. See the Burst Mode Efficiency vs Inductor Value curve in the Typical Performance Characteristics section for more information.

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While in Burst Mode operation the bottom switch peak current is approximately 1.2A as shown in the Switching Waveforms in Burst Mode operation curve in the Typical Performance Characteristics section. This behavior results in larger output voltage ripple compared to that in pulse-skipping mode operation which has lower bottom switch peak current. However, the output voltage ripple can be reduced proportionally by increasing the output capacitance. When adjusting output capacitance, a careful evaluation of system stability should be made to ensure adequate design margin. As the load ramps upward from zero, the switching frequency keeps increasing until reaching the switching frequency programmed by the resistor at the RT pin. The output load at which the LT8337/LT8337-1 reaches the programmed frequency varies based on input voltage, output voltage, and inductor choice.

Pulse-skipping mode operation offers two major differences from Burst Mode operation. First, the internal clock stays awake at all times and all switching cycles are aligned to the clock. In this mode the internal circuitry is awake at all times, increasing quiescent current to several hundred µA compared to the 5µA of V_{IN} pin quiescent current in Burst Mode operation. Second, as the load ramps upward from zero, the switching frequency programmed by the resistor at the RT pin is reached at a lower output load than in Burst Mode operation, therefore, pulse-skipping mode operation exhibits lower output ripple as well as lower audio noise and RF interference.

Switching Frequency and Synchronization

The choice of switching frequency is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing the power switches' switching losses and gate drive current. However, lower frequency operation requires a physically larger inductor. The LT8337/LT8337-1 uses a constant-frequency architecture that can be programmed over a 300kHz to 3MHz range with a single external resistor from the RT pin to ground, as shown in Block Diagram. A table for selecting the value of R_T for a given switching frequency is shown in Table 1. Figure 1 shows the R_T Value vs Switching Frequency curve.

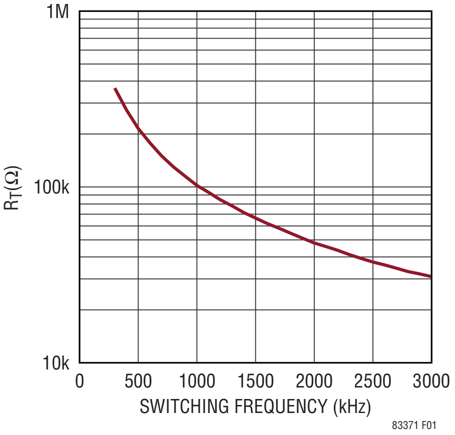

Figure 1. R_T Value vs Switching Frequency

Table 1. SW Frequency (f_{SW}) vs R_T Value

f_{SW} (MHz)	R_T (kΩ)	f_{SW} (MHz)	R_T (kΩ)
0.3	357	1.7	57.6
0.4	267	1.8	53.6
0.5	210	1.9	51.1
0.6	174	2.0*	47.5
0.7	147	2.1	45.2
0.8	127	2.2	43.2
0.9	113	2.3	40.2
1.0	102	2.4	39.2
1.1	90.9	2.5	37.4
1.2	84.5	2.6	35.7
1.3	76.8	2.7	34.0
1.4	71.5	2.8	32.4
1.5	64.9	2.9	30.9
1.6	61.9	3.0	30.1

* Programming 2MHz will ensure f_{SW} stays above 1.85MHz (out of the AM band).

The operating frequency of the LT8337/LT8337-1 can be synchronized to an external clock source with 100ns minimum pulse width. By providing a digital clock signal to the SYNC/MODE pin, the IC operates at the SYNC pulse frequency and automatically enters pulse-skipping mode operation at light load. If this feature is used, an RT resistor should be chosen to program a switching frequency as close as possible to the SYNC pulse frequency.

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Spread Spectrum Frequency Modulation

The LT8337/LT8337-1 features spread spectrum frequency modulation to further reduce EMI emissions. The user can select spread spectrum frequency modulation with Burst Mode operation by connecting the SYNC/MODE pin to ground through a 50k resistor, or spread spectrum frequency modulation with pulse-skipping operation by connecting the SYNC/MODE pin to $INTV_{CC}$. When spectrum frequency modulation is selected, a stepped triangular frequency modulation is used to vary the internal oscillator frequency between the value programmed by the RT resistor to approximately 20% higher than that value. The modulation frequency is approximately 0.45% of the switching frequency. For example, when the IC is programmed to 2MHz, and spread spectrum frequency modulation is selected, the oscillator frequency varies from 2MHz to 2.4MHz at a 9kHz rate (see Oscillator Frequency with Spread Spectrum Modulation curve in the Typical Performance Characteristics section). When operating at light load, the spread spectrum frequency modulation is more effective in pulse-skipping mode than in Burst Mode operation, due to the fact that pulse-skipping operation maintains the programmed switching frequency down to a much lower load current as compared to Burst Mode operation.

V_{IN} to V_{OUT} PassThru Mode Operation

In the boost pre-regulator applications for automotive stop-start and cold crank, V_{IN} is normally above the regulated V_{OUT} voltage. In this condition, LT8337/LT8337-1 enters PassThru operation. LT8337/LT8337-1 is designed to have an accurate, well controlled PassThru operation with low quiescent current consumption. If V_{IN} transiently falls below the V_{OUT} regulation setpoint, the boost converter commences switching to maintain the output voltage in regulation.

As shown in Block Diagram, V_{IN} is compared with V_{OUT} using the comparator A3 with 0.6V hysteresis. When V_{IN} rises above V_{OUT} (causing A3's output high), and at the same time V_{OUT} is higher than its regulation voltage programmed by the FB resistor network, the IC boost converter enters PassThru operation, where the synchronous power switch M2 is kept on continuously and the power switch M1 is kept off continuously. The voltage across the boost capacitor (C_{BST}), V_{BST_SW}, is constantly monitored. When V_{BST_SW} drops below 3.2V, an internal charge pump is turned on to charge V_{BST_SW} up to 3.6V, and then turned off. In PassThru mode the V_{OUT} is essentially shorted to V_{IN} by the inductor and M2, and V_{IN} pin quiescent current is limited to 15µA (LT8337) or 30µA (LT8337-1) regardless of the SYNC/MODE pin's configuration. V_{OUT} pin draws 30µA (typ). A typical waveforms drawing is shown in the Typical Performance Characteristics section.

Several conditions cause the IC to exit from the PassThru mode operation. First, when V_{OUT} drops below its regulation voltage programmed by the FB resistor network, the IC exits from PassThru mode operation and normal boost switching operation resumes to maintain the regulated V_{OUT} voltage. Second, when V_{OUT} is still higher than its regulation voltage but V_{IN} drops below V_{OUT} by the comparator A3's hysteresis of 0.6V (typ) or more to cause A3's output low, M2 is turned off to prevent the reverse current from V_{OUT} to V_{IN} from ramping up. IC is back to the PassThru mode when A3's output is high again. Third, when V_{OUT} is still higher than its regulation voltage but M2's reverse current (flowing from its drain to source) rises above 1.5A (typ), M2 is turned off to prevent the reverse current from V_{OUT} to V_{IN} from ramping up. The IC re-enters the PassThru mode when A3's output is high again. Waveforms for typical reverse current protection are shown in the Typical Performance Characteristics section.

To ensure the PassThru mode operation works properly, the IC's V_{IN} pin must be connect to the input of the power stage (the input terminal of inductor as shown in Block Diagram).

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FB Resistor Network and the Quiescent Current at No Load

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to Equation 2.

$$R1 = R2 \bullet \left(\frac{V_{OUT}}{1V} - 1\right) \quad (2)$$

Reference designators refer to Block Diagram. The 1% resistors are recommended to maintain output voltage accuracy.

If low input quiescent current and good light-load efficiency are desired, use large resistor values for the FB resistor divider. The current flowing in the divider acts as a load current, and will increase the no load input current to the converter.

When $V_{IN} < V_{OUT}$, the LT8337 converter Burst Mode quiescent current at no load can be estimated using Equation 3, and the LT8337-1 converter Burst Mode quiescent current at no load can be estimated using Equation 4.

$$I_Q \approx 4\mu A + \left(\frac{V_{OUT}}{R1 + R2} + 1\mu A\right) \bullet \left(\frac{V_{OUT}}{V_{IN}}\right) \bullet 1.2 \quad (3)$$

$$I_Q \approx 23\mu A + \left(\frac{V_{OUT}}{R1 + R2} + 1\mu A\right) \bullet \left(\frac{V_{OUT}}{V_{IN}}\right) \bullet 1.4 \quad (4)$$

where 4µA and 23µA are the V_{IN} pin quiescent current of the LT8337 and LT8337-1 respectively, and the second term is the current drawn by the feedback divider and V_{OUT} pin (1µA) reflected to the input of the boost operating.

For a 12V input, 24V output boost converter with R1 = 1M and R2 = 43.2k, it can be calculated that the LT8337 converter draws approximately 60µA from the supply at no load, and the LT8337-1 converter draws approximately 90µA from the supply at no load. Note that Equation 3 and Equation 4 imply that the no load current is a function of V_{IN}.

When V_{IN} is higher than the regulated V_{OUT} voltage, the IC enters PassThru operation and V_{OUT} is essentially shorted to V_{IN} by the inductor and M2. The converter quiescent current at no load can be estimated using Equation 5 for LT8337 and Equation 6 for LT8337-1.

$$I_Q \approx 45\mu A + \frac{V_{IN}}{R1 + R2} \quad (5)$$

$$I_Q \approx 60\mu A + \frac{V_{IN}}{R1 + R2} \quad (6)$$

where 45µA and 60µA are is the sum of the V_{IN} pin and V_{OUT} pin quiescent current of the LT8337 and LT8337-1 respectively, and the second term is the current drawn by the feedback divider.

When using large FB resistors, a 4.7pF to 22pF phase-lead capacitor should be connected from V_{OUT} to FB, and a careful evaluation of system stability should be made to ensure adequate design margin.

Overvoltage Lockout

The V_{OUT} pin voltage is constantly monitored by the LT8337/LT8337-1. An overvoltage condition occurs when V_{OUT} pin voltage exceeds approximately 28V. Switching is stopped at such condition. Normal switching is resumed when the V_{OUT} pin voltage drops back to 28V or lower.

Switching Frequency Foldback when V_{IN} Approaches V_{OUT}

In some applications, V_{IN} may rise to a voltage very close to V_{OUT}. In this condition the switching regulator must operate at a very low duty cycles to keep V_{OUT} in regulation. However, the minimum on-time limitation may prevent the switcher from attaining a sufficiently low duty cycle at the programmed switching frequency. As a result a typical boost converter may experience a large output ripple under these conditions. The LT8337/LT8337-1 addresses this issue by adopting a switching frequency foldback function to smoothly decrease the switching frequency when its minimum on-time starts to limit the

APPLICATIONS INFORMATION

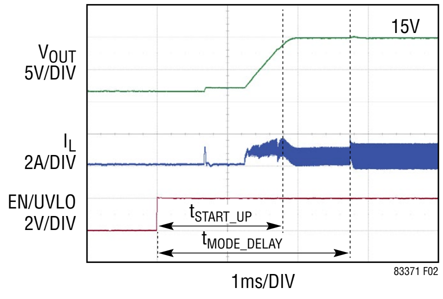
switcher from attaining a sufficiently low duty cycle. The typical switching waveforms in these V_{IN} approaching V_{OUT} conditions are shown in the Typical Performance Characteristics section.

Start-Up

To limit the peak switch current and V_{OUT} overshoot during start-up, the LT8337/LT8337-1 contains internal circuitry to provide soft-start operation (refer to the error amplifier EA in Block Diagram). During start-up, the internal soft-start circuity slowly ramps the internal SS signal from zero to 1V. When the SS voltage falls between the FB initial voltage and 1V, the IC regulates the FB pin voltage to the SS voltage instead of 1V. In this way the output capacitor is charged gradually towards its final value while limiting the start-up peak switch currents.

Referring to Figure 2, the start-up time T_{START_UP} is the time period from EN/UVLO transitioning high to V_{OUT} having reached 90% of its regulation voltage programmed by FB resistor network. When V_{IN} > 3.6V, T_{START_UP} is approximately given by Equation 7.

$$T_{START\_UP} = 0.25\text{ms} + \frac{2100}{f_{SW}} \qquad (7)$$



V_{IN} = 7.2V
FRONT PAGE CIRCUIT

Figure 2. Typical Start-Up Waveforms

When V_{IN} < 3.6V, T_{START_UP} is approximately given by Equation 8.

$$T_{START\_UP} = 0.25\text{ms} + \frac{3.5\text{V}}{V_{IN} - 0.1\text{V}} \bullet \frac{2100}{f_{SW}} \qquad (8)$$

The IC selects pulse-skipping mode with no spread spectrum frequency modulation during start-up, and the SYNC/MODE pin configuration is ignored. The IC reads SYNC/MODE pin configuration after the start-up delay (Equation 9).

$$T_{MODE\_DELAY} = 0.22\text{ms} + \frac{4096}{f_{SW}} \qquad (9)$$

If the LT8337/LT8337-1 boost converter is plugged into a live supply, the V_{OUT} could ring to twice the voltage of V_{IN}, due to the resonant circuit composed by L, C_{OUT1-3}, and the body diode of M2 (refer to Block Diagram). If such over-shoot exceeds the V_{OUT} rating, it must be limited to protect the load and the converter. For these situations, a small Schottky diode or silicon diode can be connected between V_{IN} and V_{OUT} to deactivate the resonant circuit and limit the V_{OUT} over-shoot as shown in Figure 3. With the diode connected, the boost is also more robust against output fault conditions such as output short circuit or overload, due to the fact that the diode diverts a great amount of output current from the IC. The diode can be rated for about one half to one fifth of the full load current since it only conducts current during start-up or output fault conditions.

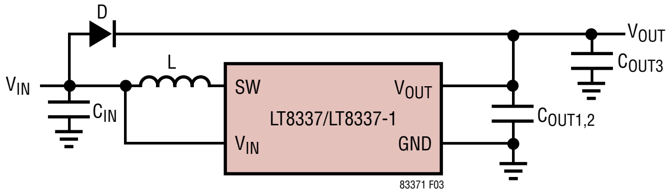


Figure 3. A Simplified LT8337/LT8337-1 Power Stage with a Diode Added Between V_{IN} and V_{OUT}

Inductor Selection

When operating in continuous conduction mode (CCM), the duty cycle can be calculated based on the output voltage (V_{OUT}) and the input voltage (V_{IN}). The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage (Equation 10).

$$D_{MAX} = \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}} \qquad (10)$$

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Discontinuous conduction mode (DCM) provides higher conversion ratios at a given frequency at the cost of reduced efficiencies and higher switching currents.

The inductor ripple current ΔI_{SW} has a direct effect on the choice of the inductor value, the converter's maximum output current capability, and the light load efficiency in Burst Mode operation. Choosing smaller values of ΔI_{SW} increases output current capability and light load efficiency in Burst Mode operation, but require large inductance values and reduce the current loop gain. Accepting larger values of ΔI_{SW} provides fast transient response and allows the use of low inductance values, but results in higher input current ripple, greater core losses, lower light load efficiency in Burst Mode operation, and lower output current capability. Large values of ΔI_{SW} at high duty cycle operation may result in sub-harmonic oscillation. ΔI_{SW} = 1.2A to 2.4A generally provides a good starting value for many applications, and careful evaluation of system stability should be made to ensure adequate design margin.

Given an operating input voltage range, and having chosen the operating frequency and ripple current in the inductor, the inductor value of the boost converter can be determined using Equation 11.

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \bullet f_{SW}} \bullet D_{MAX} \qquad (11)$$

The peak inductor current is equal to the LT8337/LT8337-1 bottom switch current limit as given in the Electrical Characteristics table. The user should choose an inductor with sufficient saturation and RMS current ratings to handle the inductor's peak current.

Input Capacitor Selection

The input ripple current in a boost converter is relatively low (compared with the output ripple current), because this current is continuous. The voltage rating of the input capacitor, C_{IN}, should comfortably exceed the maximum input voltage. Although ceramic capacitors can be relatively tolerant of overvoltage conditions, aluminum electrolytic capacitors are not. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

The value of C_{IN} is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance.

The RMS C_{IN} ripple current can be estimated by Equation 12.

$$I_{RMS(CIN)} = 0.3 \bullet \Delta I_L \qquad (12)$$

Output Capacitor Selection

The output capacitor has two essential functions. First, it filters the LT8337/LT8337-1's discontinuous top switch current to produce the DC output. In this role, it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the IC's control loop. The X5R or X7R type ceramic capacitors have very low equivalent series resistance (ESR), which provides low output ripple and good transient response. Transient performance can be improved with higher output capacitance and the addition of a feedforward capacitor placed between V_{OUT} and FB. When a feedforward capacitor is used or output capacitance is adjusted, a careful evaluation of system stability should be made to ensure adequate design margin. Increasing the output capacitance will also decrease the output voltage ripple. Lower value of output capacitance can be used to save space and cost, but transient performance will suffer and loop instability may result.

Besides the bulk output capacitors, two small output ceramic capacitors, 1µF each, should be placed as close as possible to the IC to complete the Silent Switcher cancellation loops.

See the Board Layout section for more detail. XR7 or X5R capacitors are recommended for best performance across temperature and output voltage variations. Note that larger output capacitance is required when a lower switching frequency is used. If there is significant inductance to the load due to long wires or cables, additional

APPLICATIONS INFORMATION

bulk capacitance may be necessary. This can be provided with an electrolytic capacitor. When choosing a capacitor, special attention should be given to capacitor's data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor, or one with a higher voltage rating, may be required. For good starting values, refer to the Typical Applications section.

Output Power Good (LT8337 Only)

When the LT8337's FB voltage is within the ±8% window of the regulation point, the output voltage is considered good and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal pull-down device will pull the PG pin low. To prevent glitching both the upper and lower thresholds include 1% of hysteresis. The PG pin is also actively pulled low during several fault conditions: corresponding EN/UV pin below 1V, $INTV_{CC}$ voltage falling too low, V_{IN} under voltage, or thermal shutdown.

Frequency Compensation (LT8337-1 Only)

The LT8337-1 has a V_C pin which can be used to optimize the loop compensation. Designing the compensation network is a bit complicated and the best values depend on the application and in particular the type of output capacitor. A practical approach is to start with one of the circuits in the data sheet that is similar to your application and tune the compensation network to optimize the performance. LTspice® simulations can help in this process. Stability should then be checked across all operating conditions, including load current, input voltage, and temperature.

Figure 4 shows an equivalent circuit for the LT8337-1 control loop. The error amplifier is a transconductance amplifier with finite output impedance. The power section, consisting of the modulator, power switches, and inductor, is modeled as a transconductance amplifier generating an output current proportional to the voltage at the V_C pin. Note that the output capacitor integrates this current and that the capacitor on the V_C pin (C_C) integrates the error amplifier output current, resulting in two poles in the loop.

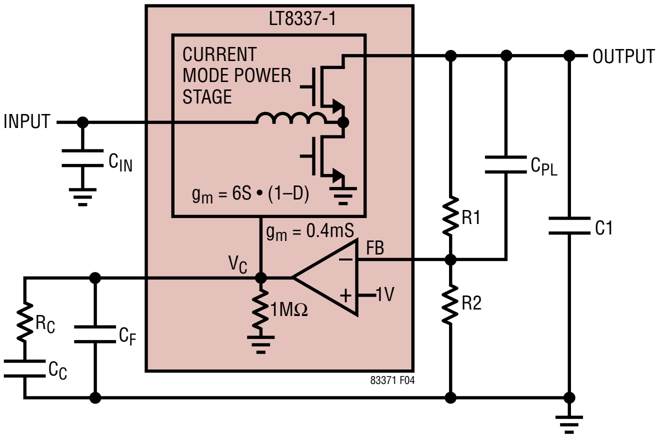


Figure 4. Mode for Loop Response

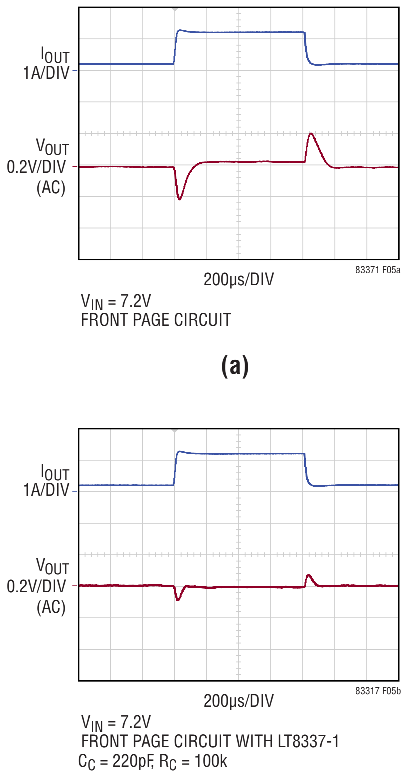
A zero is required and comes from a resistor R_C in series with C_C. This simple model works well as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency.

A small capacitor C_F can be added to filter the switching noise that is coupled on the V_C pin. A phase lead capacitor (CPL) across the feedback divider can be used to improve the transient response and is required to cancel the parasitic pole caused by the feedback node to ground capacitance.

Figure 5a shows the transient response for the front page application with LT8337 which uses internal compensation.

Figure 5b shows a faster transient response of the same application with LT8337-1 when a 100k R_C and 220pF C_C compensation network is used on its V_C pin. The LT8337-1 V_{IN} pin draws 20µA more quiescent current compared to LT8337.

APPLICATIONS INFORMATION



V_{IN} = 7.2V
FRONT PAGE CIRCUIT

(a)

V_{IN} = 7.2V
FRONT PAGE CIRCUIT WITH LT8337-1
C_C = 220pF, R_C = 100k

(b)

Figure 5. Transient Response

Board Layout

The LT8337/LT8337-1 is specifically designed to minimize EMI/EMC emissions and also to maximize efficiency when switching at high frequencies. Figure 6 shows a recommended PCB layout for LT8337. For more detail and PCB design files refer to the demo board guide for the LT8337/LT8337-1.

For optimal performance the LT8337/LT8337-1 requires the use of multiple V_{OUT} bypass capacitors. It is recommended to connect one 1µF capacitor between V_{OUT} at Pin 6 and GND at Pin 5 only, and a matching 1µF capacitor between V_{OUT} at Pin 7 and GND at Pin 8 only to complete the Silent Switcher EMI cancellation loops. These two capacitors must be placed as close as possible to the IC, and the loops formed by these two capacitors should be symmetrical and as small as possible to achieve an optimized EMI cancellation performance. Capacitors with small case size, such as 0402 or 0603, are optimal due to the low parasitic inductance. Additional bulk capacitors of 2.2µF or more should be placed close to the IC with the positive terminals connected to V_{OUT}, and negative terminals connected to ground plane. The bypass capacitors for V_{IN} and $INTV_{CC}$ pins should also be connected to the ground plane.

The output capacitors, along with the inductor and input capacitors, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken power ground plane under the application circuit on the layer closest to the surface layer. The SW and BST nodes should be as small as possible.

Keep the FB and RT nodes small so that the ground traces will shield them from the noise generated by the SW and BST nodes. It is recommended to use the GND at Pin 3 for the ground connection of the resistors connecting FB pin or RT Pin (refer to Figure 6).

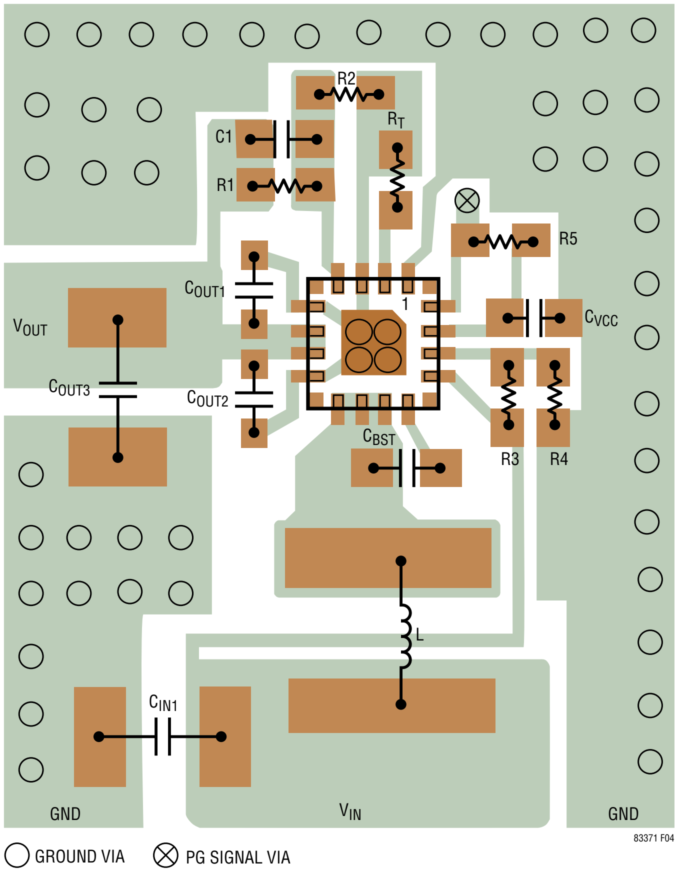


Figure 6. A Recommended PCB Layout for the LT8337

APPLICATIONS INFORMATION

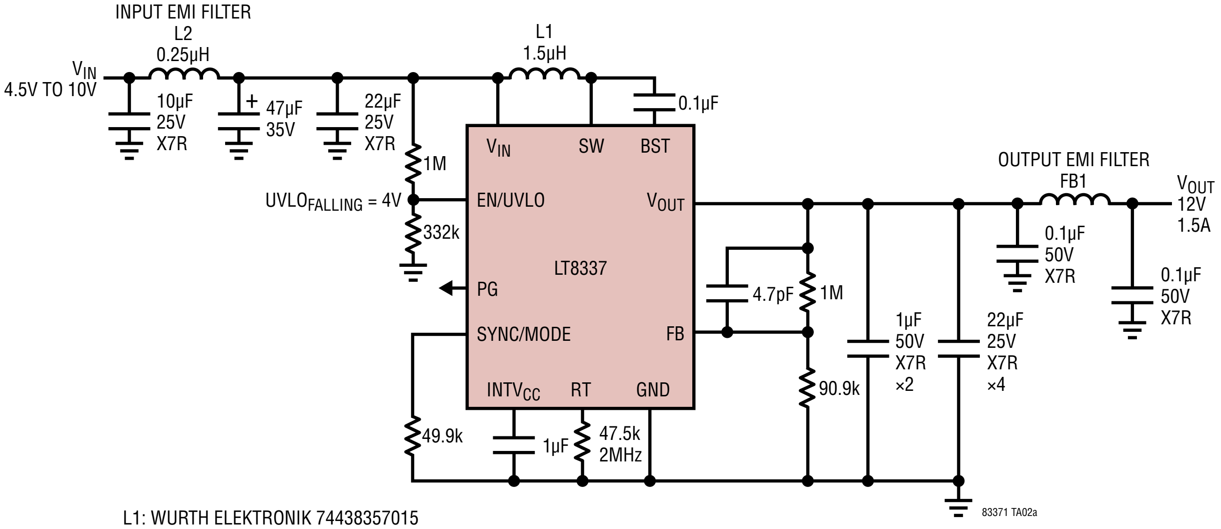
The exposed pad on the bottom of the package should be soldered to the ground plane to reduce the package thermal resistance. To keep the thermal resistance low, extend the ground plane as much as possible, and add many thermal vias to additional power ground planes within the circuit board.

Thermal Considerations

Care should be taken in the layout of the PCB to ensure good heat sinking of the LT8337/LT8337-1. The power ground plane should consist of large copper layers with thermal vias; these layers spread heat dissipated by the IC. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the junction temperature approaches its maximum temperature rating. Power dissipation within the IC can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The junction temperature can be calculated by multiplying the total IC power dissipation by the thermal resistance from junction to ambient and adding the ambient temperature. The IC includes internal overtemperature protection that is intended to protect the device during momentary overload conditions. The overtemperature protection shuts down the IC when the junction temperature exceeds 170°C (typ). The internal soft-start is triggered when the junction temperature drops below 165°C (typ). The maximum rated junction temperature is exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature (see Absolute Maximum Ratings section) may impair device reliability or permanently damage the device.

TYPICAL APPLICATIONS

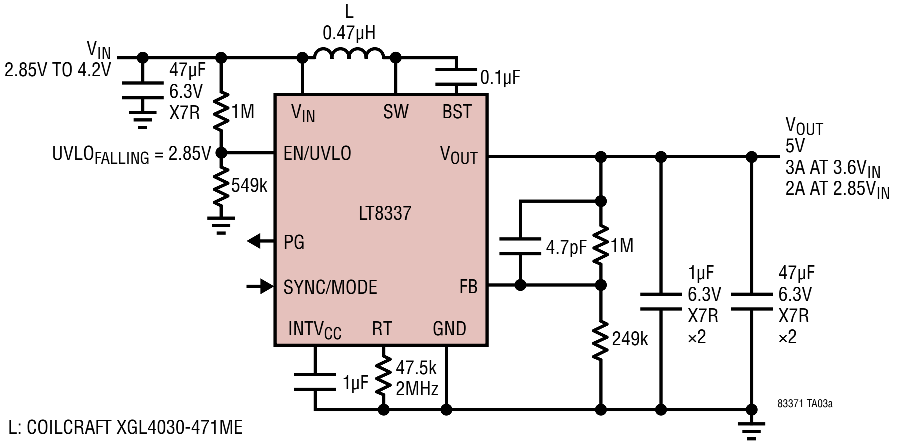
Low I_Q, Low EMI, 15V Output Boost Converter with SSFM


INPUT EMI FILTER
L2
0.25µH
V_{IN}
4.5V TO 10V
10µF
25V
X7R
47µF
35V
22µF
25V
X7R
L1
1.5µH
0.1µF
1M
UVLO$_{FALLING}$ = 4V
332k
V_{IN}
SW
BST
EN/UVLO
V_{OUT}
LT8337
PG
SYNC/MODE
FB
INTV$_{CC}$
RT
GND
49.9k
1µF
47.5k
2MHz
4.7pF
1M
90.9k
1µF
50V
X7R
×2
22µF
25V
X7R
×4
OUTPUT EMI FILTER
FB1
0.1µF
50V
X7R
V_{OUT}
12V
1.5A
0.1µF
50V
X7R
83371 TA02a

L1: WURTH ELEKTRONIK 74438357015
L2: WURTH ELEKTRONIK 74479290125
FB1: WURTH ELEKTRONIK 742792040
* THE EMI PERFORMANCE IS SHOWN IN THE TYPICAL PERFORMANCE CHARACTERISTICS SECTION.

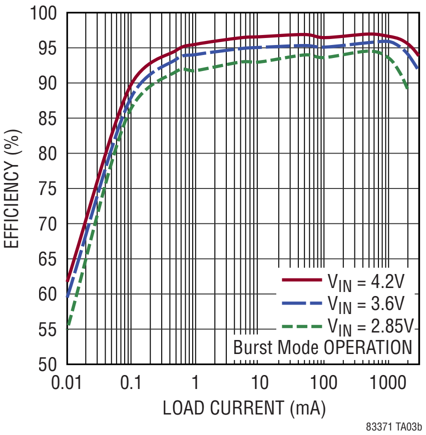
TYPICAL APPLICATIONS

2.85V to 4.2V Input, 2MHz, 5V Output Boost Converter

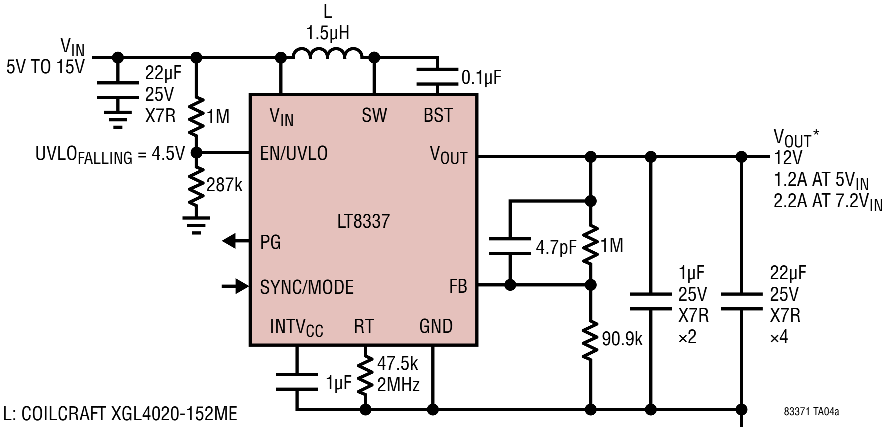

L
0.47µH
V_{IN}
2.85V TO 4.2V
47µF
6.3V
X7R
1M
0.1µF
V_{IN}
SW
BST
$UVLO_{FALLING}$ = 2.85V
EN/UVLO
V_{OUT}
549k
LT8337
PG
SYNC/MODE
FB
$INTV_{CC}$
RT
GND
4.7pF
1M
249k
1µF
6.3V
X7R
×2
47µF
6.3V
X7R
×2
V_{OUT}
5V
3A AT $3.6V_{IN}$
2A AT $2.85V_{IN}$
1µF
47.5k
2MHz
83371 TA03a

L: COILCRAFT XGL4030-471ME

Efficiency vs Output Current

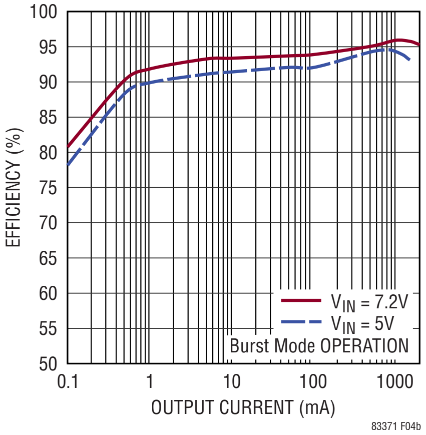


5V to 15V Input, 2MHz, 12V Output Boost Converter

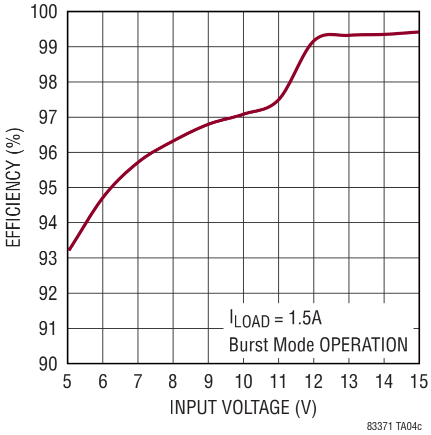

L
1.5µH
V_{IN}
5V TO 15V
22µF
25V
X7R
1M
0.1µF
V_{IN}
SW
BST
$UVLO_{FALLING}$ = 4.5V
EN/UVLO
V_{OUT}
287k
LT8337
PG
SYNC/MODE
FB
$INTV_{CC}$
RT
GND
4.7pF
1M
90.9k
1µF
25V
X7R
×2
22µF
25V
X7R
×4
V_{OUT}*
12V
1.2A AT $5V_{IN}$
2.2A AT $7.2V_{IN}$
1µF
47.5k
2MHz
83371 TA04a

L: COILCRAFT XGL4020-152ME
*WHEN V_{IN} > 12V, V_{OUT} FOLLOWS V_{IN}.

Efficiency vs Output Current

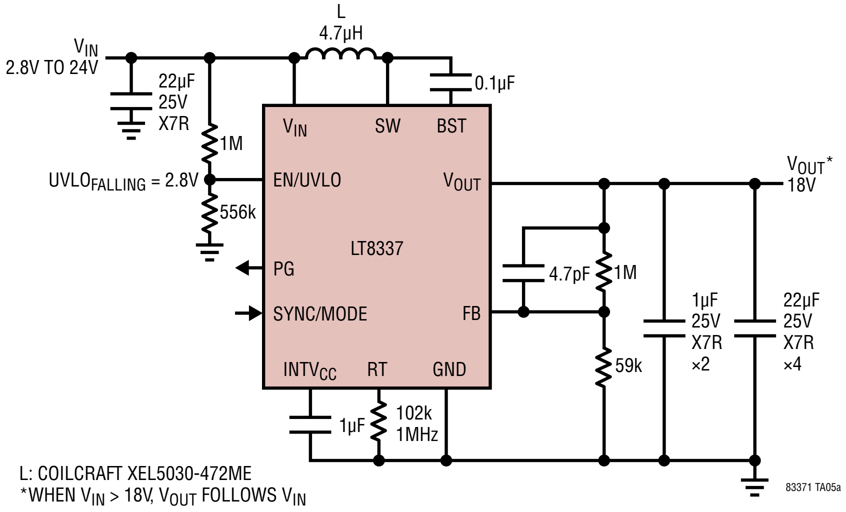


Efficiency vs Input Voltage



TYPICAL APPLICATIONS

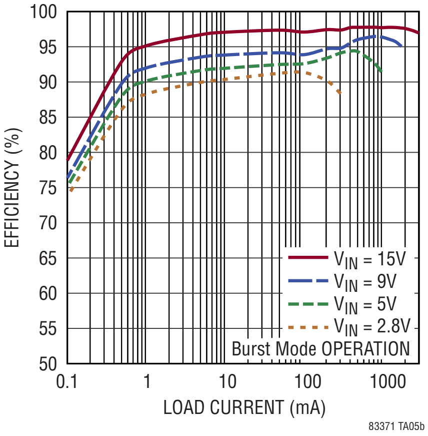
2.8V to 24V Input, 18V Output Boost Converter



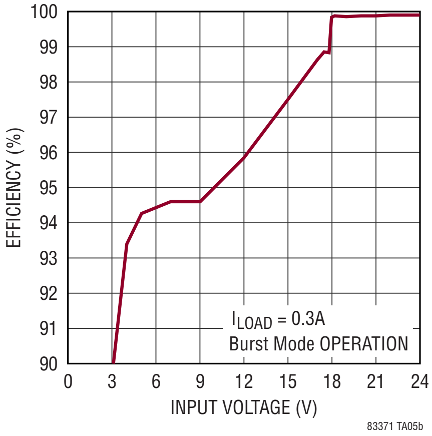
L
4.7µH
V_{IN}
2.8V TO 24V
22µF
25V
X7R
0.1µF
1M
$UVLO_{FALLING}$ = 2.8V
556k
V_{IN}
SW
BST
EN/UVLO
V_{OUT}
LT8337
PG
SYNC/MODE
FB
$INTV_{CC}$
RT
GND
V_{OUT}*
18V
4.7pF
1M
59k
1µF
25V
X7R
×2
22µF
25V
X7R
×4
1µF
102k
1MHz
83371 TA05a

L: COILCRAFT XEL5030-472ME
*WHEN V_{IN} > 18V, V_{OUT} FOLLOWS V_{IN}

Efficiency vs Output Current

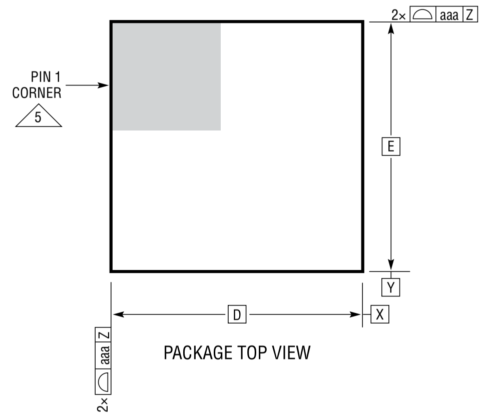


Efficiency vs Input Voltage

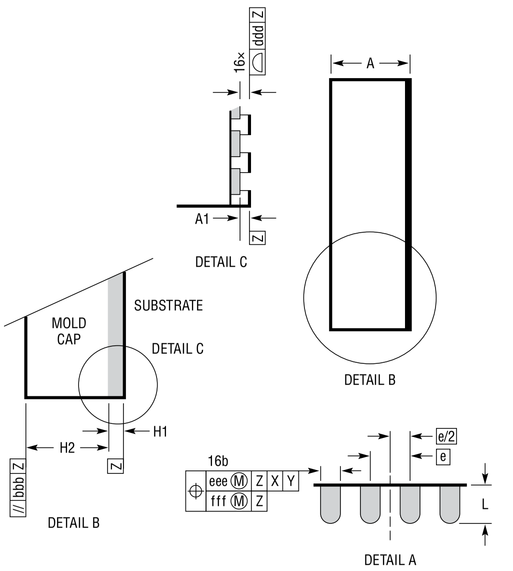


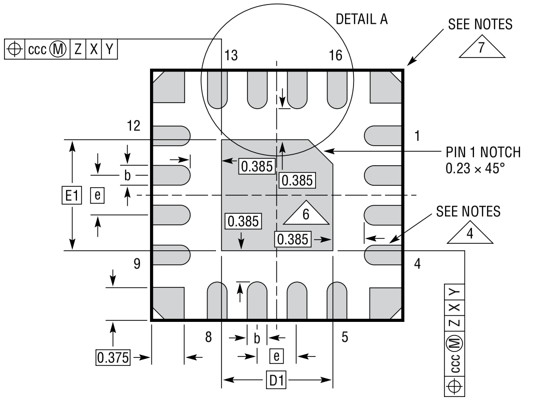
PACKAGE DESCRIPTION

LQFN Package
16-Lead (3mm × 3mm × 0.95mm)
(Reference LTC DWG # 05-08-1798 Rev Ø)

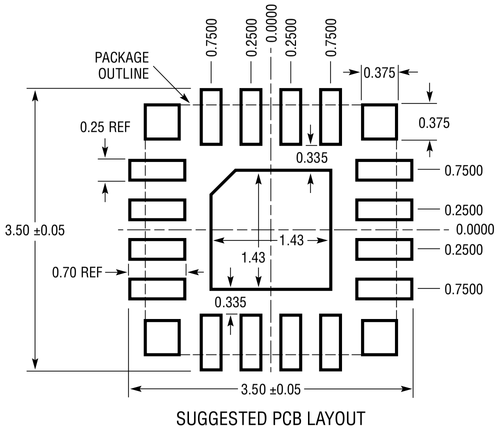

PIN 1
CORNER
5
2× aaa Z
E
Y
D
X
2× aaa Z

PACKAGE TOP VIEW


16×
ddd Z
A1
Z
DETAIL C
A
DETAIL B
MOLD
CAP
SUBSTRATE
DETAIL C
H1
H2
Z
// bbb Z
DETAIL B
16b
eee M Z X Y
fff M Z
e/2
e
L
DETAIL A


ccc M Z X Y
DETAIL A
SEE NOTES
7
13
16
12
1
PIN 1 NOTCH
0.23 × 45°
0.385
0.385
0.385
0.385
6
SEE NOTES
4
E1
e
b
9
4
8
5
b
e
D1
0.375
ccc M Z X Y

PACKAGE BOTTOM VIEW


PACKAGE
OUTLINE
0.7500
0.2500
0.0000
0.2500
0.7500
0.375
0.375
0.25 REF
0.335
0.7500
0.2500
0.0000
0.2500
0.7500
3.50 ±0.05
1.43
1.43
0.70 REF
0.335
3.50 ±0.05

SUGGESTED PCB LAYOUT
TOP VIEW

DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.85	0.95	1.05	
A1			0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		3.00		
E		3.00		
D1		1.43		
E1		1.43		
e		0.50		
H1		0.25 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

2. ALL DIMENSIONS ARE IN MILLIMETERS

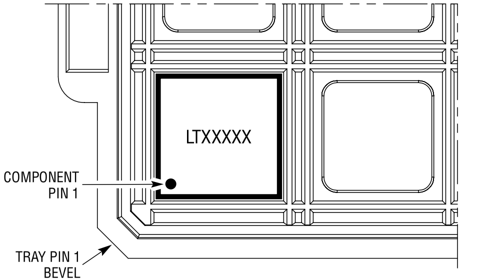
3. PRIMARY DATUM -Z- IS SEATING PLANE

4 METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES

5 DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE

6 THE EXPOSED HEAT FEATURE MAY HAVE OPTIONAL CORNER RADII

7 CORNER SUPPORT PAD CHAMFER IS OPTIONAL


LTXXXXX
COMPONENT
PIN 1
TRAY PIN 1
BEVEL

PACKAGE IN TRAY LOADING ORIENTATION

LGA 16 0321 REV Ø

Rev. 0

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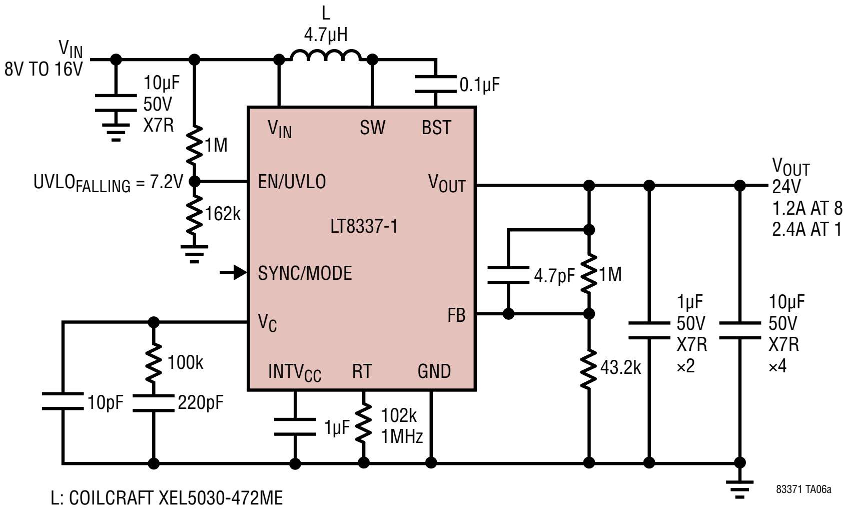
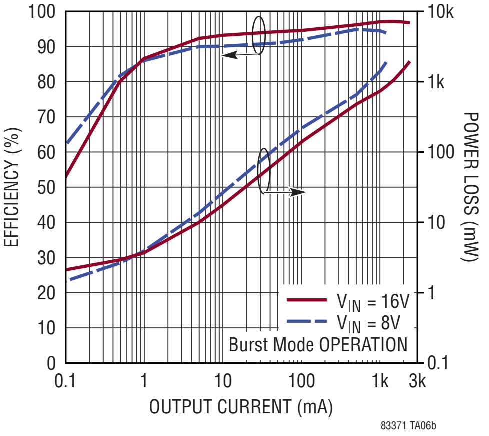
TYPICAL APPLICATION

8V to 16V Input, 24V Output Boost Converter


L
4.7µH
V_{IN}
8V TO 16V
10µF
50V
X7R
1M
UVLO$_{FALLING}$ = 7.2V
162k
0.1µF
V_{IN}
SW
BST
EN/UVLO
V_{OUT}
LT8337-1
SYNC/MODE
V_C
FB
INTV$_{CC}$
RT
GND
100k
10pF
220pF
1µF
102k
1MHz
4.7pF
1M
43.2k
1µF
50V
X7R
×2
10µF
50V
X7R
×4
V_{OUT}
24V
1.2A AT 8V_{IN}
2.4A AT 16V_{IN}
83371 TA06a

L: COILCRAFT XEL5030-472ME

Efficiency and Power Loss vs Output Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8330	1A (I_{SW}), 60V, 2MHz High Efficiency Boost/SEPIC/Inverting DC/DC Converter	V_{IN} = 3V to 40V, $V_{OUT(MAX)}$ = 60V, I_Q = 6µA (Burst Mode Operation), I_{SD} = <1µA, ThinSOT, 2mm × 3mm DFN Packages
LT8331	0.5A (I_{SW}), 140V, 500kHz High Efficiency Boost/Flyback/SEPIC/Inverting DC/DC Converter	V_{IN} = 4.5V to 100V, $V_{OUT(MAX)}$ = 135V, I_Q = 6µA (Burst Mode Operation), I_{SD} = <1µA, MSOP-16(12)E
LT3957A/ LT3957	Boost, Flyback, SEPIC and Inverting Converter with 5A/40V Switch	3V ≤ V_{IN} ≤ 40V, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 5mm × 6mm QFN-36 Package
LT3958	High Input Voltage, Boost, Flyback, SEPIC and Inverting Converter with 3.5A/80V Switch	5V ≤ V_{IN} < 80V, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 5mm × 6mm QFN-36 Package
LT8335	28V, 2A, Low I_Q Boost/SEPIC/Inverting 2MHz Converter	V_{IN} = 3V to 25V, $V_{OUT(MAX)}$ = 25V, I_Q = 6µA (Burst Mode Operation), 3mm × 2mm DFN Package
LT8336	40V, 2.5A, Low I_Q Synchronous Step-Up Silent Switcher	V_{IN} = 2.7V to 40V, $V_{OUT(MAX)}$ = 40V, I_Q = 4µA (Burst Mode Operation), 3mm × 3mm LQFN Package
LT8362	60V, 2A, Low I_Q Boost/SEPIC/Inverting 2MHz Converter	V_{IN} = 2.8V to 60V, $V_{OUT(MAX)}$ = 60V, I_Q = 9µA (Burst Mode Operation), MSOP-16(12)E, 3mm × 3mm DFN-10 Packages
LT8364	60V, 4A, Low I_Q Boost/SEPIC/Inverting 2MHz Converter	V_{IN} = 2.8V to 60V, $V_{OUT(MAX)}$ = 60V, I_Q = 9µA (Burst Mode Operation), MSOP-16(12)E, 4mm × 3mm DFN-12 Packages
LT8494	70V, 2A Boost/SEPIC 1.5MHz High Efficiency Step-Up DC/DC Converter	V_{IN} = 1V to 60V (2.5V to 32V Start-Up), $V_{OUT(MAX)}$ = 70V, I_Q = 3µA (Burst Mode Operation), I_{SD} = <1µA, 20-Lead TSSOP
LT8580	1A (I_{SW}), 65V 1.5MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.55V to 40V, $V_{OUT(MAX)}$ = 65V, I_Q = 1.2mA, I_{SD} = <1µA, 3mm × 3mm DFN-8, MSOP-8E

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