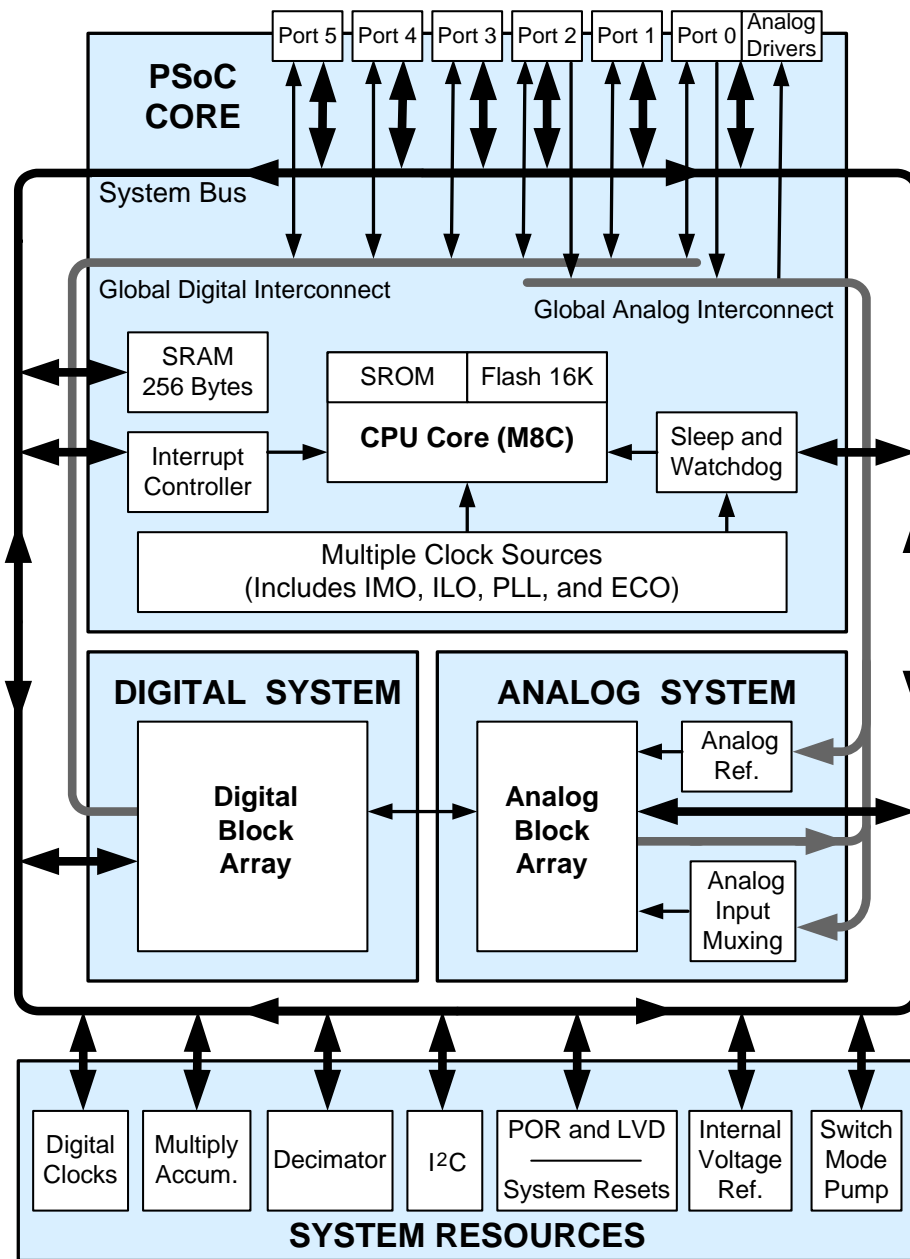## Features

- HB LED Controller
  - Configurable dimmers support up to Eight independent LED channels
  - 8- to 32- bits of resolution per channel
  - Dynamic reconfiguration enables LED controller plus other features: CapSense®, Battery Charging, and Motor Control

- Visual embedded design
  - LED-Based drivers
    - Binning compensation
    - Temperature feedback
    - Optical feedback
    - DMX512

- PrISM modulation technology
  - Reduces radiated EMI
  - Reduces low frequency blinking

- Powerful Harvard-architecture processor
  - M8C processor speeds to 24 MHz
  - 3.0 to 5.25 V operating voltage
  - Operating voltages down to 1.0 V using on-chip switch mode pump (SMP)
  - Industrial temperature range: –40 °C to +85 °C

- Flexible on-chip memory
  - 16 K flash program storage 50,000 erase/write cycles
  - 256 bytes static random access memory (SRAM) data storage
  - In-system serial programming (ISSP)
  - Partial flash updates
  - Flexible protection modes
  - EEPROM emulation in flash

- Advanced peripherals (PSoC® blocks)
  - Eight digital PSoC blocks provide:
    - 8- to 32-bit timers, counters, and pulse-width modulator (PWMs)
    - Up to two full-duplex universal asynchronous receiver transmitter (UARTs)
    - Multiple serial peripheral interface (SPI) masters or slaves
    - Connectable to all general purpose I/O (GPIO) pins
  - 12 Rail-to-Rail analog PSoC blocks provide:
    - Up to 14-bit ADCs
    - Up to 9-bit DACs
    - Programmable gain amplifiers (PGA)
    - Programmable filters and comparators
  - Complex peripherals by combining blocks

- Programmable pin configurations
  - 25 mA sink, 10 mA source on all GPIOs
  - Pull-up, pull-down, high Z, strong, or open-drain drive modes on all GPIOs
  - Up to 12 analog inputs on GPIOs
  - Four 30 mA analog outputs on GPIOs
  - Configurable interrupt on all GPIOs

- Complete development tools
  - Free development software
    - PSoC Designer™
  - Full featured, in-circuit emulator (ICE) and programmer
  - Full speed emulation
  - Complex breakpoint structure
  - 128 KB trace memory

Logic Block Diagram

Contents

1. EZ-Color™ Functional Overview

Cypress' EZ-Color family of devices offers the ideal control solution for high brightness LED applications requiring intelligent dimming control. EZ-Color devices combine the power and flexibility of Programmable System-on-Chip (PSoC®). Cypress' precise illumination signal modulation (PrISM™) modulation technology provides lighting designers a fully customizable and integrated lighting solution platform.

The EZ-Color family supports a range of independent LED channels from 4 channels at 32 bits of resolution each, up to 16 channels at 8 bits of resolution each. This enables lighting designers the flexibility to choose the LED array size and color quality. PSoC Designer software, with lighting specific drivers, can significantly cut development time and simplify implementation of fixed color points through temperature, optical, and LED binning compensation. EZ-Color's virtually limitless analog and digital customization enable simple integration of features in addition to intelligent lighting, such as battery charging, image stabilization, and motor control during the development process. These features, along with Cypress' best-in-class quality and design support, make EZ-Color the ideal choice for intelligent HB LED control applications.

1.1 Target Applications

■ LCD Backlight

■ Large Signs

■ General Lighting

■ Architectural Lighting

■ Camera/Cell Phone Flash

■ Flashlights

1.2 The PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable General Purpose I/O (GPIO).

The M8C CPU core is a powerful processor with speeds up to 48 MHz, providing a four MIPS 8-bit Harvard-architecture microprocessor. The CPU uses an interrupt controller with 17 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and watchdog timers (WDT).

Memory encompasses 16K of Flash for program storage, 256 bytes of SRAM for data storage, and up to 2K of EEPROM emulated using the Flash. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The EZ-Color family incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to 2.5% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz internal low speed oscillator (ILO) is provided for the Sleep timer and WDT. If crystal accuracy is desired, the external crystal oscillator (ECO) (32.768 kHz ECO) is available for use as a real time clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a

system resource), provide the flexibility to integrate almost any timing requirement into the EZ-Color device.

EZ-Color GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

1.3 The Digital System

The digital system is composed of 8 digital blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules.

Figure 1-1. Digital System Block Diagram
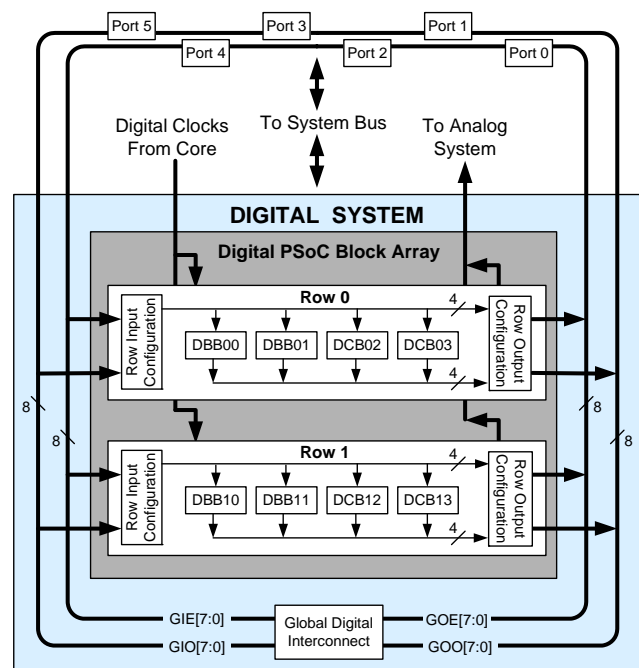
Digital peripheral configurations include the following:

■ PrISM (8- to 32-bit)

■ PWMs (8- to 32-bit)

■ PWMs with dead band (8- to 32-bit)

■ Counters (8- to 32-bit)

■ Timers (8- to 32-bit)

■ UART 8-bit with selectable parity (up to two)

■ SPI slave and master (up to two)

■ I²C slave and multi-master (one available as a system resource)

■ Cyclical redundancy checker (CRC)/Generator (8- to 32-bit)

■ IrDA (up to two)

■ Generators (8- to 32-bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also enable signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by EZ-Color device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled EZ-Color Device Characteristics.

1.4 The Analog System

The analog system is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common EZ-Color analog functions (most available as user modules) are as follows:

■ Analog-to-digital converters (up to 4, with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)

■ Filters (2, 4, 6, and 8 pole band-pass, low-pass, and notch)

■ Amplifiers (up to 4, with selectable gain to 48x)

■ Instrumentation amplifiers (up to 2, with selectable gain to 93x)

■ Comparators (up to 4, with 16 selectable thresholds)

■ DACs (up to 4, with 6- to 9-bit resolution)

■ Multiplying DACs (up to 4, with 6- to 9-bit resolution)

■ High current output drivers (four with 30 mA drive as a core resource)

■ 1.3-V reference (as a system resource)

■ DTMF Dialer

■ Modulators

■ Correlators

■ Peak detectors

■ Many other topologies possible

Analog blocks are provided in columns of three, which includes one Continuous Time (CT) and two Switched Capacitor (SC) blocks, as shown in the figure below.

Figure 1-2. Analog System Block Diagram
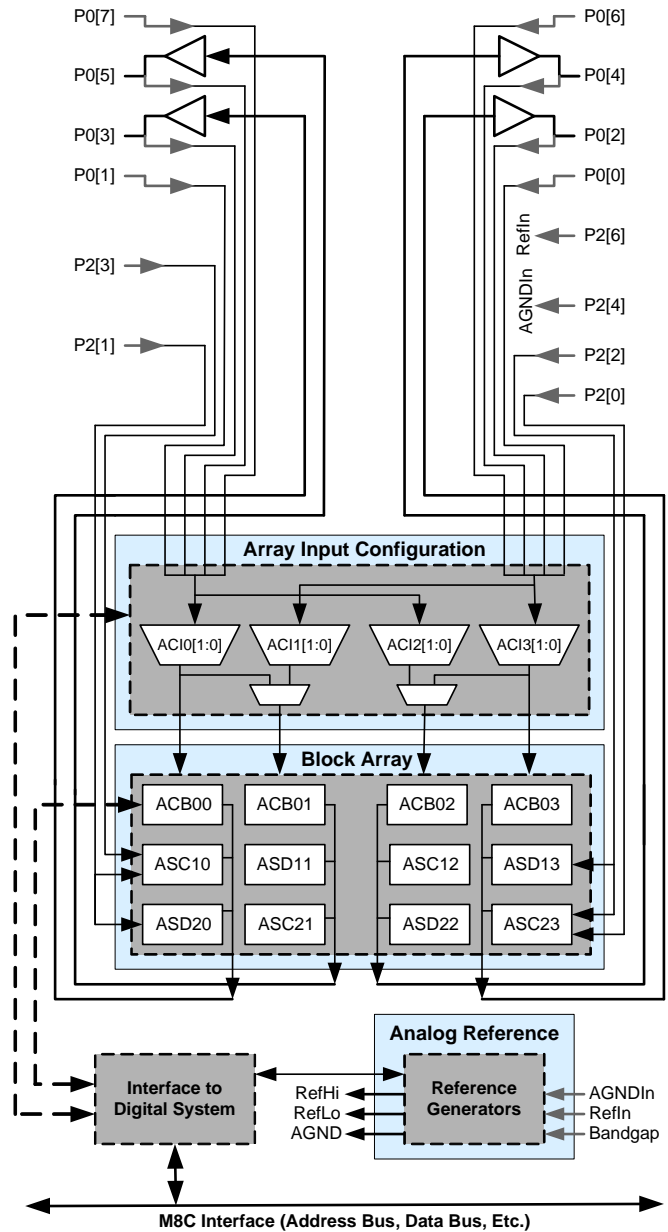
1.1 Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, switch mode pump (SMP), low-voltage detect (LVD), and power-on reset (POR). Statements describing the merits of each system resource are below.

■ Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital blocks as clock dividers.

■ Multiply accumulate (MAC) provides fast 8-bit multiplier with 32-bit accumulate, to assist in general math and digital filters.

■ The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.

■ The I^2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.

■ Low-voltage detect (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.

■ An internal 1.3-V reference provides an absolute reference for the analog system, including ADCs and DACs.

■ An integrated SMP generates normal operating voltages from a single 1.2-V battery cell, providing a low cost boost converter.

1.2 EZ-Color Device Characteristics

Depending on your EZ-Color device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific EZ-Color device groups. The device covered by this data sheet is shown in the highlighted row of the table.

Table 1-1. EZ-Color Device Characteristics

Part Number	LED Channels	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size	CapSense
CY8CLED02	2	16	1	4	8	0	2	4	256 Bytes	4K	No
CY8CLED04	4	56	1	4	48	2	2	6	1K	16K	Yes
CY8CLED08	8	44	2	8	12	4	4	12	256 Bytes	16K	No
CY8CLED16	16	44	4	16	12	4	4	12	2K	32K	No

2. Getting Started

The quickest way to understanding the EZ-Color silicon is by reading this data sheet and using the PSoC Designer integrated development environment (IDE). This data sheet is an overview of the EZ-Color integrated circuit and presents specific pin, register, and electrical specifications.

For up-to-date ordering, packaging, and electrical specification information, see the latest device data sheets on the web at http://www.cypress.com.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com,

covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

3. Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration

- Extensive user module catalog

- Integrated source-code editor (C and assembly)

- Free C compiler with no size restrictions or time limits

- Built-in debugger

- In-circuit emulation

- Built-in support for communication interfaces:
  - Hardware and software I^{2}C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

4. Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called "user modules." User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the "Generate Configuration Files" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

5. Pin Information

5.1 Pinouts

5.1.1 48-Pin Part Pinout QFN

Table 5-1. 48-Pin Part Pinout (QFN)[1]

Pin No.	Type Digital	Type Analog	Pin Name	Description
1	I/O	I	P2[3]	Direct switched capacitor block input.
2	I/O	I	P2[1]	Direct switched capacitor block input.
3	I/O		P4[7]	
4	I/O		P4[5]	
5	I/O		P4[3]	
6	I/O		P4[1]	
7	Power		SMP	Switch mode pump (SMP) connection to external components required.
8	I/O		P3[7]	
9	I/O		P3[5]	
10	I/O		P3[3]	
11	I/O		P3[1]	
12	I/O		P5[3]	
13	I/O		P5[1]	
14	I/O		P1[7]	I^{2}C serial clock (SCL).
15	I/O		P1[5]	I^{2}C serial data (SDA).
16	I/O		P1[3]	
17	I/O		P1[1]	Crystal input (XTALin), I^{2}C SCL, ISSP-SCLK[1].
18	Power		Vss	Ground connection.
19	I/O		P1[0]	Crystal Output (XTALout), I^{2}C SDA, ISSP-SDATA[1].
20	I/O		P1[2]	
21	I/O		P1[4]	Optional external clock input (EXTCLK).
22	I/O		P1[6]	
23	I/O		P5[0]	
24	I/O		P5[2]	
25	I/O		P3[0]	
26	I/O		P3[2]	
27	I/O		P3[4]	
28	I/O		P3[6]	
29	Input		XRES	Active high external reset with internal pull down.
30	I/O		P4[0]	
31	I/O		P4[2]	
32	I/O		P4[4]	
33	I/O		P4[6]	
34	I/O	I	P2[0]	Direct switched capacitor block input.
35	I/O	I	P2[2]	Direct switched capacitor block input.
36	I/O		P2[4]	External Analog Ground (AGND).
37	I/O		P2[6]	External Voltage Reference (VRef).
38	I/O	I	P0[0]	Analog column mux input.
39	I/O	I/O	P0[2]	Analog column mux input and column output.
40	I/O	I/O	P0[4]	Analog column mux input and column output.
41	I/O	I	P0[6]	Analog column mux input.
42	Power		V$_{DD}$	Supply voltage.
43	I/O	I	P0[7]	Analog column mux input.
44	I/O	I/O	P0[5]	Analog column mux input and column output.

Figure 5-1. 48-Pin Device
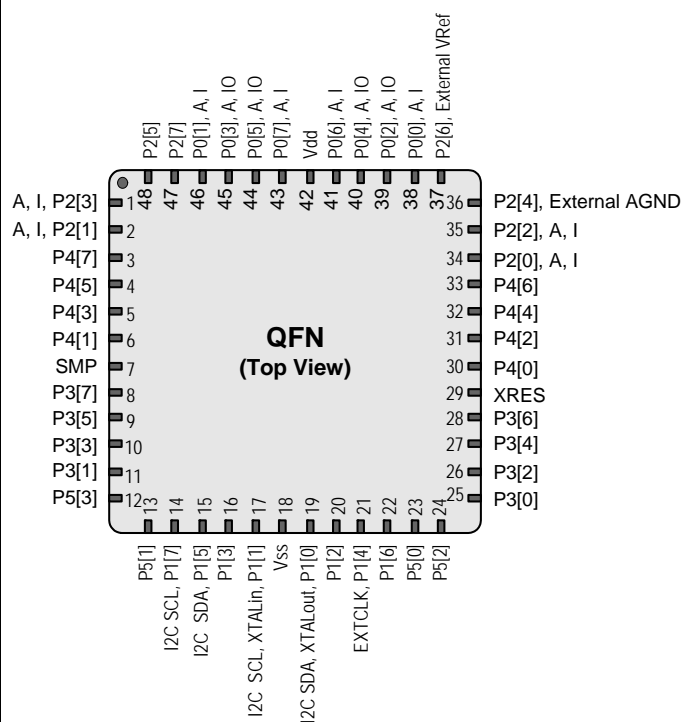
Notes
1. These are the ISSP pins, which are not High Z at POR.
2. The center pad on the QFN package should be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

Table 5-1. 48-Pin Part Pinout (QFN)[1]

45	I/O	I/O	P0[3]	Analog column mux input and column output.
46	I/O	I	P0[1]	Analog column mux input.
47	I/O		P2[7]	
48	I/O		P2[5]	

LEGEND: A = Analog, I = Input, and O = Output.

6. Register Reference

This section lists the registers of the CY8CLED08 EZ-Color device.

6.1 Register Conventions

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

6.2 Register Mapping Tables

The device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and Bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set to 1, the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Table 6-1. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW		C0	
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48		ASC12CR0	88	RW		C8	
PRT2IE	09	RW		49		ASC12CR1	89	RW		C9	
PRT2GS	0A	RW		4A		ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW		4B		ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW		4C		ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW		4D		ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW		4E		ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW		D0	
PRT4IE	11	RW		51		ASD20CR1	91	RW		D1	
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW		D3	
PRT5DR	14	RW		54		ASC21CR0	94	RW		D4	
PRT5IE	15	RW		55		ASC21CR1	95	RW		D5	
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW		DC	
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW

Blank fields are Reserved and should not be accessed.   # Access is bit specific.

Table 6-1. Register Map Bank 0 Table: User Space (continued)

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
	1F			5F		ASC23CR3	9F	RW		DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL_X	E8	W
DCB02DR1	29	W		69			A9		MUL_Y	E9	W
DCB02DR2	2A	RW		6A			AA		MUL_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL_DL	EB	R
DCB03DR0	2C	#		6C			AC		ACC_DR1	EC	RW
DCB03DR1	2D	W		6D			AD		ACC_DR0	ED	RW
DCB03DR2	2E	RW		6E			AE		ACC_DR3	EE	RW
DCB03CR0	2F	#		6F			AF		ACC_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCB12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#	ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.   # Access is bit specific.

Table 6-2. Register Map Bank 1 Table: Configuration Space

Name	Add (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASC10CR0	80	RW		C0	
PRT0DM1	01	RW		41		ASC10CR1	81	RW		C1	
PRT0IC0	02	RW		42		ASC10CR2	82	RW		C2	
PRT0IC1	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DM0	04	RW		44		ASD11CR0	84	RW		C4	
PRT1DM1	05	RW		45		ASD11CR1	85	RW		C5	
PRT1IC0	06	RW		46		ASD11CR2	86	RW		C6	
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW		48		ASC12CR0	88	RW		C8	
PRT2DM1	09	RW		49		ASC12CR1	89	RW		C9	
PRT2IC0	0A	RW		4A		ASC12CR2	8A	RW		CA	
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW		CB	
PRT3DM0	0C	RW		4C		ASD13CR0	8C	RW		CC	
PRT3DM1	0D	RW		4D		ASD13CR1	8D	RW		CD	
PRT3IC0	0E	RW		4E		ASD13CR2	8E	RW		CE	
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW		50		ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW		54		ASC21CR0	94	RW		D4	
PRT5DM1	15	RW		55		ASC21CR1	95	RW		D5	
PRT5IC0	16	RW		56		ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
	18			58		ASD22CR0	98	RW		D8	
	19			59		ASD22CR1	99	RW		D9	
	1A			5A		ASD22CR2	9A	RW		DA	

Blank fields are Reserved and should not be accessed.   # Access is bit specific.

Table 6-2. Register Map Bank 1 Table: Configuration Space (continued)

Name	Add (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
	1B			5B		ASD22CR3	9B	RW		DB	
	1C			5C		ASC23CR0	9C	RW		DC	
	1D			5D		ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
	1E			5E		ASC23CR2	9E	RW	OSC_CR4	DE	RW
	1F			5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	W
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW		6C			AC			EC	
DCB03IN	2D	RW		6D			AD			ED	
DCB03OU	2E	RW		6E			AE			EE	
	2F			6F			AF			EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11IN	35	RW	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11OU	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12IN	39	RW	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12OU	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
	3B		ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13FN	3C	RW	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13IN	3D	RW	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13OU	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
	3F		ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

**Blank fields are Reserved and should not be accessed.**   # Access is bit specific.

7. Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED08 EZ-Color device. For the most up to date electrical specifications, confirm that you have the most recent datasheet by going to the web at http://www.cypress.com.

Specifications are valid for –40 °C $\leq T_A \leq$ 85 °C and $T_J \leq$ 100 °C, except where noted. Specifications for devices running at greater than 12 MHz are valid for –40 °C $\leq T_A \leq$ 70 °C and $T_J \leq$ 82 °C.

Figure 7-1. Voltage vs. CPU Frequency
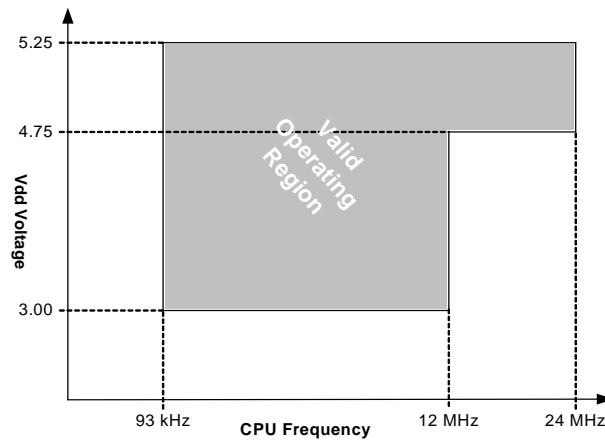
7.1 Absolute Maximum Ratings

Table 7-1. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	−55	25	+100	°C	Higher storage temperatures will reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C will degrade reliability.
$T_{BAKETEMP}$	Bake temperature	−	125	See package label	°C	
$T_{BAKETIME}$	Bake Time	See package label	−	72	Hours	
T_A	Ambient temperature with power applied	−40	−	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to Vss	−0.5	−	+6.0	V	
V_{IO}	DC input voltage	Vss- 0.5	−	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	Vss - 0.5	−	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	−25	−	+50	mA	
I_{MAIO}	Maximum current into any port pin configured as analog driver	−50	−	+50	mA	
ESD	Electrostatic discharge voltage	2000	−	−	V	Human Body Model ESD.
LU	Latch up current	−	−	200	mA	

7.2 Operating Temperature

Table 7-2. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	−40	−	+85	°C	
T_J	Junction temperature	−40	−	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 41. The user must limit the power consumption to comply with this requirement.

7.3 DC Electrical Characteristics

7.3.1 DC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and −40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and −40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 7-3. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	3.00	–	5.25	V	
I_{DD}	Supply current	–	5	8	mA	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I_{DD3}	Supply current	–	3.3	6.0	mA	Conditions are V_{DD} = 3.3 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I_{SB}	Sleep (mode) current with POR, LVD, sleep timer, and WDT.[3]	–	3	6.5	μA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, −40 °C ≤ T_A ≤ 55 °C.
I_{SBH}	Sleep (mode) current with POR, LVD, sleep timer, and WDT at high temperature.[3]	–	4	25	μA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, 55 °C < T_A ≤ 85 °C.
I_{SBXTL}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and external crystal.[3]	–	4	7.5	μA	Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V_{DD} = 3.3 V, −40 °C ≤ T_A ≤ 55 °C.
I_{SBXTLH}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and external crystal at high temperature.[3]	–	5	26	μA	Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V_{DD} = 3.3 V, 55 °C < T_A ≤ 85 °C.
V_{REF}	Reference voltage (Bandgap) for Silicon A [4]	1.275	1.300	1.325	V	Trimmed for appropriate V_{DD}.
V_{REF}	Reference voltage (Bandgap) for Silicon B [4]	1.280	1.300	1.320	V	Trimmed for appropriate V_{DD}.

Notes
3. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This should be compared with devices that have similar functions enabled.
4. Refer to the "Ordering Information" on page 44.

7.3.2 DC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C $\leq T_A \leq$ 85 °C, or 3.0 V to 3.6 V and –40 °C $\leq T_A \leq$ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 7-4. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} - 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])).
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])).
I_{OH}	High level source current	10	–	–	mA	V_{OH} = V_{DD}-1.0 V. See the limitations of the total current in the Note for V_{OH}.
I_{OL}	Low level sink current	25	–	–	mA	V_{OL} = 0.75 V. See the limitations of the total current in the Note for VOL.
V_{IL}	Input low level	–	–	0.8	V	V_{DD} = 3.0 to 5.25.
V_{IH}	Input high level	2.1	–		V	V_{DD} = 3.0 to 5.25.
V_H	Input hysterisis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.

7.3.3 DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C $\leq T_A \leq$ 85 °C, or 3.0 V to 3.6 V and –40 °C $\leq T_A \leq$ 85 °C, respectively. Typical parameters are measured at to 5 V and 3.3 V at 25 °C and are for design guidance only.

The operational amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25 °C and are for design guidance only.

Table 1. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, opamp bias = low Power = low, opamp bias = high Power = medium, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = low Power = high, opamp bias = high	– – – – – –	1.6 1.6 1.6 1.6 1.6 1.6	10 10 10 10 10 10	mV mV mV mV mV mV	
TCV_{OSOA}	Average input offset voltage drift	–	4	20	μV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	20	–	pA	Gross tested to 1 μA.
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C

Table 1. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{CMOA}	Common mode voltage range	0	–	V_{DD}	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
	Common mode voltage range (high power or high opamp bias)	0.5	–	$V_{DD} - 0.5$	V	
$CMRR_{OA}$	Common mode rejection ratio Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	60 60 60	– – –	– – –	dB dB dB	Specification is applicable at both High and Low opamp bias.
G_{OLOA}	Open loop gain Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	60 60 80	– – –	– – –	dB dB dB	Specification is applicable at High opamp bias. For Low opamp bias mode, minimum is 60dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	$V_{DD} - 0.2$ $V_{DD} - 0.2$ $V_{DD} - 0.5$	– – –	– – –	V V V	
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, opamp bias = high Power = medium, opamp bias = high Power = high, opamp bias = high	– – –	– – –	0.2 0.2 0.5	V V V	
I_{SOA}	Supply current (including associated AGND buffer) Power = low, opamp bias = low Power = low, opamp bias = high Power = medium, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = low Power = high, opamp bias = high	– – – – – –	150 300 600 1200 2400 4600	200 400 800 1600 3200 6400	µA µA µA µA µA µA	
$PSRR_{OA}$	Supply voltage rejection ratio	60	–	–	dB	$Vss £ V_{IN} £ (V_{DD} - 2.25)$ or $(V_{DD} - 1.25 V) £ V_{IN} £ V_{DD}$.

Table 2. 3.3-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, opamp bias = low Power = low, opamp bias = high Power = medium, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = low Power = high, opamp bias = high	– – – – – –	1.4 1.4 1.4 1.4 1.4 –	10 10 10 10 10 –	mV mV mV mV mV mV	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
TCV_{OSOA}	Average input offset voltage drift	–	7	40	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	20	–	pA	Gross tested to 1µA.
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common mode voltage range	0.2	–	$V_{DD} - 0.2$	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.

Table 2. 3.3-V DC Operational Amplifier Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Notes
$CMRR_{OA}$	Common mode rejection ratio Power = low, opamp bias = low Power = medium, opamp bias = low Power = high, opamp bias = low	 50 50 50	 – – –	 – – –	 dB dB dB	Specification is applicable at Low opamp bias. For High bias mode (except High Power, High opamp bias), minimum is 60 dB.
G_{OLOA}	Open loop gain Power = low, opamp bias = low Power = medium, opamp bias = low Power = high, opamp bias = low	 60 60 80	 – – –	 – – –	 dB dB dB	Specification is applicable at Low opamp bias. For High opamp bias mode (except High Power, High opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, opamp bias = low Power = medium, opamp bias = low Power = high, opamp bias = low	 $V_{DD} - 0.2$ $V_{DD} - 0.2$ $V_{DD} - 0.2$	 – – –	 – – –	 V V V	Power = high, opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, opamp bias = low Power = medium, opamp bias = low Power = high, opamp bias = low	 – – –	 – – –	 0.2 0.2 0.2	 V V V	Power = high, opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
I_{SOA}	Supply current (including associated AGND buffer) Power = low, opamp bias = low Power = low, opamp bias = high Power = medium, opamp bias = low Power = medium, opamp bias = high Power = high, opamp bias = low Power = high, opamp bias = high	 – – – – – –	 150 300 600 1200 2400 –	 200 400 800 1600 3200 –	 μA μA μA μA μA μA	Power = high, opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
$PSRR_{OA}$	Supply voltage rejection ratio	50	80	–	dB	$V_{SS} £ V_{IN} £ (V_{DD} - 2.25)$ or $(V_{DD} - 1.25 V) £ V_{IN} £ V_{DD}$.

7.3.4 DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40 °C \le T_A \le 85 °C$, 3.0 V to 3.6 V and $-40 °C \le T_A \le 85 °C$, or 2.4 V to 3.0 V and $-40 °C \le T_A \le 85 °C$, respectively. Typical parameters are measured at 5 V at 25 °C and are for design guidance only.

Table 7-5. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	V_{DD} - 1	V	
I_{SLPC}	LPC supply current	–	10	40	μA	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	

7.3.5 DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C $\leq$ T_A $\leq$ 85 °C, or 3.0 V to 3.6 V and –40 °C $\leq$ T_A $\leq$ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 3. 5-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{OSOB}	Input offset voltage (absolute value) Power = low, opamp bias = low Power = low, opamp bias = high Power = high, opamp bias = low Power = high, opamp bias = high	– – – –	3 3 3 3	19 19 19 19	mV mV mV mV	
TCV_{OSOB}	Average input offset voltage drift	–	5	30	µV/°C	
V_{CMOB}	Common-mode input voltage range	0.5	–	$V_{DD} - 1.0$	V	
R_{OUTOB}	Output resistance Power = low Power = high	– –	1 1	– –	W W	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 ohms to V_{DD}/2) Power = low Power = high	$0.5 \times V_{DD} + 1.3$ $0.5 \times V_{DD} + 1.3$	– –	– –	V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 ohms to V_{DD}/2)					
	Power = low	–	–	$0.5 \times V_{DD} - 1.3$	V	
	Power = high	–	–	$0.5 \times V_{DD} - 1.3$	V	
I_{SOB}	Supply current including opamp bias cell (no load) Power = low Power = high	– –	1.1 2.6	5.1 8.8	mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	60	64	–	dB	
I_{OMAX}	Maximum output current	–	40	–	mA	
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit driven by the analog output buffer.

Table 4. 3.3-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{OSOB}	Input offset voltage (absolute value) Power = low, opamp bias = low Power = low, opamp bias = high Power = high, opamp bias = low Power = high, opamp bias = high	– – – –	3.2 3.2 6 6	20 20 25 25	mV mV mV mV	High power setting is not recommended.
TCV_{OSOB}	Average input offset voltage drift Power = low, opamp bias = low Power = low, opamp bias = high Power = high, opamp bias = low Power = high, opamp bias = high	– – – –	9 9 12 12	55 55 70 70	µV/°C µV/°C µV/°C µV/°C	High power setting is not recommended.
V_{CMOB}	Common-mode input voltage range	0.5	–	$V_{DD} - 1.0$	V	
R_{OUTOB}	Output resistance Power = low Power = high	– –	1 1	– –	W W	
$V_{OHIGHOB}$	High output voltage swing (load = 32 ohms to $V_{DD}/2$) Power = low Power = high	$0.5 \times V_{DD} + 1.0$ $0.5 \times V_{DD} + 1.0$	– –	– –	V V	
V_{OLOWOB}	Low output voltage swing (load = 32 ohms to $V_{DD}/2$) Power = low Power = high	– –	– –	$0.5 \times V_{DD} - 1.0$ $0.5 \times V_{DD} - 1.0$	V V	
I_{SOB}	Supply current including opamp bias cell (no load) Power = low Power = high	– –	0.8 2.0	2 4.3	mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	60	64	–	dB	
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit driven by the analog output buffer.

7.3.6 DC Switch Mode Pump Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at to 5 V and 3.3 V at 25 °C and are for design guidance only.

**Table 7-6. DC Switch Mode Pump (SMP) Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP} 5 V	5 V output voltage	4.75	5.0	5.25	V	Configured as in Note 5. Average, neglecting ripple. SMP trip voltage is set to 5.0 V.
V_{PUMP} 3 V	3 V output voltage	3.00	3.25	3.60	V	Configured as in Note 5. Average, neglecting ripple. SMP trip voltage is set to 3.25 V.
I_{PUMP}	Available output current V_{BAT} = 1.5 V, V_{PUMP} = 3.25 V V_{BAT} = 1.8 V, V_{PUMP} = 5.0 V	8 5	– –	– –	mA mA	Configured as in Note 5. SMP trip voltage is set to 3.25 V. SMP trip voltage is set to 5.0 V.
V_{BAT}5V	Input voltage range from battery	1.8	–	5.0	V	Configured as in Note 5. SMP trip voltage is set to 5.0 V.
V_{BAT}3V	Input voltage range from battery	1.0	–	3.3	V	Configured as in Note 5. SMP trip voltage is set to 3.25 V.
$V_{BATSTART}$	Minimum input voltage from battery to start pump	1.1	–	–	V	Configured as in Note 5.
ΔV_{PUMP_Line}	Line regulation (over V_{BAT} range)	–	5	–	%V_O	Configured as in Note 5. V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 7-2 on page 29.
ΔV_{PUMP_Load}	Load regulation	–	5	–	%V_O	Configured as in Note 5. V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 7-2 on page 29.
ΔV_{PUMP_Ripple}	Output voltage ripple (depends on capacitor/load)	–	100	–	mVpp	Configured as in Note 5. Load is 5 mA.
E_3	Efficiency	35	50	–	%	Configured as in Note 5. Load is 5 mA. SMP trip voltage is set to 3.25 V.
F_{PUMP}	Switching frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching duty cycle	–	50	–	%	

Note
5. L1 = 2 μH inductor, C1 = 10 μF capacitor, D1 = Schottky diode.

Figure 7-2. Basic Switch Mode Pump Circuit
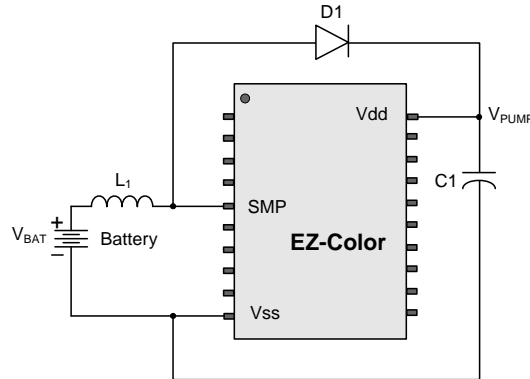
7.0.1 DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\ °C \leq T_A \leq 85\ °C$, or 3.0 V to 3.6 V and $-40\ °C \leq T_A \leq 85\ °C$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 5. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.228	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.352	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ − 0.078	$V_{DD}/2$ − 0.007	$V_{DD}/2$ + 0.063	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ − Bandgap	$V_{DD}/2$ − 1.336	$V_{DD}/2$ − 1.295	$V_{DD}/2$ − 1.250	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.224	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.356	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ − 0.056	$V_{DD}/2$ − 0.005	$V_{DD}/2$ + 0.043	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ − Bandgap	$V_{DD}/2$ − 1.338	$V_{DD}/2$ − 1.298	$V_{DD}/2$ − 1.255	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.356	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ − 0.057	$V_{DD}/2$ − 0.006	$V_{DD}/2$ + 0.044	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ − Bandgap	$V_{DD}/2$ − 1.337	$V_{DD}/2$ − 1.298	$V_{DD}/2$ − 1.256	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.226	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.359	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ − 0.047	$V_{DD}/2$ − 0.004	$V_{DD}/2$ + 0.035	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ − Bandgap	$V_{DD}/2$ − 1.338	$V_{DD}/2$ − 1.299	$V_{DD}/2$ − 1.258	V

Table 5. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] − 0.085	P2[4] + P2[6] − 0.016	P2[4] + P2[6] + 0.044	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] − P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] − P2[6] − 0.022	P2[4] − P2[6] + 0.010	P2[4] − P2[6] + 0.055	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] − 0.077	P2[4] + P2[6] − 0.010	P2[4] + P2[6] + 0.051	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] − P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] − P2[6] − 0.022	P2[4] − P2[6] + 0.005	P2[4] − P2[6] + 0.039	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] − 0.070	P2[4] + P2[6] − 0.010	P2[4] + P2[6] + 0.050	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] − P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] − P2[6] − 0.022	P2[4] − P2[6] + 0.005	P2[4] − P2[6] + 0.039	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] + P2[6] − 0.070	P2[4] + P2[6] − 0.007	P2[4] + P2[6] + 0.054	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] − P2[6] (P2[4] = V_{DD}/2, P2[6] = 1.3 V)	P2[4] − P2[6] − 0.022	P2[4] − P2[6] + 0.002	P2[4] − P2[6] + 0.032	V
0b010	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} − 0.037	V_{DD} − 0.009	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 − 0.061	V_{DD}/2 − 0.006	V_{DD}/2 + 0.047	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.007	V_{SS} + 0.028	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} − 0.039	V_{DD} − 0.006	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 − 0.049	V_{DD}/2 − 0.005	V_{DD}/2 + 0.036	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.019	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} − 0.037	V_{DD} − 0.007	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 − 0.054	V_{DD}/2 − 0.005	V_{DD}/2 + 0.041	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.024	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} − 0.042	V_{DD} − 0.005	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 − 0.046	V_{DD}/2 − 0.004	V_{DD}/2 + 0.034	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.017	V

Table 5. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b011	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	3 × Bandgap	3.788	3.891	3.986	V
		V_{AGND}	AGND	2 × Bandgap	2.500	2.604	3.699	V
		V_{REFLO}	Ref Low	Bandgap	1.257	1.306	1.359	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	3 × Bandgap	3.792	3.893	3.982	V
		V_{AGND}	AGND	2 × Bandgap	2.518	2.602	2.692	V
		V_{REFLO}	Ref Low	Bandgap	1.256	1.302	1.354	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	3 × Bandgap	3.795	3.894	3.993	V
		V_{AGND}	AGND	2 × Bandgap	2.516	2.603	2.698	V
		V_{REFLO}	Ref Low	Bandgap	1.256	1.303	1.353	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	3 × Bandgap	3.792	3.895	3.986	V
		V_{AGND}	AGND	2 × Bandgap	2.522	2.602	2.685	V
		V_{REFLO}	Ref Low	Bandgap	1.255	1.301	1.350	V
0b100	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.495 – P2[6]	2.586 – P2[6]	2.657 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.502	2.604	2.719	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.531 – P2[6]	2.611 – P2[6]	2.681 – P2[6]	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.500 – P2[6]	2.591 – P2[6]	2.662 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.519	2.602	2.693	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.530 – P2[6]	2.605 – P2[6]	2.666 – P2[6]	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.503 – P2[6]	2.592 – P2[6]	2.662 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.517	2.603	2.698	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.529 – P2[6]	2.606 – P2[6]	2.665 – P2[6]	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.505 – P2[6]	2.594 – P2[6]	2.665 – P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.525	2.602	2.685	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.528 – P2[6]	2.603 – P2[6]	2.661 – P2[6]	V

Table 5. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b101	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.222	P2[4] + 1.290	P2[4] + 1.343	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.331	P2[4] – 1.295	P2[4] – 1.254	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.226	P2[4] + 1.293	P2[4] + 1.347	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.331	P2[4] – 1.298	P2[4] – 1.259	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.227	P2[4] + 1.294	P2[4] + 1.347	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.331	P2[4] – 1.298	P2[4] – 1.259	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.228	P2[4] + 1.295	P2[4] + 1.349	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.332	P2[4] – 1.299	P2[4] – 1.260	V
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.535	2.598	2.644	V
		V_{AGND}	AGND	Bandgap	1.227	1.305	1.398	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.009	V_{SS} + 0.038	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.530	2.598	2.643	V
		V_{AGND}	AGND	Bandgap	1.244	1.303	1.370	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.024	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.532	2.598	2.644	V
		V_{AGND}	AGND	Bandgap	1.239	1.304	1.380	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.026	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.528	2.598	2.645	V
		V_{AGND}	AGND	Bandgap	1.249	1.302	1.362	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.018	V
0b111	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.041	4.155	4.234	V
		V_{AGND}	AGND	1.6 × Bandgap	1.998	2.083	2.183	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.010	V_{SS} + 0.038	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.047	4.153	4.236	V
		V_{AGND}	AGND	1.6 × Bandgap	2.012	2.082	2.157	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.024	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.049	4.154	4.238	V
		V_{AGND}	AGND	1.6 × Bandgap	2.008	2.083	2.165	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.026	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.047	4.154	4.238	V
		V_{AGND}	AGND	1.6 × Bandgap	2.016	2.081	2.150	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.018	V

Table 6. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.225$	$V_{DD}/2 + 1.292$	$V_{DD}/2 + 1.361$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 - 0.067$	$V_{DD}/2 - 0.002$	$V_{DD}/2 + 0.063$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 - 1.35$	$V_{DD}/2 - 1.293$	$V_{DD}/2 - 1.210$	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.218$	$V_{DD}/2 + 1.294$	$V_{DD}/2 + 1.370$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 - 0.038$	$V_{DD}/2 - 0.001$	$V_{DD}/2 + 0.035$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 - 1.329$	$V_{DD}/2 - 1.296$	$V_{DD}/2 - 1.259$	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.221$	$V_{DD}/2 + 1.294$	$V_{DD}/2 + 1.366$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 - 0.050$	$V_{DD}/2 - 0.002$	$V_{DD}/2 + 0.046$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 - 1.331$	$V_{DD}/2 - 1.296$	$V_{DD}/2 - 1.260$	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.226$	$V_{DD}/2 + 1.295$	$V_{DD}/2 + 1.365$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 - 0.028$	$V_{DD}/2 - 0.001$	$V_{DD}/2 + 0.025$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 - 1.329$	$V_{DD}/2 - 1.297$	$V_{DD}/2 - 1.262$	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.098	P2[4] + P2[6] – 0.018	P2[4] + P2[6] + 0.055	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.055	P2[4] – P2[6] + 0.013	P2[4] – P2[6] + 0.086	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.082	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.050	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.037	P2[4] – P2[6] + 0.006	P2[4] – P2[6] + 0.054	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.079	P2[4] + P2[6] – 0.012	P2[4] + P2[6] + 0.047	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.038	P2[4] – P2[6] + 0.006	P2[4] – P2[6] + 0.057	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.080	P2[4] + P2[6] – 0.008	P2[4] + P2[6] + 0.055	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.032	P2[4] – P2[6] + 0.003	P2[4] – P2[6] + 0.042	V

Table 6. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b010	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	$V_{DD} - 0.06$	$V_{DD} - 0.010$	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 - 0.05$	$V_{DD}/2 - 0.002$	$V_{DD}/2 + 0.040$	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.009	Vss + 0.056	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	$V_{DD} - 0.060$	$V_{DD} - 0.006$	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 - 0.028$	$V_{DD}/2 - 0.001$	$V_{DD}/2 + 0.025$	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.005	Vss + 0.034	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	$V_{DD} - 0.058$	$V_{DD} - 0.008$	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 - 0.037$	$V_{DD}/2 - 0.002$	$V_{DD}/2 + 0.033$	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.007	Vss + 0.046	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	$V_{DD} - 0.057$	$V_{DD} - 0.006$	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 - 0.025$	$V_{DD}/2 - 0.001$	$V_{DD}/2 + 0.022$	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.004	Vss + 0.030	V
0b011	All power settings. Not allowed for 3.3 V	–	–	–	–	–	–	–
0b100	All power settings. Not allowed for 3.3 V	–	–	–	–	–	–	–
0b101	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = $V_{DD}/2$)	P2[4] + 1.213	P2[4] + 1.291	P2[4] + 1.367	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = $V_{DD}/2$)	P2[4] – 1.333	P2[4] – 1.294	P2[4] – 1.208	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = $V_{DD}/2$)	P2[4] + 1.217	P2[4] + 1.294	P2[4] + 1.368	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = $V_{DD}/2$)	P2[4] – 1.320	P2[4] – 1.296	P2[4] – 1.261	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = $V_{DD}/2$)	P2[4] + 1.217	P2[4] + 1.294	P2[4] + 1.369	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = $V_{DD}/2$)	P2[4] – 1.322	P2[4] – 1.297	P2[4] – 1.262	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = $V_{DD}/2$)	P2[4] + 1.219	P2[4] + 1.295	P2[4] + 1.37	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	V
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = $V_{DD}/2$)	P2[4] – 1.324	P2[4] – 1.297	P2[4] – 1.262	V

Table 6. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Unit
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.507	2.598	2.698	V
		V_{AGND}	AGND	Bandgap	1.203	1.307	1.424	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.012	Vss + 0.067	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.516	2.598	2.683	V
		V_{AGND}	AGND	Bandgap	1.241	1.303	1.376	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.007	Vss + 0.040	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.510	2.599	2.693	V
		V_{AGND}	AGND	Bandgap	1.240	1.305	1.374	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.008	Vss + 0.048	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.515	2.598	2.683	V
		V_{AGND}	AGND	Bandgap	1.258	1.302	1.355	V
		V_{REFLO}	Ref Low	Vss	Vss	Vss + 0.005	Vss + 0.03	V
0b111	All power settings. Not allowed for 3.3 V	–	–	–	–	–	–	–

7.0.2 DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters ar measured to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 7-1. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor unit value (continuous time)	–	12.2	–	kΩ	
C_{SC}	Capacitor unit value (switched capacitor)	–	80	–	fF	

7.0.3 DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured to 5 V and 3.3 V at 25 °C and are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register.

Table 7-2. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PPOR0R} V_{PPOR1R} V_{PPOR2R}	V_{DD} Value for PPOR Trip (positive ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	2.91 4.39 4.55	–	V V V	V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0} V_{PPOR1} V_{PPOR2}	V_{DD} Value for PPOR Trip (negative ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	2.82 4.39 4.55	–	V V V	
V_{PH0} V_{PH1} V_{PH2}	PPOR Hysteresis PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	– – –	92 0 0	– – –	mV mV mV	
V_{LVD0} V_{LVD1} V_{LVD2} V_{LVD3} V_{LVD4} V_{LVD5} V_{LVD6} V_{LVD7}	V_{DD} Value for LVD Trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.86 2.96 3.07 3.92 4.39 4.55 4.63 4.72	2.92 3.02 3.13 4.00 4.48 4.64 4.73 4.81	2.98[6] 3.08 3.20 4.08 4.57 4.74[7] 4.82 4.91	V V V V V V V V V	
V_{PUMP0} V_{PUMP1} V_{PUMP2} V_{PUMP3} V_{PUMP4} V_{PUMP5} V_{PUMP6} V_{PUMP7}	V_{DD} Value for PUMP Trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.96 3.03 3.18 4.11 4.55 4.63 4.72 4.90	3.02 3.10 3.25 4.19 4.64 4.73 4.82 5.00	3.08 3.16 3.32 4.28 4.74 4.82 4.91 5.10	V V V V V V V V	

Notes
6. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
7. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

7.0.4 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 7-3. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools.
V_{DDLV}	Low V_{DD} for verify	3	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools.
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools.
$V_{DDIWRITE}$	Supply voltage for flash write operation	3.0	–	5.25	V	This specification applies to this device when it is executing internal flash writes.
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	Vss + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} - 1.0	–	V_{DD}	V	
Flash$_{ENPB}$	Flash endurance (per block)	50,000[8]	–	–	–	Erase/write cycles per block.
Flash$_{ENT}$	Flash endurance (total)[9]	1,800,000	–	–	–	Erase/write cycles.
Flash$_{DR}$	Flash data retention	10	–	–	Years	

Notes
8. The 50,000 cycle Flash endurance per block will only be guaranteed if the Flash is operating within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
9. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.
10. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO specifications sections. The I²C GPIO pins also meet the above specs.

7.0.5 DC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 7. DC I²C Specifications

Parameter	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}[10]	Input low level	–	–	0.3 × V_{DD}	V	3.0 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}[10]	Input high level	0.7 × V_{DD}	–	–	V	3.0 V ≤ V_{DD} ≤ 5.25 V

7.1 AC Electrical Characteristics

7.1.1 AC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 7-4. AC Chip Level Specifications

| Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO}	Internal main oscillator frequency	23.4	24	24.6[11]	MHz	Trimmed. Using factory trim values.
F_{CPU1}	CPU frequency (5 V nominal)	0.0914	24	24.6[11,12]	MHz	Trimmed. Using factory trim values. SLIMO mode = 0.
F_{CPU2}	CPU frequency (3.3 V nominal)	0.0914	12	12.3[12,13]	MHz	Trimmed. Using factory trim values.SLIMO mode = 0.
F_{48M}	Digital PSoC block frequency	0	48	49.2[11,12,14]	MHz	Refer to the AC Digital Block Specifications below.
F_{24M}	Digital PSoC block frequency	0	24	24.6[12, 14]	MHz	
F_{32K1}	Internal low speed oscillator frequency	15	32	64	kHz	
F_{32K_U}	Internal low speed oscillator untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the *PSoC Technical Reference Manual* for details on timing this.
DC_{ILO}	Internal Low Speed Oscillator Duty Cycle	20	50	80	%	
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	Multiple (x732) of crystal frequency.
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$T_{PLLSLEWSLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	1700	2620	ms	

Notes
11. 4.75 V < V_{DD} < 5.25 V.
12. Accuracy derived from IMO with appropriate trim for V_{DD} range.
13. 3.0 V < V_{DD} < 3.6 V.
14. See the individual user module data sheets for information on maximum frequencies for user modules.

Table 7-4. AC Chip Level Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
T_{OSACC}	External crystal oscillator startup to 100 ppm	–	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 mW maximum drive level 32.768 kHz crystal. 3.0V £ V_{DD} £ 5.5 V, –40 °C £ T_A £ 85 °C.
T_{XRST}	External reset pulse width	10	–	–	ms	
DC24M	24 MHz duty cycle	40	50	60	%	
Step24M	24 MHz trim step size	–	50	–	kHz	
Fout48M	48 MHz output frequency	46.8	48.0	49.2[11,13]	MHz	Trimmed. Utilizing factory trim values.
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power up.
$T_{POWERUP}$	Time from End of POR to CPU executing code	–	16	100	ms	Power up from 0 V. See the System Resets section of the *PSoC Technical Reference Manual*.
tjit_IMO[15]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	700	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	900		N = 32
	24 MHz IMO period jitter (RMS)	–	100	400		
tjit_PLL [15]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	800	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	1200		N = 32
	24 MHz IMO period jitter (RMS)	–	100	700		

Figure 7-3. PLL Lock Timing Diagram
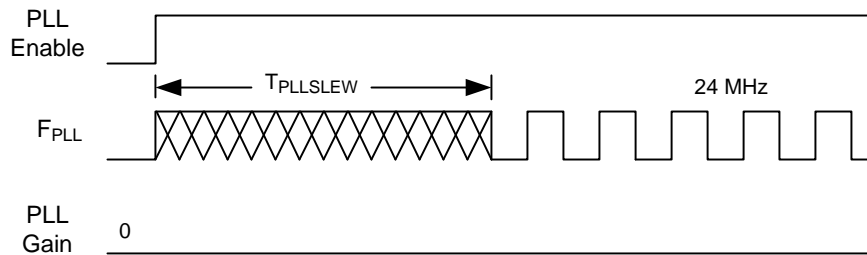
Figure 7-4. PLL Lock for Low Gain Setting Timing Diagram
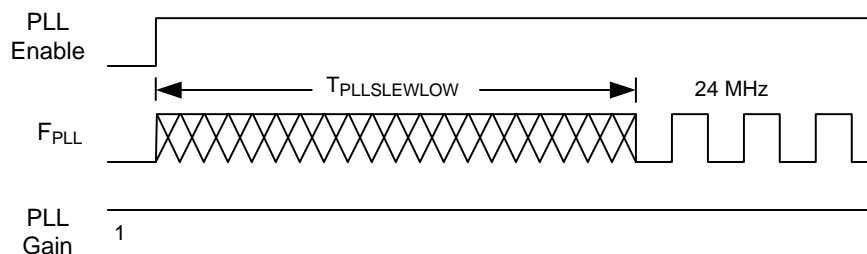
Figure 7-5. External Crystal Oscillator Startup Timing Diagram
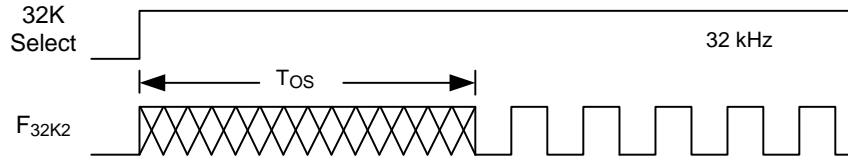
7.0.1 AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C $\leq T_A \leq$ 85 °C, or 3.0 V to 3.6 V and –40 °C $\leq T_A \leq$ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 7-1. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal strong mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% - 90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% - 90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10% - 90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10% - 90%

Figure 1. GPIO Timing Diagram
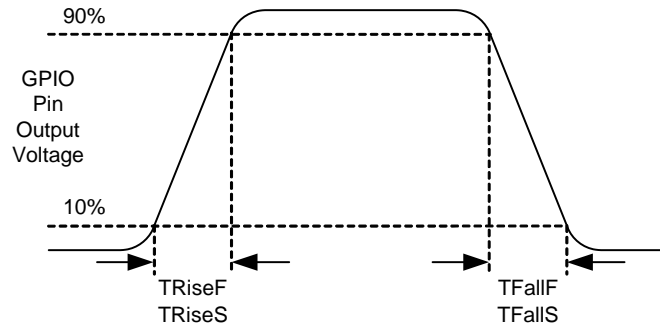
7.0.2 AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C $\leq T_A \leq$ 85 °C, or 3.0 V to 3.6 V and –40 °C $\leq T_A \leq$ 85 °C, respectively. Typical parameters are measured to 5 V and 3.3 V at 25 °C and are for design guidance only. Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3 V.

Table 7-2. 5-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = Low, opamp bias = Low Power = Medium, opamp bias = High Power = High, opamp bias = High	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs	
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, opamp bias = Low Power = Medium, opamp Bias = High Power = High, opamp bias = High	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs	

Note
15. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

**Table 7-2. 5-V AC Operational Amplifier Specifications** (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
SR$_{ROA}$	Rising slew rate (20% to 80%)(10 pF load, unity gain) Power = Low, opamp bias = Low Power = Medium, opamp bias = High Power = High, opamp bias = High	 0.15 1.7 6.5	 – – –	 – – –	 V/μs V/μs V/μs	
SR$_{FOA}$	Falling slew rate (20% to 80%)(10 pF load, unity gain) Power = Low, opamp bias = Low Power = Medium, opamp bias = High Power = High, opamp bias = High	 0.01 0.5 4.0	 – – –	 – – –	 V/μs V/μs V/μs	
BW$_{OA}$	Gain bandwidth product Power = Low, opamp bias = Low Power = Medium, opamp bias = High Power = High, opamp bias = High	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz	
E$_{NOA}$	Noise at 1 kHz (Power = Medium, opamp bias = High)	–	100	–	nV/rt-Hz	

Table 7-3. 3.3-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T$_{ROA}$	Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, opamp bias = Low Power = Low, opamp bias = High	 – –	 – –	 3.92 0.72	 μs μs	
T$_{SOA}$	Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, opamp bias = Low Power = Medium, opamp bias = High	 – –	 – –	 5.41 0.72	 μs μs	
SR$_{ROA}$	Rising slew rate (20% to 80%)(10 pF load, unity gain) Power = Low, opamp bias = Low Power = Medium, opamp bias = High	 0.31 2.7	 – –	 – –	 V/μs V/μs	
SR$_{FOA}$	Falling slew rate (20% to 80%)(10 pF load, unity gain) Power = Low, opamp bias = Low Power = Medium, opamp bias = High	 0.24 1.8	 – –	 – –	 V/μs V/μs	
BW$_{OA}$	Gain bandwidth product Power = Low, opamp bias = Low Power = Medium, opamp bias = High	 0.67 2.8	 – –	 – –	 MHz MHz	
E$_{NOA}$	Noise at 1 kHz (Power = Medium, opamp bias = High)	–	100	–	nV/rt-Hz	

When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 7-6. Typical AGND Noise with P2[4] Bypass
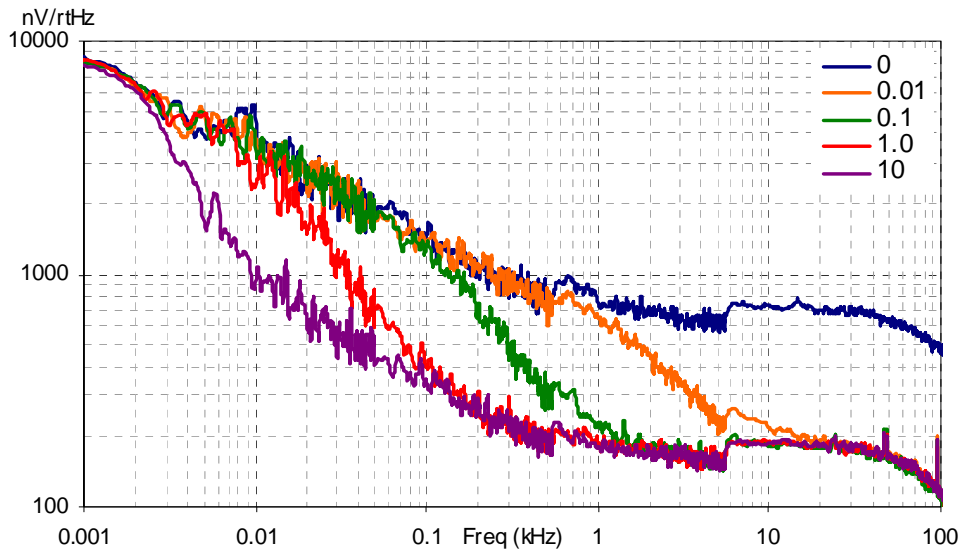
At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 7-7. Typical Opamp Noise
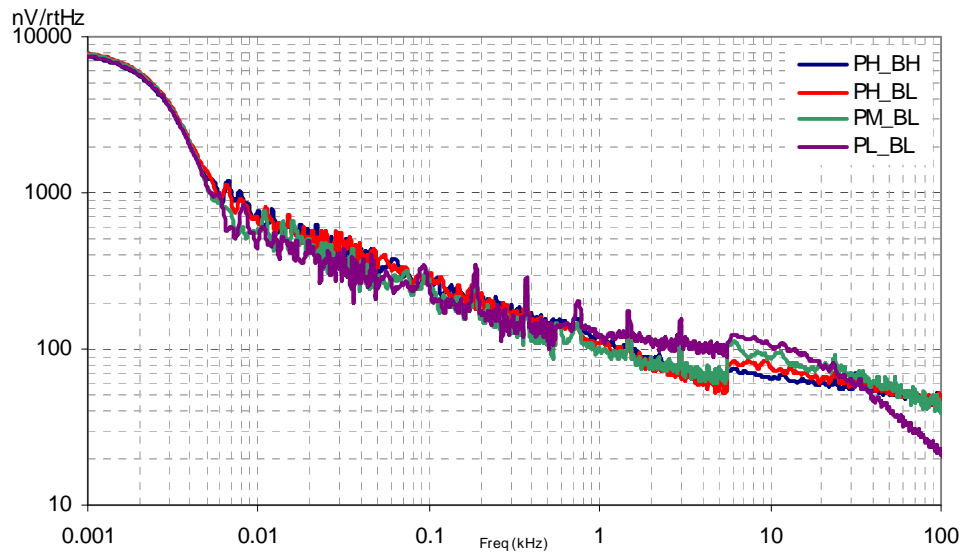
7.4.4 AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and −40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and −40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and −40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V at 25 °C and are for design guidance only.

Table 7-1. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	μs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

7.4.5 AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 8. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
Timer	Input clock frequency					
	No capture, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	No capture, V_{DD} < 4.75 V	–	–	24.6	MHz	
	With capture	–	–	24.6	MHz	
	Capture pulse width	50[16]	–	–	ns	
Counter	Input clock frequency					
	No enable input, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	No enable input, V_{DD} < 4.75 V	–	–	24.6	MHz	
	With enable input	–	–	24.6	MHz	
	Enable input pulse width	50[16]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[16]	–	–	ns	
	Disable mode	50[16]	–	–	ns	
	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	24.6	MHz	
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_negated between transmissions	50[16]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	

Note
16. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

7.4.6 AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 7-2. 5-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF Load Power = Low Power = High	– –	– –	2.5 2.5	μs μs	
T_{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF Load Power = Low Power = High	– –	– –	2.2 2.2	μs μs	
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100 pF Load Power = Low Power = High	0.65 0.65	– –	– –	V/μs V/μs	
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100 pF Load Power = Low Power = High	0.65 0.65	– –	– –	V/μs V/μs	
BW_{OB}	Small signal bandwidth, 20 mV$_{pp}$, 3 dB BW, 100 pF Load Power = Low Power = High	0.8 0.8	– –	– –	MHz MHz	
BW_{OB}	Large signal bandwidth, 1 V$_{pp}$, 3 dB BW, 100 pF Load Power = Low Power = High	300 300	– –	– –	kHz kHz	

Table 7-3. 3.3-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF Load Power = Low Power = High	– –	– –	3.8 3.8	μs μs	
T_{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF Load Power = Low Power = High	– –	– –	2.6 2.6	μs μs	
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100 pF Load Power = Low Power = High	0.5 0.5	– –	– –	V/μs V/μs	
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100 pF Load Power = Low Power = High	0.5 0.5	– –	– –	V/μs V/μs	
BW_{OB}	Small signal bandwidth, 20 mV$_{pp}$, 3 dB BW, 100 pF Load Power = Low Power = High	0.7 0.7	– –	– –	MHz MHz	
BW_{OB}	Large signal bandwidth, 1 V$_{pp}$, 3 dB BW, 100 pF Load Power = Low Power = High	200 200	– –	– –	kHz kHz	

Note
17. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

7.4.7 AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C $\leq T_A \leq$ 85 °C, or 3.0 V to 3.6 V and –40 °C $\leq T_A \leq$ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 7-4. 5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High period	20.6	–	5300	ns	
–	Low period	20.6	–	–	ns	
–	Power up IMO to switch	150	–	–	μs	

Table 7-5. 3.3V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1[18]	0.093	–	12.3	MHz	
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater[19]	0.186	–	24.6	MHz	
–	High period with CPU clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU clock divide by 1	41.7	–	–	ns	
–	Power up IMO to switch	150	–	–	μs	

7.4.8 AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C $\leq T_A \leq$ 85 °C, or 3.0 V to 3.6 V and –40 °C $\leq T_A \leq$ 85 °C, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 7-6. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall time of SCLK	1	–	20	ns	
T_{SSCLK}	Data setup time to falling edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash erase time (block)	–	10	–	ms	
T_{WRITE}	Flash block write time	–	10	–	ms	
T_{DSCLK}	Data out delay from falling edge of SCLK	–	–	45	ns	$V_{DD} > 3.6$
T_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	$3.0 \leq V_{DD} \leq 3.6$
$T_{ERASEALL}$	Flash erase time (Bulk)	–	95	–	ms	Erase all blocks and protection fields at once.
$T_{PROGRAM\_HOT}$	Flash block erase + flash block write time	–	–	80[20]	ms	$0 °C \leq T_J \leq 100 °C$
$T_{PROGRAM\_COLD}$	Flash block erase + flash block write time	–	–	160[20]	ms	$–40 °C \leq T_J \leq 0 °C$

Notes
18. Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
19. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.
20. For the full industrial range, the user must employ a Temperature Sensor User Module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.

7.4.9 AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\ °C \le T_A \le 85\ °C$, or 3.0 V to 3.6 V and $-40\ °C \le T_A \le 85\ °C$, respectively. Typical parameters are measured at 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 7-7. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard-Mode		Fast-Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	μs	
T_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	μs	
$T_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	μs	
$T_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	μs	
$T_{HDDATI2C}$	Data hold time	0	–	0	–	μs	
$T_{SUDATI2C}$	Data Setup time	250	–	100[21]	–	ns	
$T_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	μs	
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	μs	
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns	

Figure 7-8. Definition for Timing for Fast-/Standard-Mode on the I²C Bus
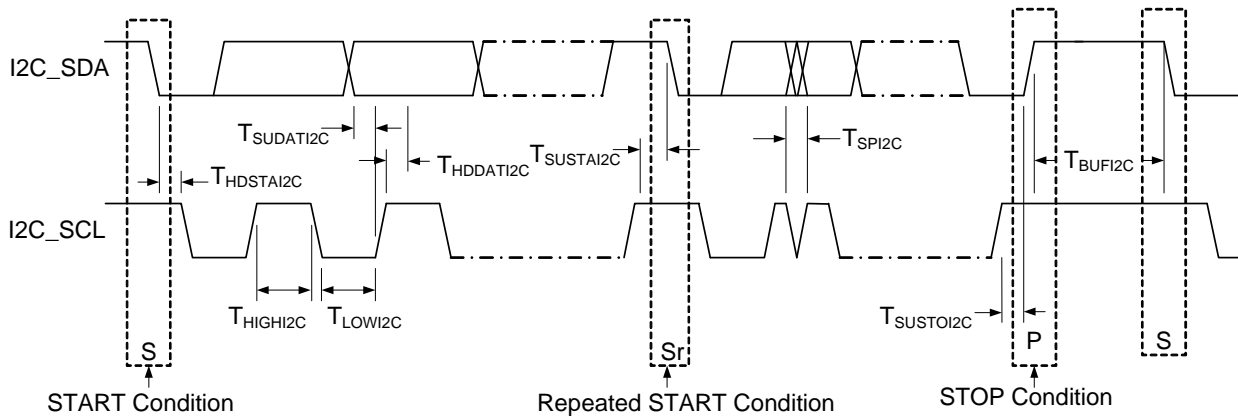
Note

21. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $t_{SU;DAT} \ge 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

8. Packaging Information

This section illustrates the packaging specifications for the CY8CLED08 EZ-Color device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

8.1 Packaging Dimensions

Figure 8-1. 48-Pin (7 × 7 × 1.0 mm) QFN (Sawn)

TOP VIEW

7.00±0.100

7.00±0.100

PIN 1 DOT
LASER MARK

48   37
1   36
12   25
13   24

SIDE VIEW

0.900±0.100

0.200 REF.

0.020 +0.025 -0.00

0.08 C

SEATING PLANE

BOTTOM VIEW

5.100 REF
0.50 PITCH
PIN1 ID
R 0.20

0.25 +0.05 -0.07

37
36
5.100 REF
25
24
0.40±0.10

1
0.45
5.500±0.100
12
13
5.500±0.100

SOLDERABLE EXPOSED PAD

NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *E

Important Note

For information on the preferred dimensions for mounting QFN packages, see the following Application Note at *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at http://www.amkor.com.

Pinned vias for thermal conduction are not required for the low-power device.

8.1 Thermal Impedances

Table 8-1. Thermal Impedances per Package

Package	Typical θ_{JA}[22]
48-pin QFN[23]	18 °C/W

8.2 Capacitance on Crystal Pins

Table 8-2. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
48-pin QFN	2.3 pF

8.3 Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 8-3. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
48-pin QFN	260 °C	30 s

Notes
22. $T_J = T_A + POWER \times \theta_{JA}$
23. To achieve the thermal impedance specified for the QFN package, refer to *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at http://www.amkor.com.

9. Development Tool Selection

This section presents the development tools available for all current PSoC based devices including the CY8CLED08 EZ-Color family.

9.1 Software Tools

9.1.1 PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com and includes a free C compiler.

9.1.2 PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube in-circuit emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

9.2 Hardware Tools

9.2.1 In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of the USB port. The base unit is universal and will operate with all PSoC based devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

9.2.2 I^2C to USB Bridge

The I^2C to USB Bridge is a quick and easy link from any design or application's I^2C bus to a PC via USB for design testing, debugging and communication.

9.3 Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

9.3.1 CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

■ MiniProg Programming Unit

■ MiniEval Socket Programming and Evaluation Board

■ 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample

■ 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample

■ PSoC Designer Software CD

■ Getting Started Guide

■ USB 2.0 Cable

9.3.2 CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

■ Evaluation Board with LCD Module

■ MiniProg Programming Unit

■ 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)

■ PSoC Designer Software CD

■ Getting Started Guide

■ USB 2.0 Cable

9.4 Device Programmers

All device programmers are sold at the Cypress Online Store.

9.4.1 CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

■ Modular Programmer Base

■ 3 Programming Module Cards

■ MiniProg Programming Unit

■ PSoC Designer Software CD

■ Getting Started Guide

■ USB 2.0 Cable

9.4.2 CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment. **Note** CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

■ CY3207 Programmer Unit

■ PSoC ISSP Software CD

■ 110 ~ 240V Power Supply, Euro-Plug Adapter

■ USB 2.0 Cable

9.5 Accessories (Emulation and Programming)

Table 9. Emulation and Programming Accessories

Part #	Pin Package	Flex-Pod Kit[24]	Foot Kit[25]	Adapter[26]
CY8CLED08-48LTXI	48-pin QFN	CY3250-LED08QFN	CY3250-48QFN-FK	Adapters can be found at http://www.emulation.com.

Notes
24. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
25. Foot kit includes surface mount feet that can be soldered to the target PCB.
26. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

10. Ordering Information

10.1 Key Device Features

The following table lists the CY8CLED08 EZ-Color devices' key package features and ordering codes.

Table 10. Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	RAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks (Rows of 4)	Analog Blocks (Columns of 3)	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
48-pin (7 × 7) QFN (Sawn)	CY8CLED08-48LTXI	16 K	256	Yes	−40 °C to +85 °C	8	12	44	12	4	Yes
48-pin (7 × 7) QFN (Tape and Reel) (Sawn)	CY8CLED08-48LTXIT	16 K	256	Yes	−40 °C to +85 °C	8	12	44	12	4	Yes

10.2 Ordering Code Definitions

CY 8 C LED xx - xx xxxx

Package Type: Thermal Rating:
  LTX = QFN Pb-free   I = Industrial

Pin Count

Part Number

LED Family Code

Technology Code: C = CMOS

Marketing Code: 8 = Cypress PSoC

Company ID: CY = Cypress
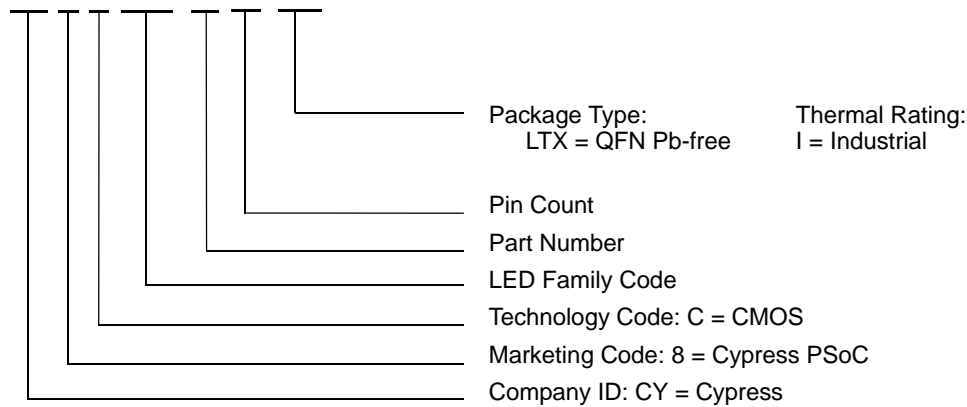
11. Acronyms

Table 11-1 lists the acronyms that are used in this document.

Table 11-1. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MAC	multiply-accumulate
ADC	analog-to-digital converter	MIPS	million instructions per second
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual-in-line package
CPU	central processing unit	PLL	phase-locked loop
CRC	cyclic redundancy check	POR	power-on reset
CT	continuous time	PPOR	precision power on reset
DAC	digital-to-analog converter	PRS	pseudo-random sequence
DC	direct current	PSoC®	Programmable System-on-Chip
DTMF	dual-tone multi-frequency	PWM	pulse-width modulator
ECO	external crystal oscillator	QFN	quad flat no leads
EEPROM	electrically erasable programmable read-only memory	RTC	real time clock
GPIO	general purpose I/O	SAR	successive approximation
I/O	input/output	SROM	supervisory read only memory
ICE	in-circuit emulator	SC	switched capacitor
IDE	integrated development environment	SMP	switch mode pump
ILO	internal low speed oscillator	SPI	serial peripheral interface
IMO	internal main oscillator	SRAM	static random access memory
IrDA	infrared data association	SSOP	shrink small-outline package
ISSP	in-system serial programming	UART	universal asynchronous receiver / transmitter
LCD	liquid crystal display	USB	universal serial bus
LED	light-emitting diode	WDT	watchdog timer
LPC	low power comparator	XRES	external reset
LVD	low-voltage detect		

12. Reference Documents

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 (001-14503)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at http://www.amkor.com.

13. Document Conventions

13.1 Units of Measure

Table 13-1 lists the units of measure.

Table 13-1. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
dB	decibels	µs	microseconds
ºC	degree Celsius	ms	milliseconds
fF	femtofarads	ns	nanoseconds
pF	picofarads	ps	picoseconds
kHz	kilohertz	µV	microvolts
MHz	megahertz	mV	millivolts
rt-Hz	root hertz	mVpp	millivolts peak-to-peak
kΩ	kilohms	nV	nanovolts
µA	microamperes	V	volts
mA	milliamperes	µW	microwatts
nA	nanoamperes	W	watts
pA	pikoamperes	mm	millimeter
µF	microfarads	ppm	parts per million
µH	microhenry	%	percent

13.2 Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, 01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.

active high	1. A logic signal having its asserted state as the logic 1 state.
	2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are switched capacitor (SC) and continuous time (CT) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz.
	2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value.
	2. The amount by which the average of a set of values departs from a reference value.
	3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.

block	1. A functional unit that performs a single function, such as an oscillator.
	2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written.
	2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device.
	3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns.
	2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0].
	3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to '1'.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.

External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I^2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I^2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the *slave device*.
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.

mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
Phase-locked loop (PLL)	An electronic circuit that controls an *oscillator* so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
Power-on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is a type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse-width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.

| slave device | A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device. |

SRAM — An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.

SROM — An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.

stop bit — A signal following a character or block that prepares the receiving device to receive the next character or block.

synchronous —
  1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal.
  2. A system whose operation is synchronized by a clock signal.

tri-state — A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.

UART — A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.

user modules — Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level *Application Programming Interface (API)* for the peripheral function.

user space — The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.

V_{DD} — A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.

V_{SS} — A name for a power net meaning "voltage source." The most negative power supply signal.

watchdog timer — A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

14. Document History Page

Document Title: CY8CLED08 EZ-Color™ HB LED Controller Document Number: 001-12981				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	1148504	SFVTMP3	06/13/2007	New document (revision **).
*A	1391163	AESA	See ECN	Added 28 pin SSOP
*B	2763950	DPT	10/01/0209	Added 48QFN package diagram (Sawn) Saw Marketing part number in ordering information.
*C	2794355	XBM	10/28/2009	Added "Contents" on page 3 Updated "Development Tools" on page 7. Corrected FCPU1 and FCPU2 parameters in "AC Chip Level Specifications" on page 31.
*D	2819954	CGX	12/02/2009	Corrected package diagram for 28-Pin (210-Mil) SSOP (Figure 8-1)
*E	2850593	FRE	01/14/2010	Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Replaced TRAMP (time) with SRPOWER_UP (slew rate) specification. Added note to Flash Endurance specification. Added IOH, IOL, DCILO, F32K_U, TPOWERUP, TERASEALL, TPROGRAM_HOT, and TPROGRAM_COLD specifications. Corrected the Pod Kit part numbers. Updated Development Tool Selection. Updated copyright and Sales, Solutions, and Legal Information URLs. Updated 28-Pin (210-Mil) SSOP package diagram.
*F	2896238	CGX	03/19/10	Updated ordering information table. Removed part numbers CY8CLED08-48LFXI and CY8CLED08-48LFXIT Updated copyright section. Updated package diagram for spec 51-85061
*G	2903043	NJF	04/01/2010	Updated Cypress website links Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters Removed sections "Third Party Tools" and "Build a PSoC Emulator"
*H	3053097	CGX	10/08/2010	Removed obsolete parts.
*I	3114945	NJF	12/19/10	Added DC I^{2}C Specifications table. Added F_{32K_U} max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated DC Analog reference, DC Analog output buffer specifications and DC operational amplifier specifications tables. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I^{2}C Timing Diagram. They were updated for clearer understanding. Updated Figure 6-6 as the labelling for y-axis was incorrect. Template and styles update.
*J	3284963	DIVA	07/08/11	Updated Getting Started, Development Tools, and Designing with PSoC Designer. Removed obsolete kits. Removed references to 48-pin SSOP and 28-pin SSOP.
*K	3474429	MKKU	01/04/12	Updated template No change in content

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