ANALOG DEVICES

HMC662LP3E

v05.0914

RoHS EARTH FRIENDLY

54 dB, LOGARITHMIC DETECTOR, 8 - 30 GHz

Typical Applications

The HMC662LP3E is ideal for:

- Point-to-Point Microwave Radio
- VSAT
- Wideband Power Monitoring
- Receiver Signal Strength Indication (RSSI)
- Test & Measurement

Features

Wide Input Bandwidth: 8 to 30 GHz

Wide Dynamic Range: >54 dB up to 28 GHz

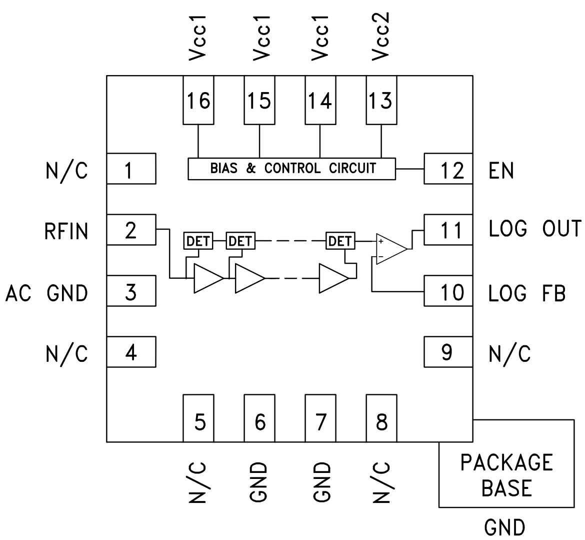
Single Positive Supply: +3.3V

Excellent Stability Over Temperature

Fast Rise/Fall Time: 5ns / 10ns

16 Lead 3x3mm SMT Package: 9mm²

Functional Diagram



General Description

The HMC662LP3E Logarithmic Detector converts RF signals at its input, to a proportional DC voltage at its output. The HMC662LP3E employs successive compression topology which delivers high dynamic range over a wide input frequency range. As the input power is increased, successive amplifiers move into saturation one by one creating an approximation of the logarithm function. The output of a series of detectors is summed, converted into the voltage domain and buffered to drive the LOG OUT output. The HMC662LP3E provides a nominal logarithmic slope of +13 mV/dB and an intercept of -127 dBm at 18 GHz. Ideal as a log detector for high volume micro-wave radio and VSAT applications, the HMC662LP3E is housed in a compact 3x3 mm RoHS compliant SMT plastic package.

Electrical Specifications, T_A = +25 C Vcc1 = Vcc2 = +3.3V

Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Input Frequency[1]	10	14	18	22	28	GHz
±3 dB Dynamic Range	59	60	63	64	54	dB
±3 dB Dynamic Range Center	-23	-24	-24	-25	-17	dBm
Log Error Over Temperature (-40 to +85)	±1	±1	±1	±2	±3	dB
Output Intercept	-120	-125	-127	-130	-113	dBm
Output Slope	14.6	13.7	13.3	13.2	14	mV/dB

[1] Video output load should be 1K Ohm or higher.

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Application Support: Phone: 1-800-ANALOG-D

HMC662* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMC662LP3E Evaluation Board

DOCUMENTATION

Data Sheet

- HMC662 Data Sheet

REFERENCE MATERIALS

Quality Documentation

- Package/Assembly Qualification Test Report: 16L 3x3mm QFN Package (QTR: 11003 REV: 02)
- Package/Assembly Qualification Test Report: LP2, LP2C, LP3, LP3B, LP3C, LP3D, LP3F, LP3G (QTR: 2014-0364)

DESIGN RESOURCES

- HMC662 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMC662 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

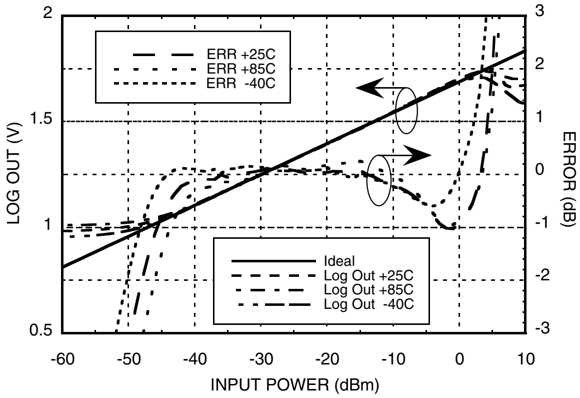
Submit feedback for this data sheet.

Electrical Specifications, (continued)

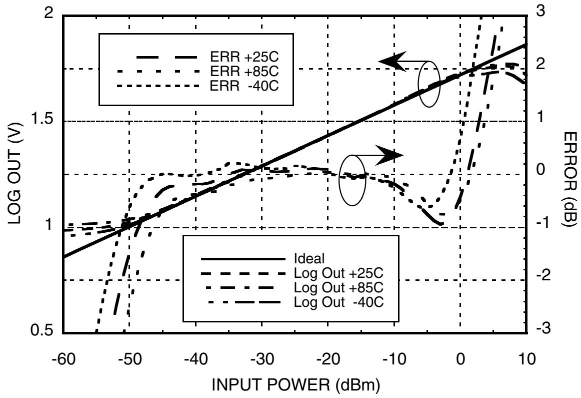
Parameter	Conditions	Min.	Typ.	Max.	Units
LOGOUT Interface					
Output Voltage Range		0.9		1.8	V
Output Rise Time [1] / Fall Time [2]	f = 10 GHz		5 / 10		ns
Power Down (EN) Interface					
Voltage Range for Normal Mode		0.8 x Vcc		Vcc	V
Voltage Range for Powerdown Mode		0		0.1 x Vcc	V
Power Supply (Vcc1, Vcc2)					
Operating Voltage Range		3.15	3.3	3.45	V
Supply Current in Normal Mode			88		mA
Supply Current in Power Down Mode			3		mA

[1] 0 dBm Input Pulsed; measured from 10% to 90%
[2] 0 dBm Input Pulsed; measured from 90% to 10%

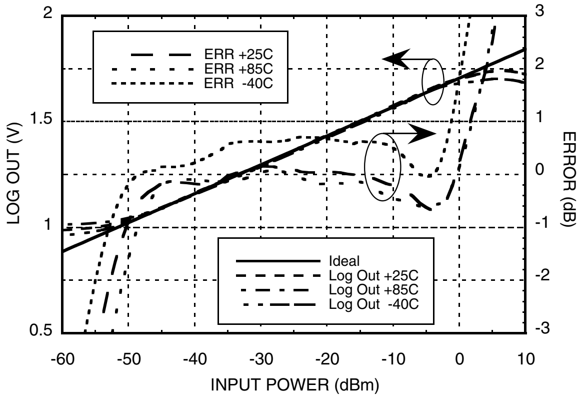
LOG OUT & Error vs. Input Power, Fin = 8 GHz



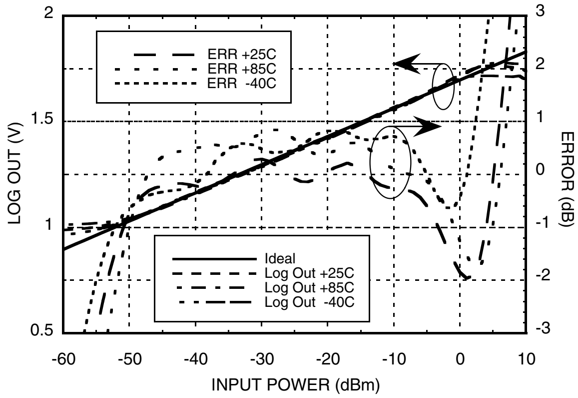
LOG OUT & Error vs. Input Power, Fin = 10 GHz



LOG OUT & Error vs. Input Power, Fin = 14 GHz



LOG OUT & Error vs. Input Power, Fin = 18 GHz



Unless otherwise noted: Vcc1, Vcc2 = +3.3V, T_A = +25 °C

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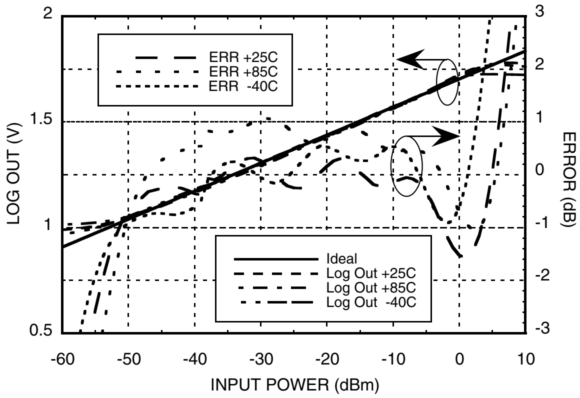
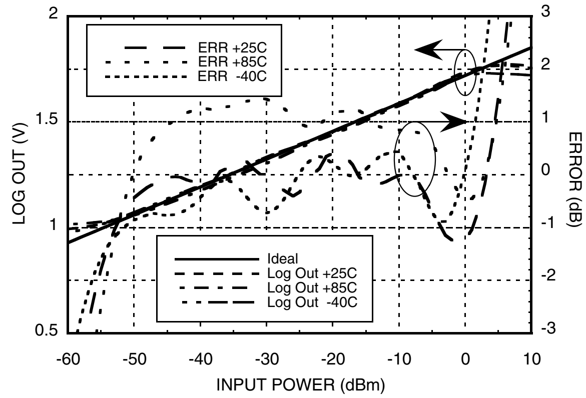
54 dB, LOGARITHMIC DETECTOR, 8 - 30 GHz

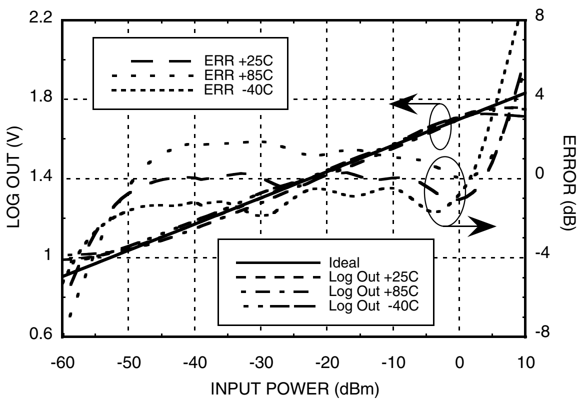
LOG OUT & Error vs. Input Power, Fin = 20 GHz



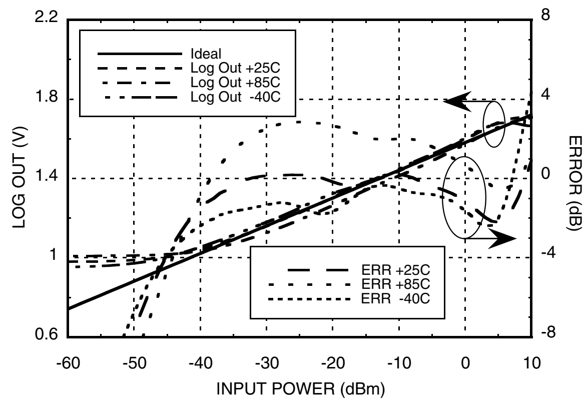
LOG OUT & Error vs. Input Power, Fin = 22 GHz



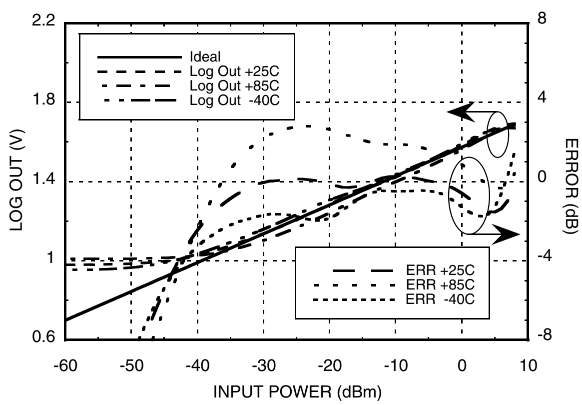
LOG OUT & Error vs. Input Power, Fin = 24 GHz



LOG OUT & Error vs. Input Power, Fin = 28 GHz



LOG OUT & Error vs. Input Power, Fin = 30 GHz



Unless otherwise noted: Vcc1, Vcc2 = +3.3V, T_A = +25 °C

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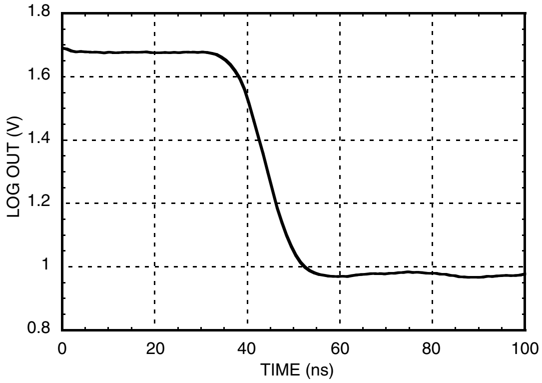
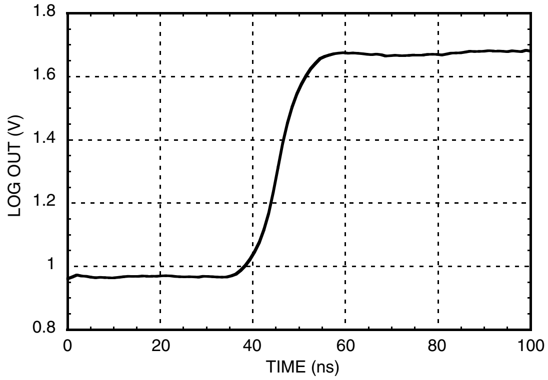
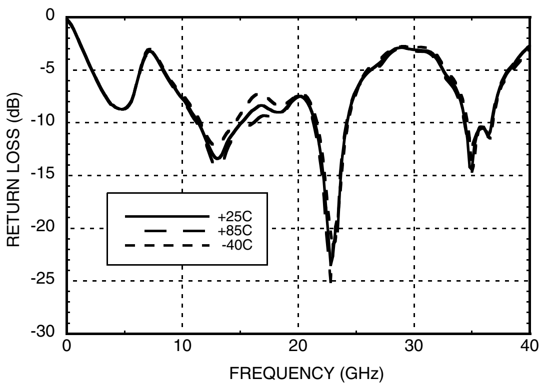
Fall Time @ 10 GHz @ 0 dBm



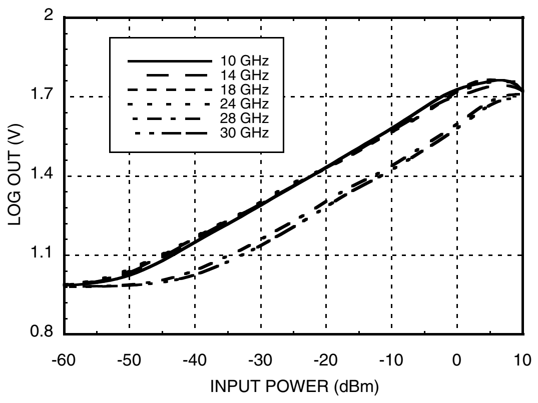
Rise Time @ 10 GHz @ 0 dBm



Input Return Loss



LOG OUT vs. Frequency



Unless otherwise noted: Vcc1, Vcc2 = +3.3V, T_A = +25 °C

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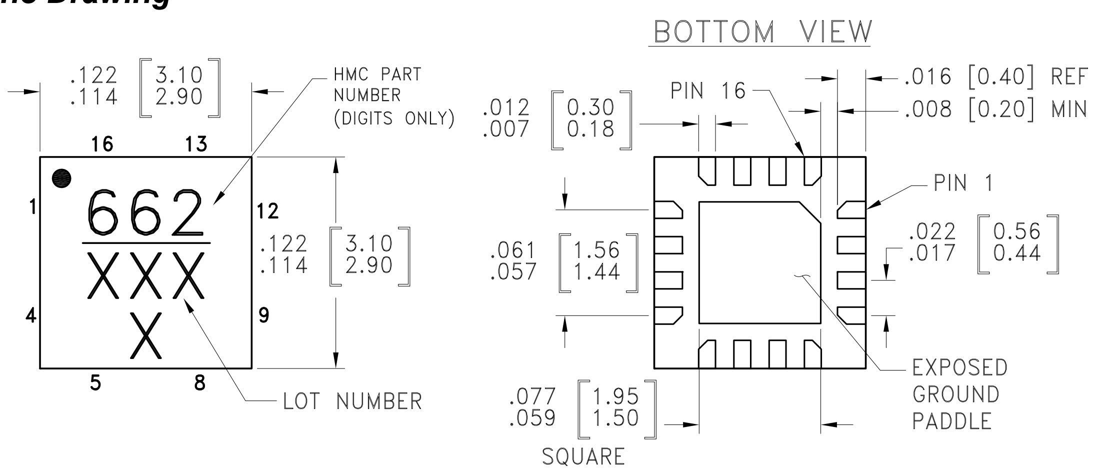
54 dB, LOGARITHMIC DETECTOR, 8 - 30 GHz

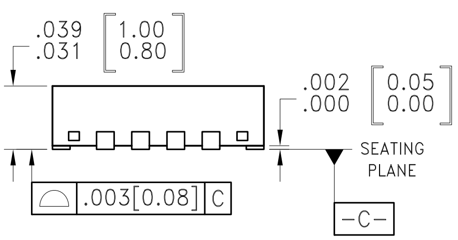
Absolute Maximum Ratings

EN	+3.6V
Vcc1. Vcc2	+3.6V
RF Input Power	+12 dBm
Junction Temperature	125 °C
Continuous Pdiss (T = 85°C) (Derate 12.63 mW/°C above 85°C)	0.51W
Thermal Resistance (R_{th}) (junction to ground paddle)	15.29 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 0

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing





NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HMC APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC662LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	662 XXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

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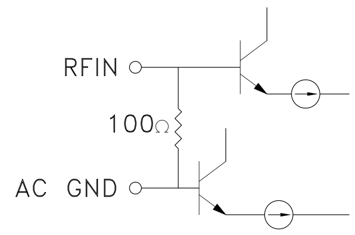
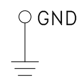
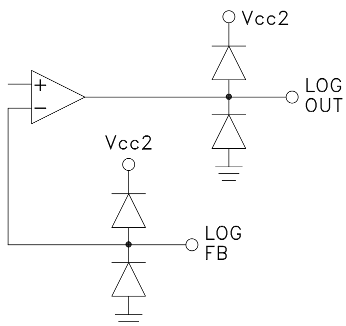
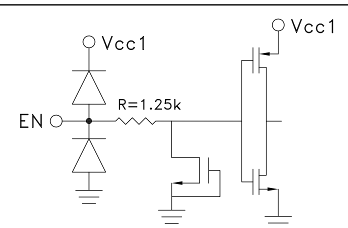
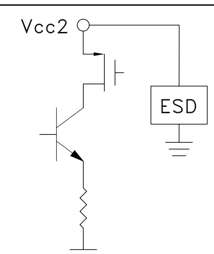
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9	N/C	No connection necessary. These pins may be connected to RF/DC ground without affecting performance.	
2	RFIN	RF input pin.	
3	AC GND	External capacitor to ground is required. See application circuit.	
6, 7	GND	These pins and the exposed package bottom must be connected to a high quality RF/DC ground.	
10, 11	LOG FB, LOG OUT	Log out and feedback. These pins should be shorted to each other (see application circuit). Log out load should be at least 1K Ohm or higher.	
12	EN	Enable pin connected to Vcc1 or Vcc2 for normal operation. Total supply current reduced to less than 3mA when EN is set to 0V.	
13	Vcc2	Bias Supply. Connect supply voltage to this pin with appropriate filtering. To ensure proper start-up supply rise time should be faster than 100usec	

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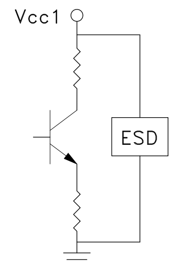
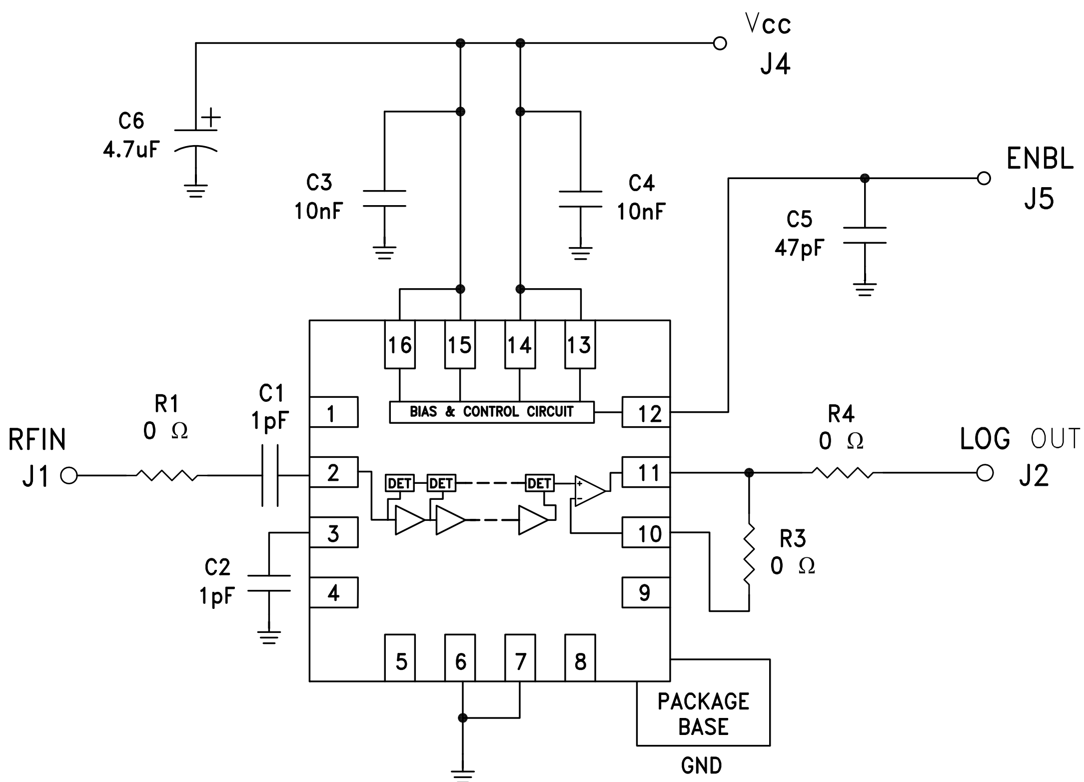
Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
14 - 16	Vcc1	Bias Supply. Connect supply voltage to these pins with appropriate filtering. To ensure proper start-up supply rise time should be faster than 100usec	

Application & Evaluation PCB Schematic



Note1: C1 and C2 should be placed as close to the package as possible.

Note2: Log out load should be 1K Ohm or higher.

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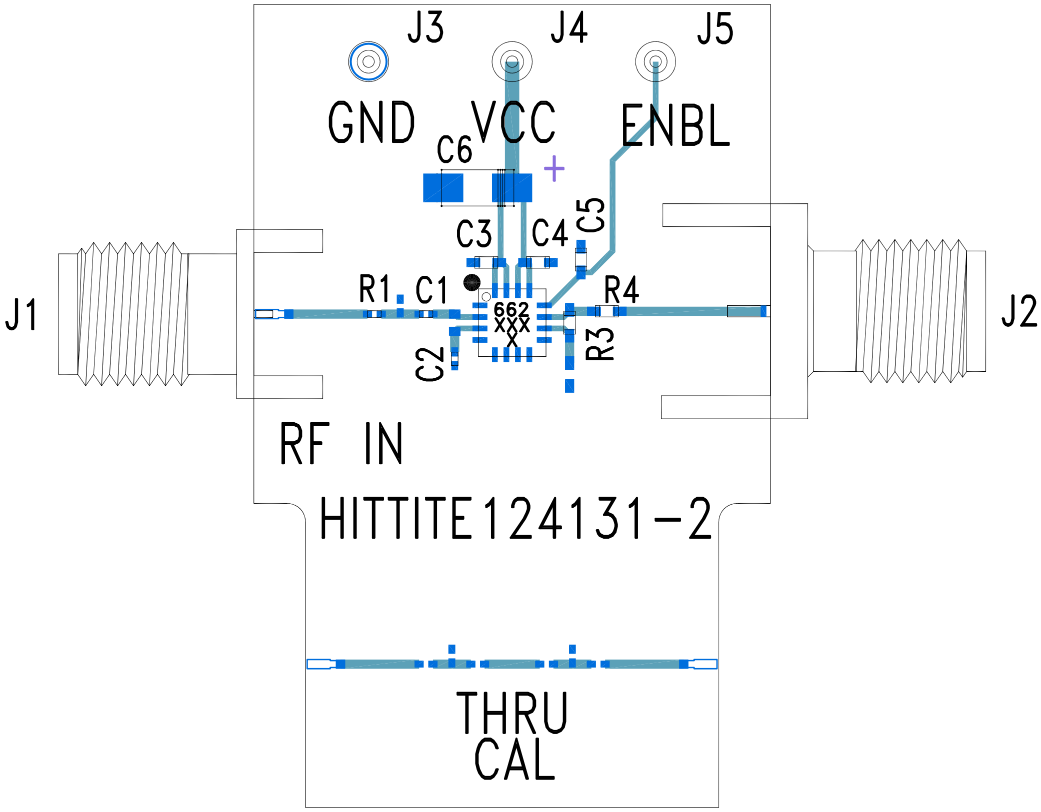
Evaluation PCB



List of Materials for Evaluation PCB 124133 [1]

Item	Description
J1	K-Type Connector
J2	SMA Connector
J3 - J5	DC Pin
C1, C2	1 pF Capacitor, 0201 Pkg.
C3, C4	10 nF Capacitor, 0402 Pkg.
C5	47 pF Capacitor, 0402 Pkg.
C6	4.7 µF Tantalum Capacitor, CASE A Pkg.
R1	0 Ω Resistor, 0201 Pkg.
R3, R4	0 Ω Resistor, 0402 Pkg.
U1	HMC662LP3E Log Detector
PCB [2]	124131 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25 FR

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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