±6A Monolithic Synchronous Step-Down Regulator for DDR Termination

FEATURES

- **±6A Output Current**
- **2.25V to 5.5V Input Voltage Range**
- **±10mV Output Voltage Accuracy**
- **Optimized for Low Output Voltages Down to 0.5V**
- **High Efficiency**
- Integrated Buffer for VTTR = VDDQIN • 0.5
- Shutdown Current: <1µA
- Adjustable Switching Frequency: Up to 4MHz
- Optional Internal Compensation
- Internal Soft-Start
- Power Good Status Output
- Input Overvoltage Protected
- Thermally Enhanced 24-Pin 3mm × 5mm QFN Package

APPLICATIONS

- DDR Termination
- Supports DDR, DDR2 and DDR3 Standards
- Tracking Supplies

DESCRIPTION

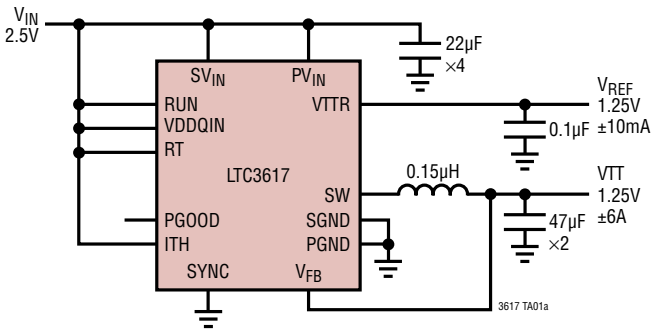
The LTC®3617 is a high efficiency monolithic synchronous buck regulator utilizing a current mode, constant frequency architecture. It operates from an input voltage range of 2.25V to 5.5V and provides a regulated output voltage equal to 0.5 • VDDQIN while sourcing and sinking up to 6A of load current. An internal amplifier provides a VTTR output voltage equal to 0.5 • VDDQIN with an output current capability of ±10mA.

The operating frequency is externally programmable up to 4MHz, allowing the use of small surface mount inductors. For switching-noise-sensitive applications, the LTC3617 can be synchronized to an external clock up to 4MHz.

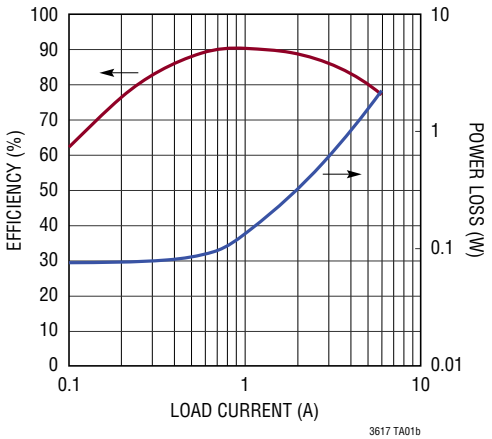
Forced continuous mode operation in the LTC3617 reduces noise and RF interference. Adjustable external compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

The internal synchronous switch increases efficiency and eliminates the need for an external catch diode, minimizing external component count and board space. The LTC3617 is offered in a leadless 24-pin 3mm × 5mm thermally enhanced QFN package.

TYPICAL APPLICATION



Efficiency and Power Loss vs Load Current

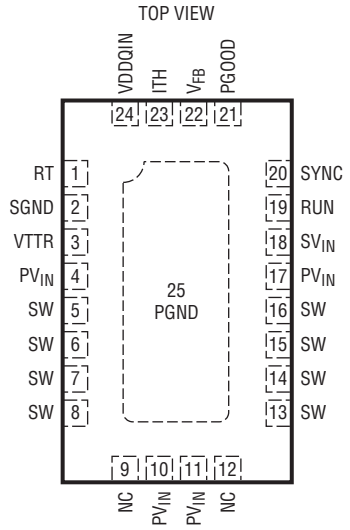


ABSOLUTE MAXIMUM RATINGS

(Note 1)

PV_{IN}, SV_{IN} Voltages ..... –0.3V to 6V
SW Voltage ..... –0.3V to (PV_{IN} + 0.3V)
ITH, RT, SYNC Voltages ..... –0.3V to (SV_{IN} + 0.3V)
VTTR, RUN, V_{FB} Voltages ..... –0.3V to (SV_{IN} + 0.3V)
VDDQIN, PGOOD Voltages ..... –0.3V to 6V
Operating Junction Temperature Range
(Notes 2, 8) ..... –40°C to 125°C
Storage Temperature ..... –65°C to 150°C

PIN CONFIGURATION



UDD PACKAGE
24-LEAD (3mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 25) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3617EUDD#PBF	LTC3617EUDD#TRPBF	LFXC	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3617IUDD#PBF	LTC3617IUDD#TRPBF	LFXC	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. PV_{IN} = SV_{IN} = 3.3V, RT = SV_{IN} unless otherwise specified (Notes 1, 2, 8).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Operating Range		●	2.25		5.5	V
V_{UVLO}	Undervoltage Lockout Threshold	SV_{IN} Ramping Down SV_{IN} Ramping Up	● ●	1.7		 2.2	V V
V_{OVLO}	Overvoltage Lockout Threshold	SV_{IN} Ramping Up Hysteresis			6.5 250	7	V mV
VTTR	VTTR Output Voltage with Line and Load Regulation	VDDQIN = 1.5V, Load = ±10mA	●	0.49 • VDDQIN	0.5 • VDDQIN	0.51 • VDDQIN	V
	VTTR Maximum Output Current					±10	mA
V_{FB}	Feedback Voltage Accuracy	VDDQIN = 1.5V (Note 3)	●	VTTR – 10	VTTR	VTTR + 10	mV
I_{FB}	Feedback Input Current	V_{FB} = 0.75V	●			±30	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. PV_{IN} = SV_{IN} = 3.3V, RT = SV_{IN} unless otherwise specified (Notes 1, 2, 8).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\Delta V_{FB(LINEREG)}$	Feedback Voltage Line Regulation	SV_{IN} = PV_{IN} = 2.25V to 5.5V, VDDQIN = 1.5V (Notes 3, 4)	●			0.2	%/V
$\Delta V_{FB(LOADREG)}$	Feedback Voltage Load Regulation	ITH from 0.5V to 0.9V (Notes 3, 4) V_{ITH} = SV_{IN} (Note 5)				0.25 0.25	% %
I_Q	Input DC Supply Current Active Mode Shutdown	 V_{FB} = 0.6V, VDDQIN = 1.5V (Note 6) SV_{IN} = PV_{IN} = 5.5V, V_{RUN} = 0V			 1100 0.1	 1	 µA µA
$R_{DS(ON)}$	Top Switch On-Resistance	PV_{IN} = 3.3V			35		mΩ
	Bottom Switch On-Resistance	PV_{IN} = 3.3V			25		mΩ
I_{LIM}	Top Switch Positive Peak Current Limit	Sourcing (Note 7), V_{FB} = 0.5V		8	10	14	A
	Top Switch Negative Peak Current Limit	Sinking (Note 7)		–12	–8	–5	A
$g_{m(EA)}$	Error Amplifier Transconductance	–5µA < I_{ITH} < 5µA (Note 4)			200		µS
I_{EAO}	Error Amplifier Maximum Output Current	(Note 4)			±30		µA
t_{SS}	Internal Soft-Start Time	V_{FB} from 0.075V to 0.675V, VDDQIN = 1.5V		0.4	0.85	2	ms
f_{OSC}	Oscillator Frequency Internal Oscillator Frequency	R_T = 370k V_{RT} = SV_{IN}	● ●	0.8 1.8	1 2.25	1.2 2.7	MHz MHz
f_{SYNC}	Synchronization Frequency Range			0.3		4	MHz
V_{SYNC}	SYNC Input Threshold High Voltage SYNC Input Threshold Low Voltage			1.2		 0.3	V V
$I_{SW(LKG)}$	Switch Leakage Current	SV_{IN} = PV_{IN} = 5.5V, V_{RUN} = 0V			0.1	1	µA
PGOOD	Power Good Voltage Windows	VDDQIN = 1.5V, Entering Window V_{FB} Ramping Up V_{FB} Ramping Down		 –3.5 3.5	 –5 5	 	 % %
		VDDQIN = 1.5V, Leaving Window V_{FB} Ramping Up V_{FB} Ramping Down		 	 8 –8	 10 –10	 % %
t_{PGOOD}	Power Good Blanking Time	Entering and Leaving Window		70	105	140	µs
R_{PGOOD}	Power Good Pull-Down On-Resistance			8	17	33	Ω
V_{RUN}	RUN voltage	Input High Input Low	● ●	1		 0.4	V V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3617 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3617E is guaranteed to meet performance specifications over the 0°C to 85°C operating junction temperature range. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3617I is guaranteed to meet specifications over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: This parameter is tested in a feedback loop which servos V_{FB} to the midpoint for the error amplifier (V_{ITH} = 0.75V).

Note 4: External compensation on ITH pin.

Note 5: Tying the ITH pin to SV_{IN} enables the internal compensation.

Note 6: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

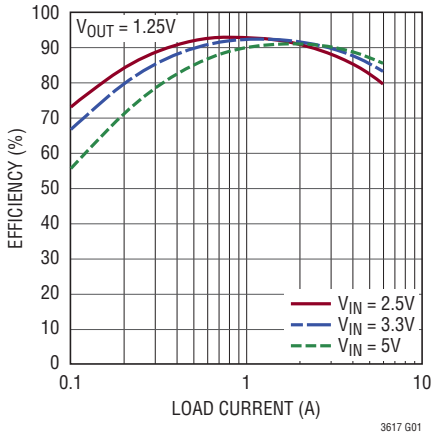
Note 7: In sourcing mode the average output current is flowing out of the SW pin. In sinking mode the average output current is flowing into the SW Pin.

Note 8: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

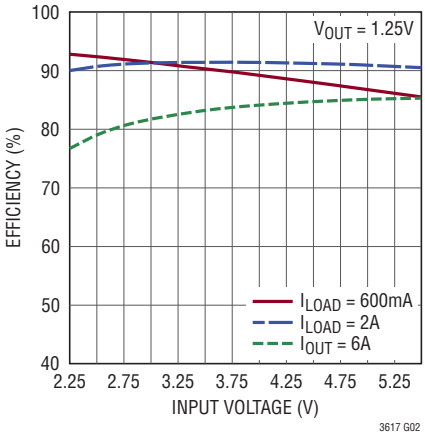
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 3.3V, f_O = 1MHz unless otherwise noted.

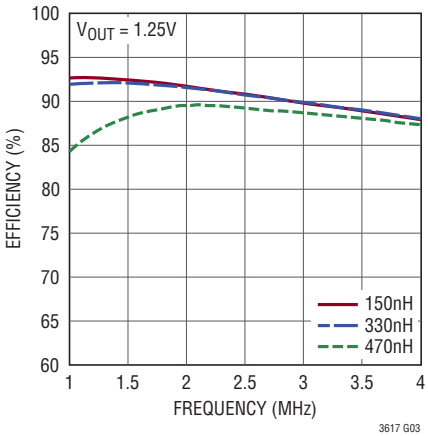
Efficiency vs Load Current



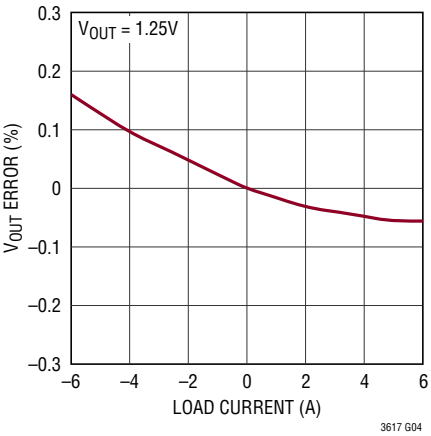
Efficiency vs Input Voltage



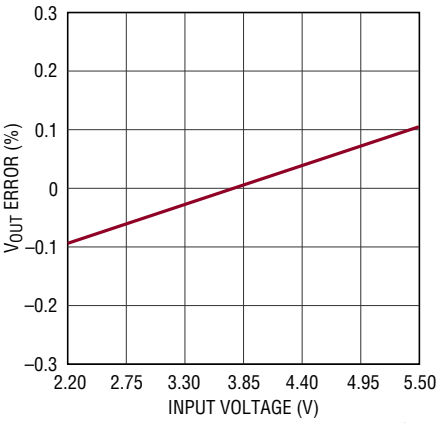
Efficiency vs Frequency



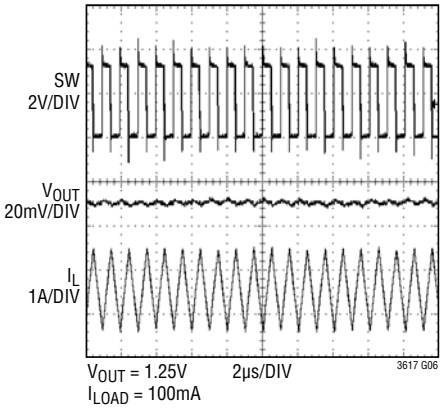
Load Regulation



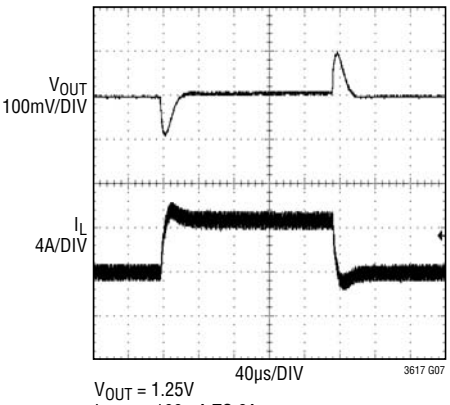
Line Regulation



Output Voltage vs Time

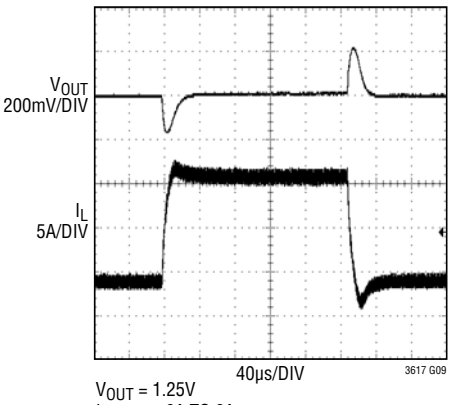


Load Step Transient



V_{OUT} = 1.25V
I_{LOAD} = 100mA TO 6A
COMPENSATION FIGURE 1

Load Step Transient

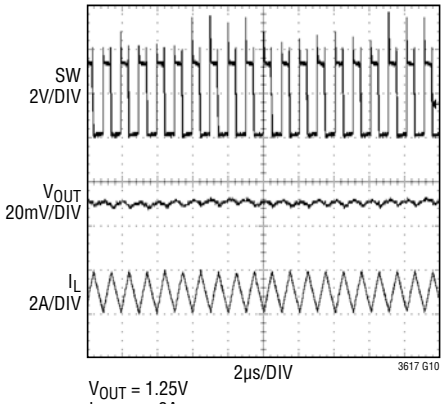


V_{OUT} = 1.25V
I_{LOAD} = –6A TO 6A
COMPENSATION FIGURE 1

TYPICAL PERFORMANCE CHARACTERISTICS

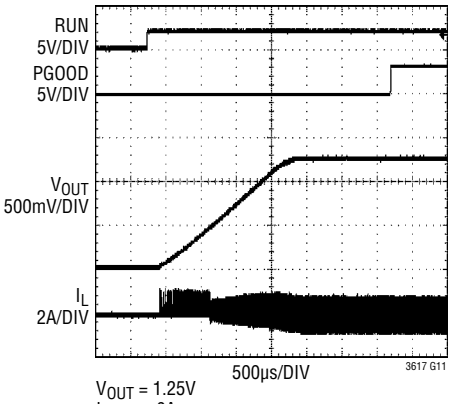
T_A = 25°C, V_{IN} = 3.3V, f_O = 1MHz unless otherwise noted.

Sinking Current



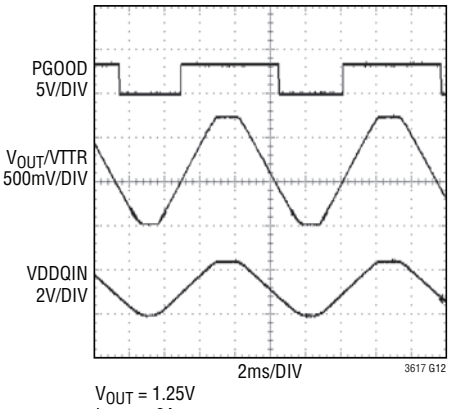
V_{OUT} = 1.25V
I_{LOAD} = –3A

Internal Start-Up



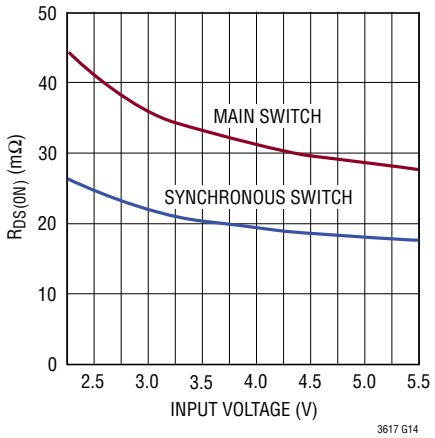
V_{OUT} = 1.25V
I_{LOAD} = 0A

Tracking Up/Down

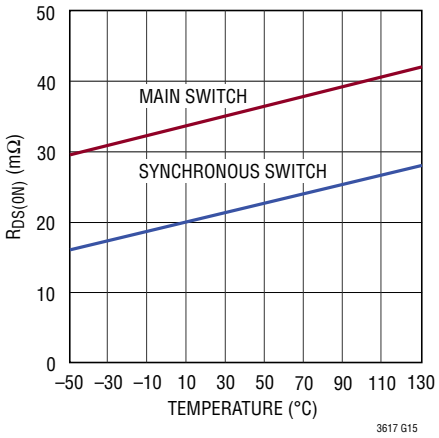


V_{OUT} = 1.25V
I_{LOAD} = 3A

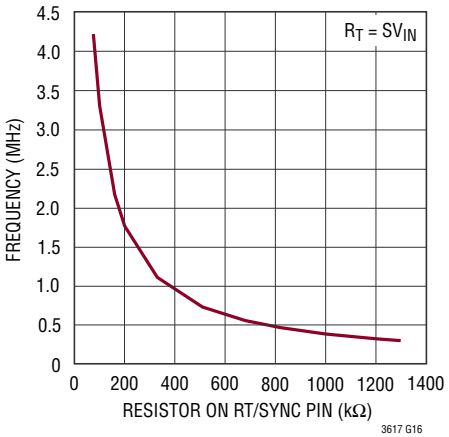
Switch On-Resistance vs Input Voltage



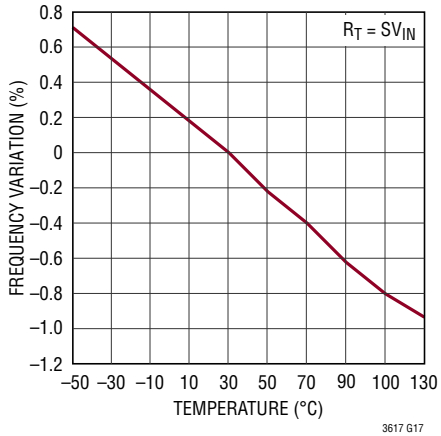
Switch On-Resistance vs Temperature



Frequency vs R_T Resistor



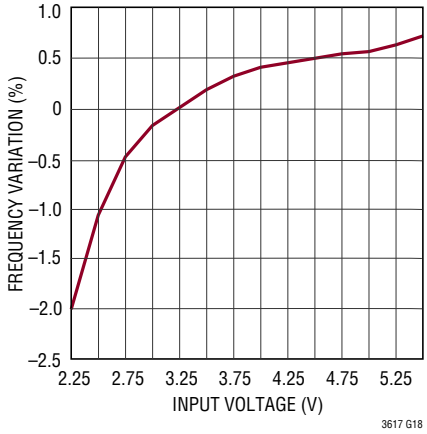
Frequency vs Temperature



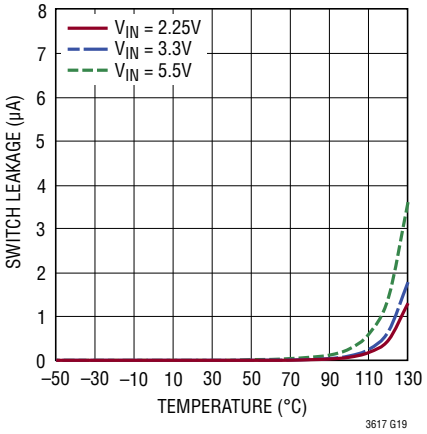
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 3.3V, f_O = 1MHz unless otherwise noted.

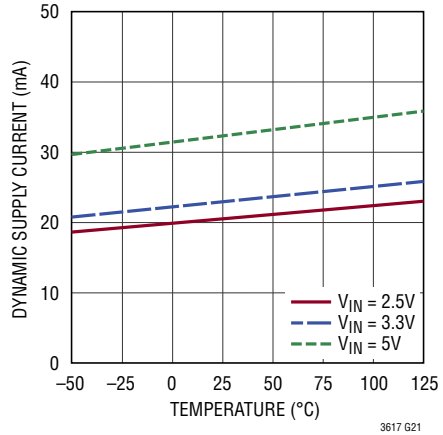
Frequency vs Input Voltage



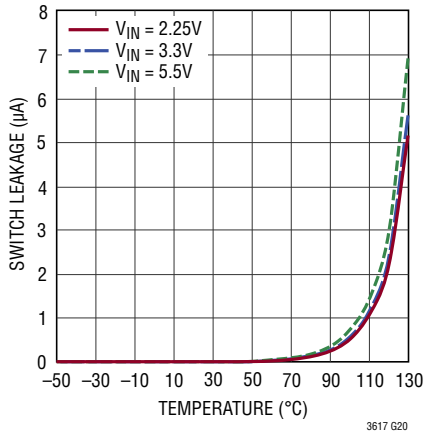
Switch Leakage Current vs Temperature, Main Switch



Dynamic Supply Current vs Temperature



Switch Leakage Current vs Temperature, Synchronous Switch



PIN FUNCTIONS

RT (Pin 1): Oscillator Frequency. This pin provides two ways of setting the constant switching frequency:

1. Connecting a resistor from RT to ground will set the switching frequency based on the resistor value.
2. Tying the RT pin to SV_{IN} enables the internal 2.25MHz oscillator frequency.

SGND (Pin 2): Signal Ground. All small-signal and compensation components should connect to this ground, which in turn should connect to PGND at a single point.

VTTR (Pin 3): Voltage Buffer Output. This pin is the output of an internal voltage buffer whose voltage is equal to VDDQIN • 0.5. Output current capability is ±10mA. VTTR is also the reference voltage of the error amplifier, which sets the output voltage. V_{FB} will regulate to VTTR. Do not exceed 0.1µF capacitance on this pin.

PV_{IN} (Pins 4, 10, 11, 17): Power Input Supply. PV_{IN} connects to the source of the internal P-channel power MOSFET. This pin is independent of SV_{IN} and may be connected to the same supply or to a lower voltage.

SW (Pins 5, 6, 7, 8, 13, 14, 15, 16): Switch Node. Connection to the inductor. These pins connect to the drains of the internal power MOSFET switches.

NC (Pins 9, 12): Can be connected to ground or left open.

SV_{IN} (Pin 18): Signal Input Supply. This pin powers the internal control circuitry and is monitored by the undervoltage lockout comparator.

RUN (Pin 19): Enable Input. Pulling this pin high enables the LTC3617 and forcing it to ground shuts the regulator down. In shutdown, all functions are disabled and the chip draws <1µA of supply current.

SYNC (Pin 20): External Synchronization Input. When a clock signal is applied to this pin, the switching frequency synchronizes to this clock signal. This pin can be either floating or tied to ground if an external clock is not being used.

PGOOD (Pin 21): Power Good. This open-drain output is pulled down to SGND on start-up and when the FB voltage is outside the power good voltage window. If the FB voltage increases and stays inside the power good window for more than 100µs the PGOOD pin is released. If the FB voltage leaves the power good window for more than 100µs the PGOOD pin is pulled low.

The power good window moves in relation to the VDDQIN pin voltage. In shutdown the PGOOD output will actively pull low and may be used to discharge the output capacitors via an external resistor.

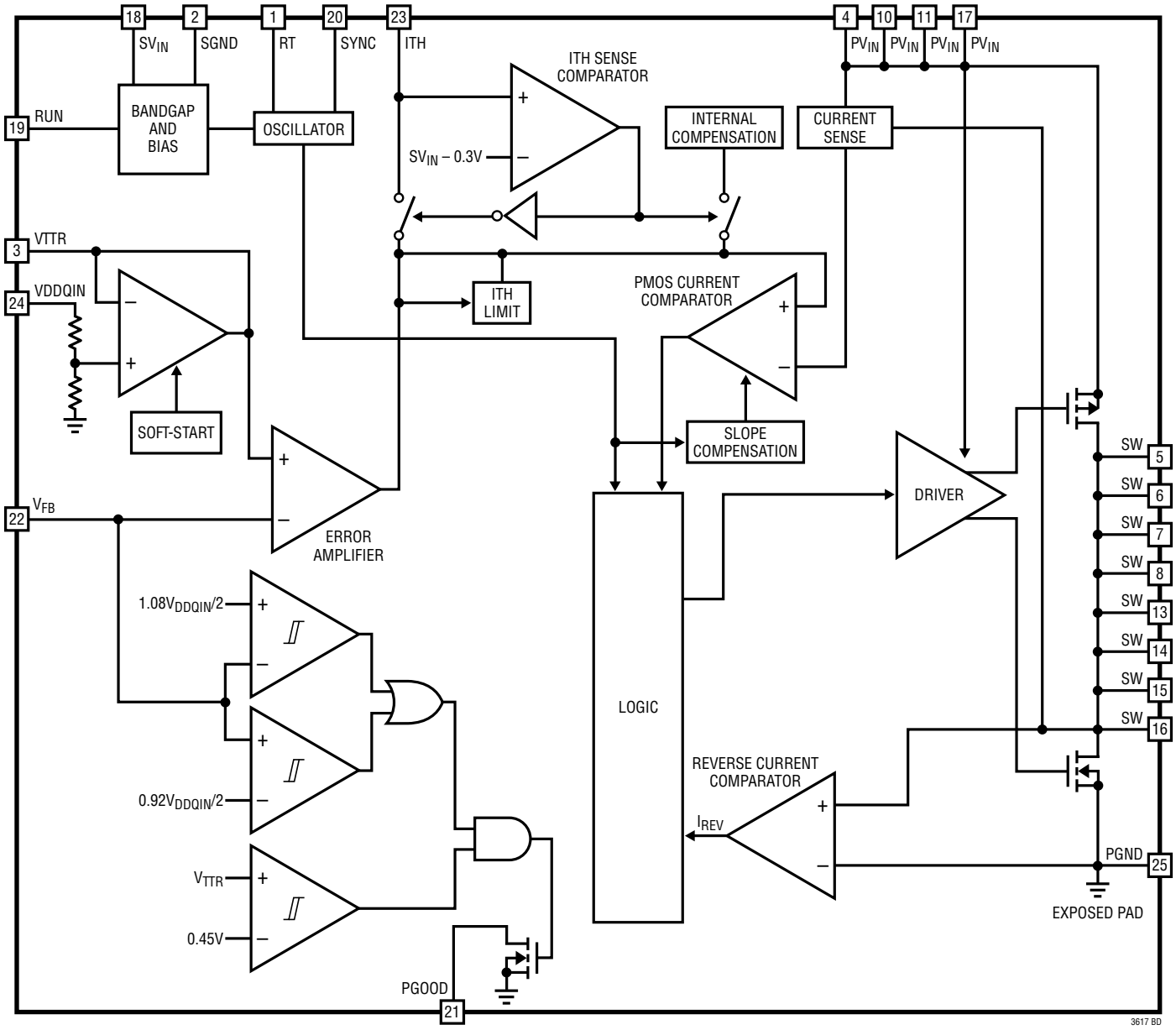
V_{FB} (Pin 22): Voltage Feedback Input Pin. Senses the feedback voltage from the external resistive divider across the output.

ITH (Pin 23): Error Amplifier Compensation. The current comparator's threshold increases with this control voltage. Tying this pin to SV_{IN} enables internal compensation.

VDDQIN (Pin 24): External Reference Input. An internal resistor divider sets the VTTR and V_{FB} regulated voltages to be equal to half the voltage applied to this input.

PGND (Exposed Pad Pin 25): Power Ground. This pin connects to the source of the internal N-channel power MOSFET. This pin should be connected close to the (–) terminal of C_{IN} and C_{OUT}.

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC3617 is a monolithic, constant frequency, current mode step-down DC/DC converter. During normal operation, the internal top power switch (P-channel MOSFET) is turned on at the beginning of each clock cycle. Current in the inductor increases until the current comparator trips and turns off the top power switch. The peak inductor current when the current comparator trips is controlled by the voltage on the ITH pin. The error amplifier adjusts the voltage on the ITH pin by comparing the feedback signal from a resistor divider on the V_{FB} pin with a reference voltage on the VTTR pin. VTTR is the output of an op amp buffer that expresses one-half the voltage on the VDDQIN pin. When the load current increases, it causes a reduction in the feedback voltage relative to the reference. The error amplifier raises the ITH voltage until the average inductor current matches the new load current. Typical voltage range for the ITH pin is from 0.2V to 1.05V with 0.575V corresponding to zero current.

When the top power switch shuts off, the synchronous bottom power switch (N-channel MOSFET) turns on until either the bottom current limit is reached or the next clock cycle begins. The bottom current limit is typically set at –10A.

The operating frequency defaults to 2.25MHz when RT is connected to SV_{IN}, or can be set by an external resistor connected between the RT pin and ground, or by a clock signal applied to the RT pin. The switching frequency can be set from 300kHz to 4MHz.

Overvoltage and undervoltage comparators pull the PGOOD output low if the output voltage varies more than ±8% (typical) from the set point.

VTTR Voltage Buffer Output

An internal high accuracy op amp buffer generates a VTTR pin voltage that is equal to VDDQIN • 0.5. VTTR can source and sink up to 10mA and is stable with a maximum bypass capacitor of 0.1µF. Short-circuit current limit is set around 20mA to prevent damage to the op amp. VTTR is also the reference voltage of the error amplifier which controls the output voltage. Therefore, large transients on this pin will impact the behavior of the output.

V_{IN} Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage spikes, the LTC3617 constantly monitors the V_{IN} pin for an overvoltage condition. When V_{IN} rises above 6.5V, the regulator suspends operation by shutting off both MOSFETS. The regulator executes its soft-start function when exiting an overvoltage condition.

Low Supply Operation

The LTC3617 is designed to operate down to an input supply voltage of 2.25V. An important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the P-channel and N-channel power switches increases. The user should calculate the power dissipation when the LTC3617 is used at 100% duty cycle with low input voltages to ensure that thermal limits are not exceeded. See the Typical Performance Characteristics graphs.

Short-Circuit Protection

The peak inductor current when the current comparator shuts off the top power switch is controlled by the voltage on the ITH pin.

If the output current increases, the error amplifier raises the ITH pin voltage until the average inductor current matches the new load current. In normal operation the LTC3617 clamps the maximum ITH pin voltage at approximately 1.05V which corresponds typically to 10A peak inductor current.

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle. To prevent current runaway from occurring, a secondary current limit is imposed on the inductor current. If the inductor current measured through the bottom MOSFET increases beyond 12A typical, the top power MOSFET will be held off and switching cycles will be skipped until the inductor current decreases below this limit.

APPLICATIONS INFORMATION

The basic LTC3617 application circuit is shown in Figure 1.

Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values.

Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output voltage ripple.

The operating frequency of the LTC3617 is determined by an external resistor that is connected between the RT pin and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by using the following equation:

$$R_T = \frac{3.82 \bullet 10^{11} Hz}{f_{OSC}(Hz)} \Omega - 16k\Omega$$

Although frequencies as high as 4MHz are possible, the minimum on-time of the LTC3617 imposes a minimum limit on the operating duty cycle. The minimum on-time is typically 80ns; therefore, the minimum duty cycle is equal to 80ns•f_{OSC}(Hz)•100%.

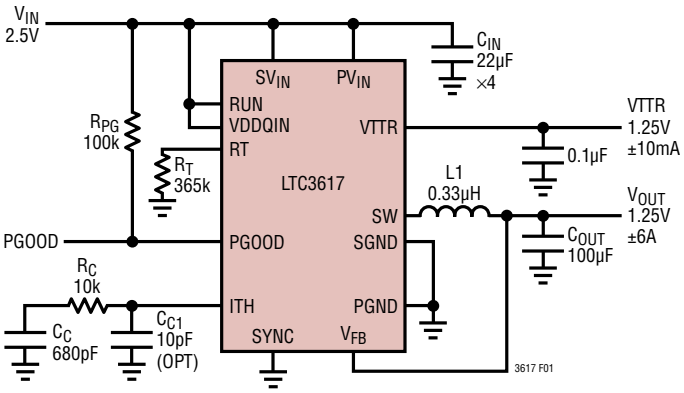


Figure 1. 1.25V, ±6A at 1MHz from 2.5V

Tying the RT pin to SV_{IN} sets the default internal operating frequency to 2.25MHz ±20%.

Frequency Synchronization

The LTC3617's internal oscillator can be synchronized to an external frequency by applying a square wave clock signal to the SYNC pin. During synchronization, the top switch turn-on is locked to the falling edge of the external frequency source. The synchronization frequency range is 300kHz to 4MHz.

The frequency set by the resistor on the RT pin should be the same as the external clock frequency to ensure the internal oscillator properly adjusts when the clock signal is applied or removed.

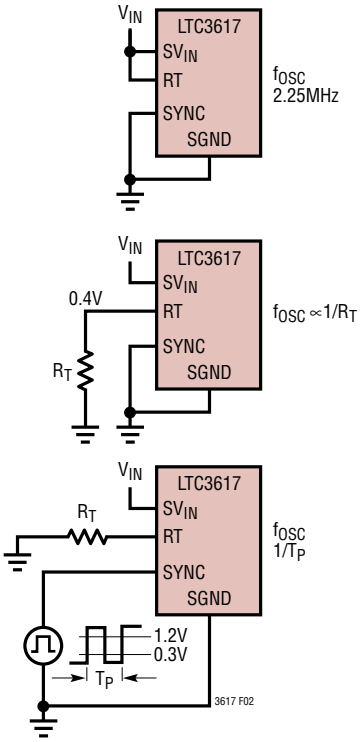


Figure 2. Setting Switching Frequency

APPLICATIONS INFORMATION

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance:

$$\Delta I_L = \left(\frac{V_{OUT}}{f_{SW} \bullet L}\right) \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces the core losses in the inductor, the ESR losses in the output capacitors and the output voltage ripple. A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.3 \bullet I_{OUT(MAX)}$. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left(\frac{V_{OUT}}{f_{SW} \bullet \Delta I_{L(MAX)}}\right) \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore, copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," meaning that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequently output voltage ripple. Do not allow a ferrite core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. Table 1 shows some typical surface mount inductors that work well in LTC3617 applications.

Input Capacitor (C_{IN}) Selection

In continuous mode, the source current of the top P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large input voltage transients, a low ESR capacitor sized for the maximum RMS current must be used at V_{IN}.

The maximum RMS capacitor current is given by:

$$I_{RMS} = I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\left(\frac{V_{IN}}{V_{OUT}} - 1\right)}$$

This formula has a maximum at $V_{IN} = 2 \bullet V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

APPLICATIONS INFORMATION

Table 1. Representative Surface Mount Inductors

INDUCTANCE (µH)	DCR (mΩ)	SATURATION CURRENT (A)	DIMENSIONS (mm)	HEIGHT (mm)
Vishay IHLP-2525CZ-01				
0.10	1.5	60	6.5 × 6.9	3
0.15	1.9	52	6.5 × 6.9	3
0.20	2.4	41	6.5 × 6.9	3
0.22	2.5	40	6.5 × 6.9	3
0.33	3.5	30	6.5 × 6.9	3
0.47	4	26	6.5 × 6.9	3
Sumida CDMC6D28 Series				
0.2	2.5	21.7	7.25 × 6.5	3
0.3	3.2	15.4	7.25 × 6.5	3
0.47	4.2	13.6	7.25 × 6.5	3
Cooper HCM0703 Series				
0.22	2.8	40	6.8 × 7.1	3.0
0.47	4.2	26	6.8 × 7.1	3.0
0.68	5.5	25	6.8 × 7.1	3.0
Würth Electronik WE-HC744310 Series				
0.24	1.8	40	7 × 6.9	3.0
0.52	3.7	20	7 × 6.9	3.0
Coilcraft SLC7530 Series				
0.100	0.123	20	7.5 × 6.7	3
0.188	0.100	21	7.5 × 6.7	3
0.272	0.100	14	7.5 × 6.7	3
0.350	0.100	11	7.5 × 6.7	3
0.400	0.100	8	7.5 × 6.7	3

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is typically driven by the required ESR to minimize voltage ripple and load step transients (low ESR ceramic capacitors are discussed in the next section). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \le \Delta I_L \bullet \left(ESR + \frac{1}{8 \bullet f_{SW} \bullet C_{OUT}} \right)$$

where f_{OSC} = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

In surface mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirement of the application. Aluminum electrolytic, special polymer, ceramic and dry tantalum capacitors are all available in surface mount packages.

Tantalum capacitors have the highest capacitance density, but can have higher ESR and must be surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can often be used in extremely cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability.

Ceramic Input and Output Capacitors

Ceramic capacitors have the lowest ESR and can be cost effective, but also have the lowest capacitance density, have high voltage and temperature coefficients, and exhibit audible piezoelectric effects. In addition, the high Q of ceramic capacitors along with trace inductance can lead to significant ringing.

They are attractive for switching regulator use because of their very low ESR, but care must be taken when using only ceramic input and output capacitors.

Ceramic capacitors are prone to temperature effects which require the designer to check loop stability over the operating temperature range. To minimize their large temperature and voltage coefficients, only X5R or X7R ceramic capacitors should be used.

When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the V_{IN} pin. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, the ringing at the input can be large enough to damage the part.

APPLICATIONS INFORMATION

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation components and the output capacitor size. Typically, 3 to 4 switching cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about 2 to 4 times the linear drop of the first cycle; however, this behavior can vary depending on the compensation component values. Thus, a good place to start is with the output capacitor size of approximately:

$$C_{OUT} \approx \frac{3.5 \bullet \Delta I_{OUT}}{f_{SW} \bullet V_{DROOP}}$$

This is only an approximation; more capacitance may be needed depending on the duty cycle and load step requirements.

In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low.

Output Voltage Programming

In most applications, V_{OUT} is connected directly to V_{FB}. The output voltage will be equal to one-half of the voltage on the VDDQIN pin for this case.

$$V_{OUT} = \frac{VDDQIN}{2}$$

If a different output relationship is desired, an external resistor divider from V_{OUT} to V_{FB} can be used. The output voltage will then be set according to the following equation:

$$V_{OUT} = \frac{VDDQIN}{2} \bullet \left(1 + \frac{R2}{R1}\right)$$

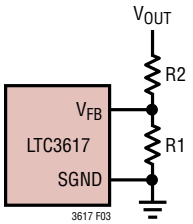


Figure 3. Setting the Output Voltage

Internal and External Compensation

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the ITH pin allows the transient response to be optimized over a wide range of output capacitance.

The ITH external components (R_C and C_C) shown in Figure 1 provide adequate compensation as a starting point for most applications. The values can be modified slightly to optimize transient response once the final PCB layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system. The external capacitor, C_{C1}, (Figure 1) is not needed for loop stability, but it helps filter out any high frequency noise that may couple onto that node.

APPLICATIONS INFORMATION

The first circuit in the Typical Applications section uses faster compensation to improve step response.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. More output capacitance may be required depending on the duty cycle and load step requirements.

Internal Compensation

The LTC3617 provides the option to use a fixed internal loop compensation network to reduce the required external component count and design time. The internal loop compensation network can be selected by connecting the ITH pin to SV_{IN}. However, selecting the internal compensation might result in an unstable output voltage when tracking down to 0V.

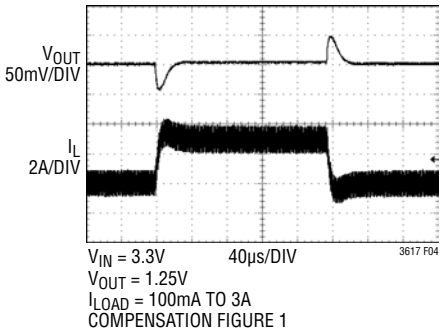


Figure 4. Load Step Transient with External Compensation

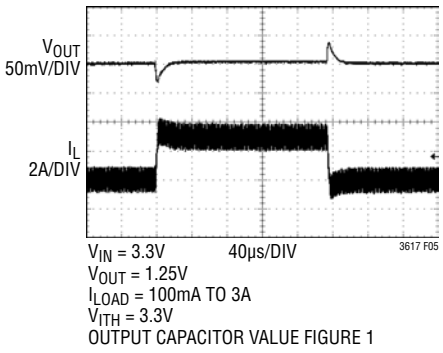


Figure 5. Load Step Transient with Internal Compensation

Shutdown and Soft-Start

The RUN pin provides a means to shut down the LTC3617. Tying the RUN pin to SGND places the regulator in a low quiescent current shutdown state (I_Q < 1µA).

Pulling the RUN pin high enables the regulator which allows an internal soft-start to slowly ramp the VTTR pin voltage at a rate of approximately 850mV/ms. During this start-up time, the regulator will operate in discontinuous mode until the VTTR pin voltage exceeds approximately 0.45V.

When RUN is pulled low, the regulator will force the peak inductor current to discharge to around 0A before shutting off both power MOSFETs.

Output Power Good

The PGOOD output of the LTC3617 is driven by a 17Ω (typical) open-drain pull-down MOSFET. This MOSFET turns off approximately 3ms to 4ms after the beginning of start-up and once the output voltage is within 5% (typical) of 0.5 • VDDQIN, allowing the voltage at PGOOD to rise via an external pull-up resistor (100k typical). If the output voltage exits an 8% (typical) regulation window of 0.5 • VDDQIN or the VTTR pin is lower than 0.45V, the open-drain output will pull low, thus dropping the PGOOD pin voltage. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTC3617 PGOOD falling edge includes a filter time of approximately 105µs.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

APPLICATIONS INFORMATION

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is usually of no consequence.

1. The V_{IN} quiescent current is due to two components: the DC bias current as given in the Electrical Characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is the current into V_{IN} due to gate charge, and it is typically larger than the DC bias current. Both the DC bias and gate charge losses are proportional to V_{IN}; thus, their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. To obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

   Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

Thermal Considerations

In most applications, the LTC3617 does not generate much heat due to its high efficiency.

However, in high current applications where the LTC3617 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat generated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 160°C, both power switches will be turned off and the SW node will become high impedance.

To prevent the LTC3617 from exceeding the maximum junction temperature, some thermal analysis is required. The temperature rise is given by:

$$T_{RISE} = (P_D) \bullet (\theta_{JA})$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by:

$$T_J = T_A + T_{RISE}$$

where T_A is the ambient temperature.

As an example, consider the case when the LTC3617 is used in a DDR application where V_{IN} = 3.3V, I_{OUT} = 6A, f = 1MHz, V_{OUT} = 1.25V. The equivalent power MOSFET resistance R_{SW} is:

$$R_{SW} = R_{DS(ON)}TOP \bullet \frac{V_{OUT}}{V_{IN}} + R_{DS(ON)}BOT \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$= 35m\Omega \bullet \frac{1.25}{3.3} + 25m\Omega \bullet \left(1 - \frac{1.25}{3.3}\right) = 28.79m\Omega$$

The V_{IN} current during 1MHz with no load is about 22mA, which includes switching and internal biasing current loss, transition loss, inductor core loss and other losses in the application. Therefore, the total power dissipated by the part is:

$$P_D = I_{OUT}^2 \bullet R_{SW} + V_{IN} \bullet I_{VIN} \text{ (No Load)}$$

$$= 36A^2 \bullet 28.79m\Omega + 3.3V \bullet 22mA = 1.11W$$

The QFN 3mm × 5mm package junction-to-ambient thermal resistance, θ_{JA}, is around 43°C/W. Therefore, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

$$T_J = 1.11W \bullet 43°C/W + 25°C = 73°C$$

APPLICATIONS INFORMATION

Remembering that the above junction temperature is obtained from the $R_{DS(ON)}$ at 25°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. Redoing the calculation assuming that R_{SW} increased 15% at 73°C yields a new junction temperature of 79°C. Therefore, we can safely assume that the actual junction temperature will not exceed the absolute maximum junction temperature of 125°C.

Note that for very low input voltage, the junction temperature will be higher due to increased switch resistance, $R_{DS(ON)}$. It is not recommended to use full load current with high ambient temperature and low input voltage.

To maximize the thermal performance of the LTC3617 the exposed pad must be soldered to a ground plane. See the PCB Layout Board Checklist.

Design Example

As a design example, consider the LTC3617 in an application with the following specifications:

V_{IN} = 2.5V, V_{OUT} = 1.25V, $I_{OUT(MAX)}$ = 6A, $I_{OUT(MIN)}$ = 200mA, f = 2.6MHz.

First, calculate the timing resistor:

$$R_T = \frac{3.82^{11}Hz}{2.6MHz} - 16k = 130k\Omega$$

Next, calculate the inductor value for about 33% ripple current at maximum V_{IN}:

$$L = \left(\frac{1.25V}{2.6MHz \bullet 2A}\right) \bullet \left(1 - \frac{1.25V}{2.5V}\right) = 0.12\mu H$$

Using a standard value of 0.1µH inductor results in a maximum ripple current of:

$$\Delta I_L = \left(\frac{1.25V}{2.6MHz \bullet 0.1\mu H}\right) \bullet \left(1 - \frac{1.25V}{2.5V}\right) = 2.4A$$

C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, a 100µF ceramic capacitor is used with a X5R or X7R dielectric.

C_{IN} should be selected for a maximum current rating of:

$$I_{RMS} = 6A \bullet \frac{1.25V}{2.5V} \bullet \sqrt{\left(\frac{2.5V}{1.25V} - 1\right)} = 3A_{RMS}$$

Decoupling PV_{IN} with four 10µF to 22µF capacitors is adequate for most applications. Connecting the V_{FB} pin directly to V_{OUT} will set the output voltage equal to one-half of the voltage on the VDDQIN pin. The complete circuit of this design example is illustrated in Figure 1.

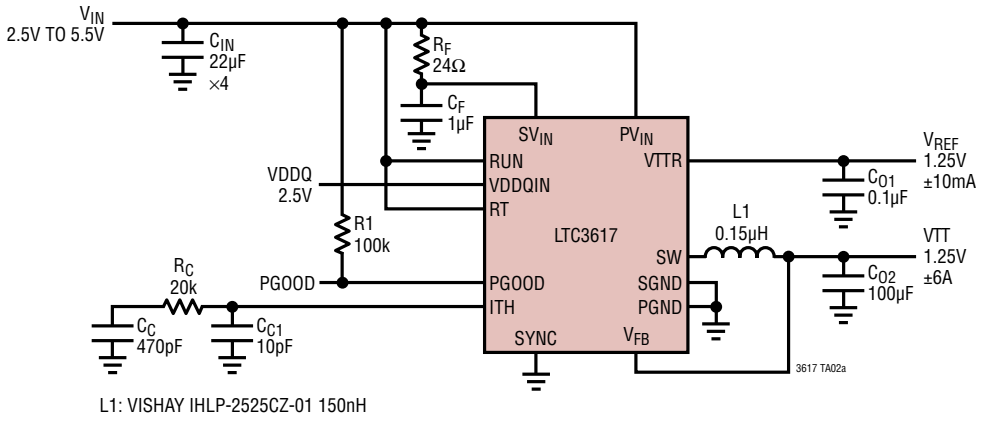
PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3617:

1. A ground plane is recommended. If a ground plane layer is not used, the signal and power grounds should be segregated with all small-signal components returning to the SGND pin at one point which is then connected to the PGND pin close to the LTC3617.
2. Connect the (+) terminal of the input capacitor(s), C_{IN}, as close as possible to the PV_{IN} pin, and the (–) terminal as close as possible to the exposed pad, PGND. This capacitor provides the AC current into the internal power MOSFETs.
3. Keep the switching node, SW, away from all sensitive small-signal nodes.
4. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to PGND (exposed pad) for best performance.
5. Connect the V_{FB} pin directly to V_{OUT}.

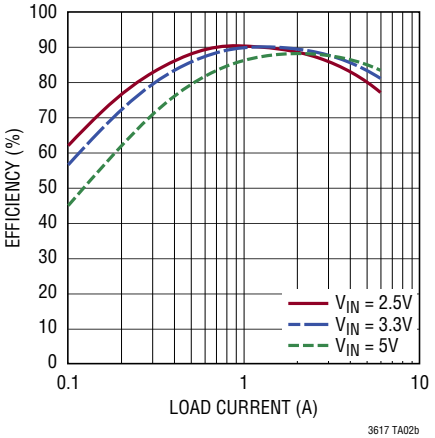
TYPICAL APPLICATIONS

1.25V, ±6A DDR Memory Termination Supply, 2.25MHz

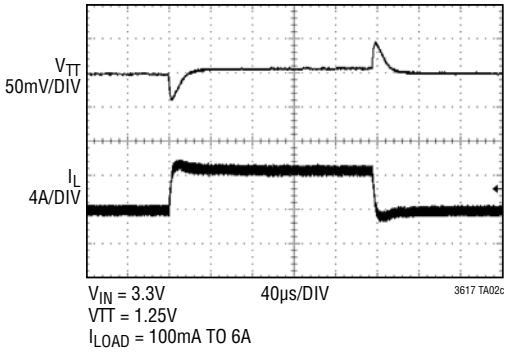


L1: VISHAY IHLP-2525CZ-01 150nH

Efficiency vs Load Current

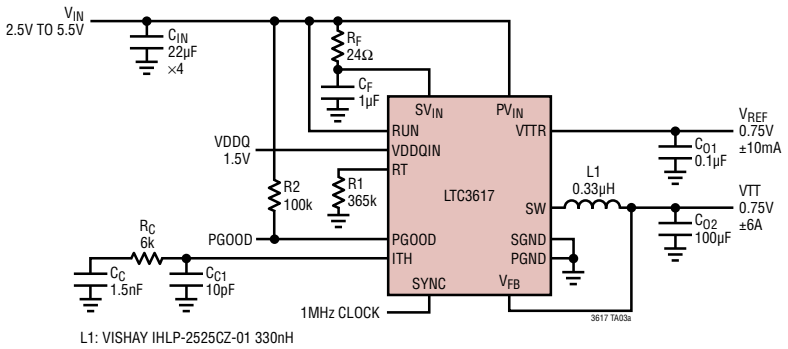


Load Step Response



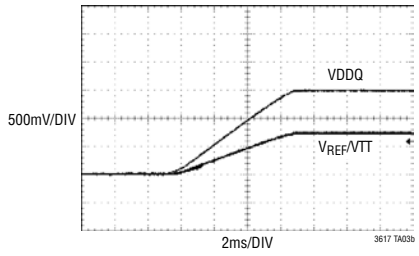
TYPICAL APPLICATIONS

0.75V, ±6A DDR Termination Using a 1MHz External Clock

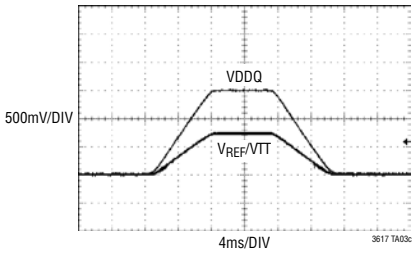


L1: VISHAY IHLP-2525CZ-01 330nH

External Start-Up

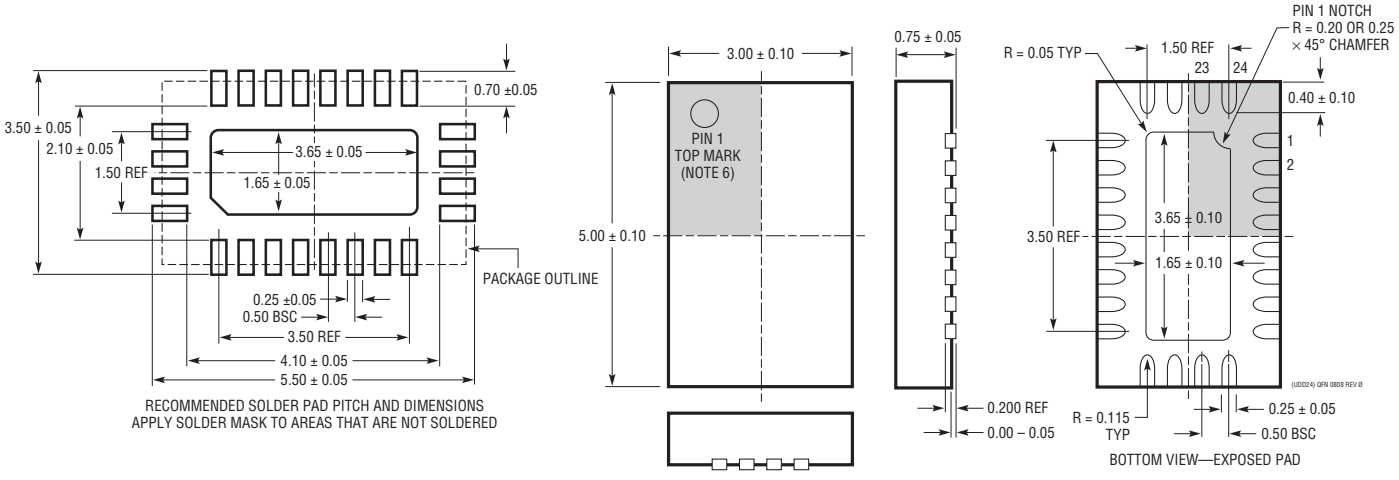


Output Tracking Up/Down



PACKAGE DESCRIPTION

UDD Package
24-Lead Plastic QFN (3mm × 5mm)
(Reference LTC DWG # 05-08-1833 Rev Ø)



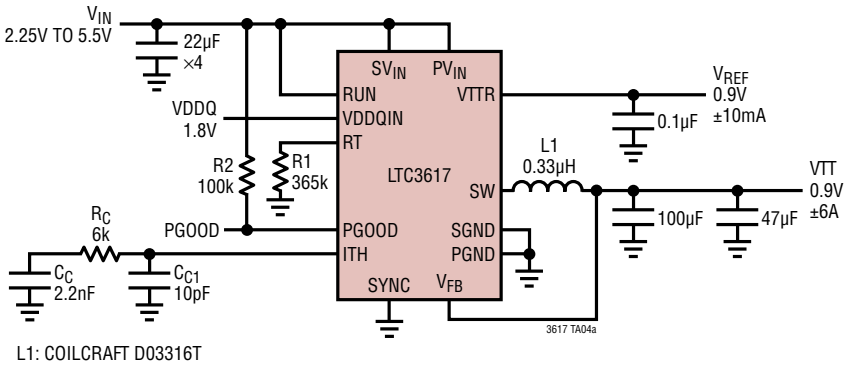
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	7/11	Updated Main Control section	9
		Updated Output Power Good section	14
		Updated Typical Application and scale on graphs	18, 20

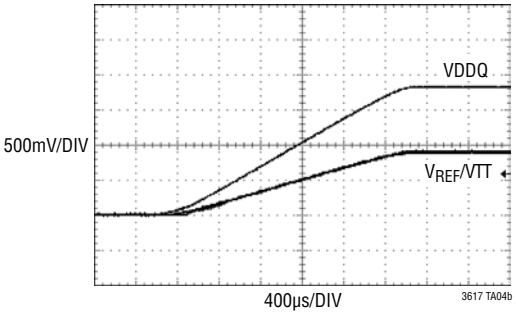
TYPICAL APPLICATION

DDR2 Termination, 1MHz



L1: COILCRAFT D03316T

External Start-Up



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3616	5.5V, 6A (I_{OUT}) 4MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.25V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 70µA, I_{SD} < 1µA, 3mm × 5mm QFN24 Package
LTC3612	5.5V, 3A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.25V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 70µA, I_{SD} <1µA, 3mm ×4mm QFN-20 TSSOP20E Package
LTC3418	5.5V, 8A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.25V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 380µA, I_{SD} <1µA, 5mm × 7mm QFN-38 Package
LTC3415	5.5V, 7A (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 450µA, I_{SD} <1µA, 5mm × 7mm QFN-38 Package
LTC3416	5.5V, 4A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.25V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 64µA, I_{SD} <1µA, TSSOP20E Package
LTC3413	5.5V, 3A (I_{OUT} Sink/Source), 2MHz, Monolithic Synchronous Regulator for DDR/QDR Memory Termination	90% Efficiency, $V_{IN(MIN)}$ = 2.25V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = V_{REF}/2, I_Q = 280µA, I_{SD} <1µA, TSSOP16E Package
LTC3412A	5.5V, 2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} <1µA, 4mm × 4mm QFN-16 TSSOP16E Package

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