Quad, 1 A, 5.5 V, Synchronous Step-Down Regulators with One RF LDO Regulator

Data Sheet

ADP5138

FEATURES

- PVINx voltage range: 3 V to 5.5 V
- Continuous output current
  - Channel 1 to Channel 4 (buck): 1 A
  - Channel 5 (LDO): 250 mA
- 3.2 MHz fixed PWM switching frequency
- Synchronization input function
- Buck regulators run at 90° out of phase
- Individual precision enable input
- Power-on reset output
- Integrated compensation
- Soft start and power-up sequencing reduce inrush current
- Active output discharge switch function
- Stable with low ESR output ceramic capacitors
- OVLO, UVM, and UVLO
- TSD protection
- Qualified for automotive applications

APPLICATIONS

- Automotive
- Industrial and instrumentation
- DC to dc point of load applications

TYPICAL APPLICATION CIRCUIT

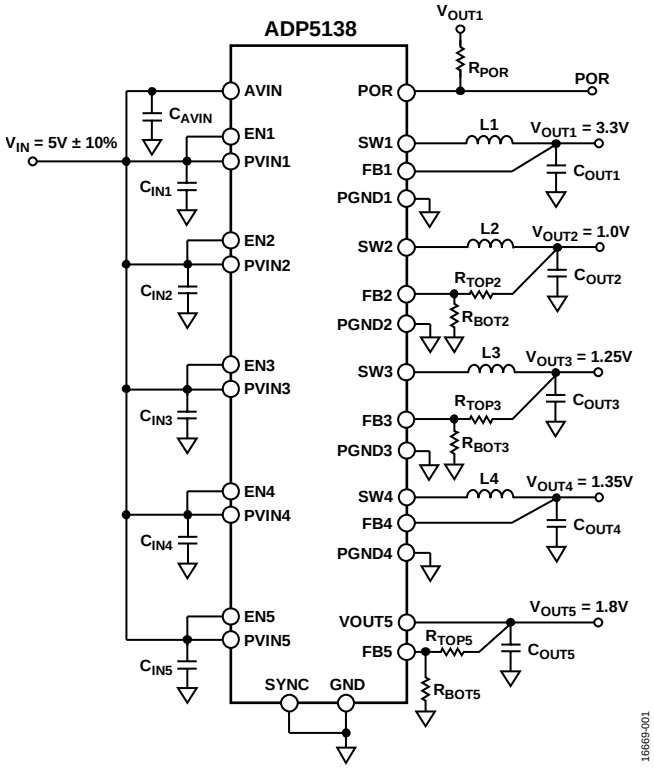

Figure 1.

GENERAL DESCRIPTION

The ADP5138 integrates four high performance synchronous step-down regulators and one low noise radio frequency (RF) low dropout (LDO) regulator. The device runs from PVINx input voltages of 3 V to 5.5 V. The output voltage of each channel is factory set or can be programmed down to 0.8 V with a resistor. Each step-down regulator can provide up to 1 A of continuous output current and the LDO can provide 250 mA of output current.

The ADP5138 runs at the fixed PWM switching frequency, 3.2 MHz, or can be synchronized to the external clock from 2.8 MHz to 3.5 MHz, which is outside the amplitude modulation (AM) band. The four buck regulators run at 90° out of phase to reduce the input ripple current and the input capacitor size, thereby helping to lower system electromagnetic interference (EMI).

The ADP5138 integrates internal compensation to simplify the design. The internal soft start circuitry and power-up sequencing help reduce the input inrush current.

The ADP5138 monitors the input voltage and provides input overvoltage lockout (OVLO), undervoltage monitor (UVM), and undervoltage lockout (UVLO) features. It also monitors the undervoltage and overvoltage of the outputs. The power-on reset (POR) signal is asserted when the input or output voltage fault occurs.

Additional protection includes overcurrent protection (OCP) and thermal shutdown (TSD).

The ADP5138 operates over the −40°C to +125°C operating temperature range (junction), and is available in a 28-lead LFCSP package.

Rev. A Document Feedback

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REVISION HISTORY

8/2018—Rev. 0 to Rev. A

Change to Figure 2 ... 3

5/2018—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

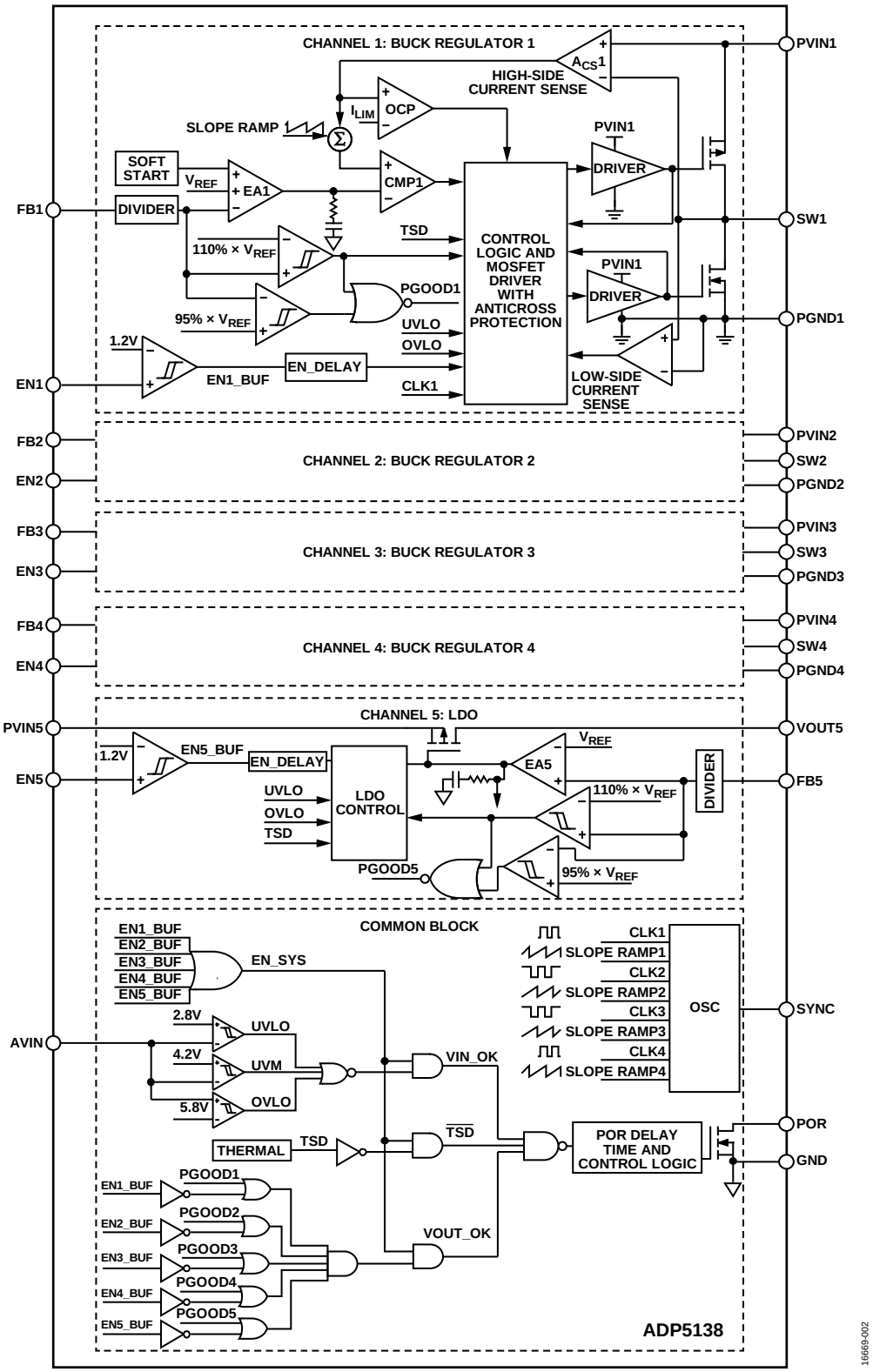


Figure 2.

SPECIFICATIONS

$V_{AVIN} = V_{PVIN1} = V_{PVIN2} = V_{PVIN3} = V_{PVIN4} = V_{PVIN5} = 5.0$ V, $T_J = -40°C$ to $+125°C$ for minimum and maximum specifications, and $T_A = 25°C$ for typical specifications, unless otherwise noted. V_{OUTx} is the output voltage on Channel x, where x is 1 to 5.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER INPUT						
PVINx Voltage Range	V_{PVINx}	PVIN1, PVIN2, PVIN3, and PVIN4 pins	3		5.5	V
		PVIN5 pin	1.7		5.5	V
AVIN Voltage Range	V_{AVIN}	AVIN pin	3		5.5	V
Quiescent Current	I_Q	No switching		6	7.5	mA
Shutdown Current	I_{SHDN}	$V_{EN1} = V_{EN2} = V_{EN3} = V_{EN4} = V_{EN5} = GND$		0.6	20	µA
Input UVLO Threshold						
AVIN UVLO Rising				2.9	3	V
AVIN UVLO Falling			2.7	2.8		V
Input Undervoltage Monitor Threshold						
AVIN UVM Falling			4.05	4.2	4.35	V
AVIN UVM Hysteresis				80	100	mV
Input OVLO Threshold						
AVIN OVLO Rising			5.6	5.8	6	V
AVIN OVLO Hysteresis				80	100	mV
ENABLE		ENx pins				
Rising Threshold				1.2	1.28	V
Falling Threshold			1.02	1.1		V
Pull-Down Resistance				1		MΩ
POWER-ON RESET (POR)		POR pin				
Output Undervoltage Threshold						
Rising Threshold		Percentage of normal V_{OUTx}	93	95	97	%
Falling Threshold		Percentage of normal V_{OUTx}	91	93	95	%
Output Overvoltage Threshold						
Rising Threshold		Percentage of normal V_{OUTx}	108	110	112	%
Falling Threshold		Percentage of normal V_{OUTx}	105.5	108	110	%
Deglitch Time						
POR Rising	$t_{POR\_DELAY\_R}$		5	5.7	6.8	ms
POR Falling	$t_{POR\_DELAY\_F}$			10		µs
POR Leakage Current		POR voltage (V_{POR}) = 5 V		0.05	1	µA
POR Output Low Voltage		POR current (I_{POR}) = 3 mA		38	100	mV
POR Effective Threshold Voltage on AVIN[1]	V_{AVIN_POR}	I_{POR} = 1 mA, $V_{POR} \leq 0.2$ V			1.16	V
START-UP SEQUENCE DELAY TIME	t_{SS_D}	Delay time during startup	500	600	700	µs
THERMAL SHUTDOWN						
Threshold[1]				150		°C
Hysteresis[1]				15		°C

[1] Guaranteed by design, but not production tested.

BUCK REGULATOR SPECIFICATIONS

V_{AVIN} = V_{PVIN1} = V_{PVIN2} = V_{PVIN3} = V_{PVIN4} = 5.0 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FEEDBACK						
FB1 to FB4 Regulation Voltage	V_{FB1} to V_{FB4}	Adjustable version	0.788	0.8	0.812	V
Fixed Output Accuracy[1]	V_{OUT1} to V_{OUT4}		−2		+2	%
OUTPUT CHARACTERISTICS		Pulse-width modulation (PWM) mode				
Load Regulation[2]	$\Delta V_{OUT}/\Delta I_{OUT}$	Output current (I_{OUT}) from 0 A to 1 A, V_{AVIN} = V_{PVINx} = 5 V		0.3		%/A
Line Regulation[2]	$\Delta V_{OUT}/\Delta V_{PVIN}$	V_{AVIN} = V_{PVINx} = 4 V to 5.5 V, I_{OUT} = 1 A		0.1		%/V
SWITCH NODE						
High-Side On Resistance[3]	R_{DSON_H}	V_{AVIN} = V_{PVINx} = 5 V, I_{SWx} = 0.5 A		130	200	mΩ
Low-Side On Resistance[3]	R_{DSON_L}	V_{AVIN} = V_{PVINx} = 5 V, I_{SWx} = 0.5 A		120	200	mΩ
SWx Leakage Current	I_{SW_LK}	V_{AVIN} = V_{PVINx} = 5 V, SWx = GND or SWx = V_{PVINx}		0.1		µA
CURRENT LIMIT						
High-Side Peak Current Limit			1.28	1.6	1.92	A
Low-Side Sink Current Limit				1		A
PWM SWITCHING FREQUENCY	f_{SW}		3	3.2	3.4	MHz
PHASE SHIFT		Phase shift between channels		90		Degrees
SYNC		SYNC pin				
Synchronization Range			2.8		3.5	MHz
SYNC Minimum On Time			100			ns
SYNC Minimum Off Time			100			ns
SYNC Input Voltage						
High			1.2			V
Low					0.4	V
OUTPUT DISCHARGE RESISTANCE	$R_{DISCHARGE1}$ to $R_{DISCHARGE4}$			64	100	Ω
SOFT START TIME	t_{SS1} to t_{SS4}		425	500	575	µs

[1] V_{OUT1} to V_{OUT4} are the output voltages on Channel 1 to Channel 4.
[2] Bench characterization result.
[3] Pin to pin measurement.

LDO REGULATOR SPECIFICATIONS

V_{AVIN} = 5.0 V, V_{PVIN5} = (output voltage of Channel 5 (V_{OUT5}) + 0.5 V) or 3 V (whichever is greater), input capacitance of Channel 5 (C_{IN5}) = output capacitance of Channel 5 (C_{OUT5}) = 1 µF, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENT						
Operating Quiescent Current	I_{Q_LDO5}	I_{OUT5} = 0 µA, V_{OUT5} = 1.8 V		58	100	µA
		I_{OUT5} = 100 mA, V_{OUT5} = 1.8 V		146	300	µA
Output Current	I_{OUT5}	$V_{PVIN5} \geq 3$ V			250	mA
		1.7 V ≤ V_{PVIN5} < 3 V			100	mA
Current Limit		V_{OUT5} drops 5% from nominal voltage	300	400		mA
FEEDBACK						
FB5 Regulation Voltage	V_{FB5}	Adjustable version	0.788	0.8	0.812	V
Fixed Output Voltage Accuracy	V_{OUT5}	I_{OUT5} = 10 mA, T_J = 25°C	−1		+1	%
		1 mA < I_{OUT5} < 250 mA	−2		+2	%
REGULATION						
Load Regulation		I_{OUT5} from 1 mA to 250 mA		0.002	0.005	%/mA
Line Regulation		I_{OUT5} = 10 mA	−0.1		+0.1	%/V
DROPOUT VOLTAGE[1]	$V_{DROPOUT5}$	V_{OUT5} = 3.3 V, I_{OUT5} = 250 mA		173		mV
		V_{OUT5} = 1.8 V, I_{OUT5} = 100 mA		132		mV
OUTPUT DISCHARGE RESISTANCE	$R_{DISCHARGE5}$			83	120	Ω
SOFT START TIME	t_{SS5}	V_{OUT5} = 1.8 V, I_{OUT5} = 250 mA	420	570	720	µs
OUTPUT NOISE[2]	OUT_{NOISE5}	10 Hz to 100 kHz, V_{PVIN5} = 5 V, V_{OUT5} = 1.8 V, I_{OUT5} = 250 mA, adjustable output option		20		µV rms
POWER SUPPLY REJECTION RATIO[2]	$PSRR_{LDO5}$	1 kHz, V_{PVIN5} = 5 V, V_{OUT5} = 1.8 V, I_{OUT5} = 250 mA, adjustable output option		55		dB

[1] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage.
[2] Bench characterization result.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
PVIN1, PVIN2, PVIN3, PVIN4, PVIN5, AVIN, VOUT5	−0.3 V to +6 V
SW1, SW2, SW3, SW4	−0.3 V to +6 V
FB1, FB2, FB3, FB4, FB5, EN1, EN2, EN3, EN4, EN5, POR, SYNC	−0.3 V to +6 V
PGND1, PGND2, PGND3, PGND4 to GND	−0.3 V to +0.3 V
Operating Temperature Range (Junction)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020
Electrostatic Discharge (ESD)	
Human Body Model	2000 V
Charged Device Model	500 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment.

Careful attention to PCB thermal design is required.

Table 5. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
CP-28-5	32.6	1.4	°C/W

[1] θ_{JA} is measured using natural convection on a JEDEC 4-layer board with the exposed pad soldered to the PCB and with thermal vias.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

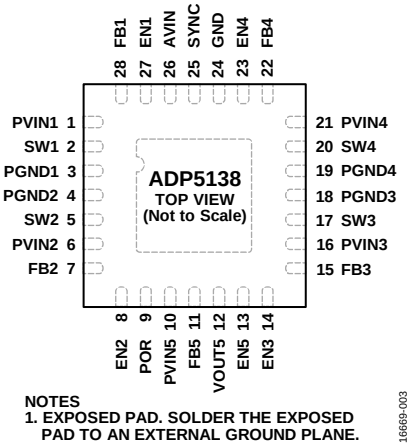


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PVIN1	Power Input for Channel 1. Connect PVIN1 to the input power source, and connect a bypass capacitor between this pin and PGND1.
2	SW1	Switch Node for Channel 1.
3	PGND1	Power Ground for Channel 1.
4	PGND2	Power Ground for Channel 2.
5	SW2	Switch Node for Channel 2.
6	PVIN2	Power Input for Channel 2. Connect PVIN2 to the input power source, and connect a bypass capacitor between this pin and PGND2.
7	FB2	Feedback Voltage Sense Input for Channel 2. Connect this pin to a resistor divider from V_{OUT2} for the adjustable version. For the fixed output version, connect this pin to V_{OUT2} directly.
8	EN2	Precision Enable Pin for Channel 2. Use an external resistor divider to set the turn-on threshold. To enable Channel 2 automatically, connect the EN2 pin to PVIN2.
9	POR	Power-On Reset Output (Open Drain).
10	PVIN5	Power Input for Channel 5. Connect PVIN5 to the input power source, and connect a bypass capacitor between this pin and ground.
11	FB5	Feedback Voltage Sense Input for Channel 5. Connect this pin to a resistor divider from V_{OUT5} for the adjustable version. For the fixed output version, connect this pin to V_{OUT5} directly.
12	VOUT5	Output of Channel 5. Connect a bypass capacitor between this pin and ground.
13	EN5	Precision Enable Pin for Channel 5. Use an external resistor divider to set the turn-on threshold. To enable Channel 5 automatically, connect the EN5 pin to PVIN5.
14	EN3	Precision Enable Pin for Channel 3. Use an external resistor divider to set the turn-on threshold. To enable Channel 3 automatically, connect the EN3 pin to PVIN3.
15	FB3	Feedback Voltage Sense Input for Channel 3. Connect this pin to a resistor divider from V_{OUT3} for the adjustable version. For the fixed output version, connect this pin to V_{OUT3} directly.
16	PVIN3	Power Input for Channel 3. Connect PVIN3 to the input power source, and connect a bypass capacitor between this pin and PGND3.
17	SW3	Switch Node for Channel 3.
18	PGND3	Power Ground for Channel 3.
19	PGND4	Power Ground for Channel 4.
20	SW4	Switch Node for Channel 4.
21	PVIN4	Power Input for Channel 4. Connect PVIN4 to the input power source, and connect a bypass capacitor between this pin and PGND4.
22	FB4	Feedback Voltage Sense Input for Channel 4. Connect this pin to a resistor divider from V_{OUT4} for the adjustable version. For the fixed output version, connect this pin to V_{OUT4} directly.
23	EN4	Precision Enable Pin for Channel 4. Use an external resistor divider to set the turn-on threshold. To enable Channel 4 automatically, connect the EN4 pin to PVIN4.

Pin No.	Mnemonic	Description
24	GND	Analog Ground. Connect this pin to the ground plane.
25	SYNC	Synchronization Input. Connect this pin to an external clock between 2.8 MHz and 3.5 MHz to synchronize the switching frequency to the external clock. If synchronization function is not used, connect this pin to GND.
26	AVIN	Bias Voltage Input Pin. Connect AVIN to PVINx, and connect a bypass capacitor between AVIN and GND.
27	EN1	Precision Enable Pin for Channel 1. Use an external resistor divider to set the turn-on threshold. To enable Channel 1 automatically, connect the EN1 pin to PVIN1.
28	FB1	Feedback Voltage Sense Input for Channel 1. Connect this pin to a resistor divider from V_{OUT1} for the adjustable version. For the fixed output version, connect this pin to V_{OUT1} directly.
	EP	Exposed Pad. Solder the exposed pad to an external ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{AVIN} = V_{PVIN1} = V_{PVIN2} = V_{PVIN3} = V_{PVIN4} = V_{PVIN5} = 5.0 V, f_{SW} = 3.2 MHz, unless otherwise noted. V_{OUTx} is the output voltage on a single channel.

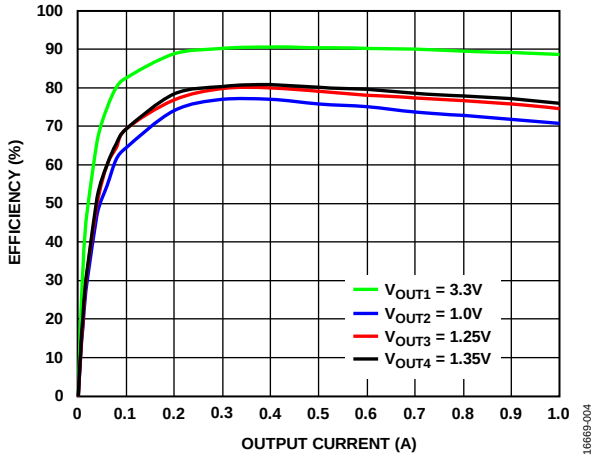


Figure 4. Efficiency vs. Output Current at V_{PVINx} = 5 V, f_{SW} = 3.2 MHz

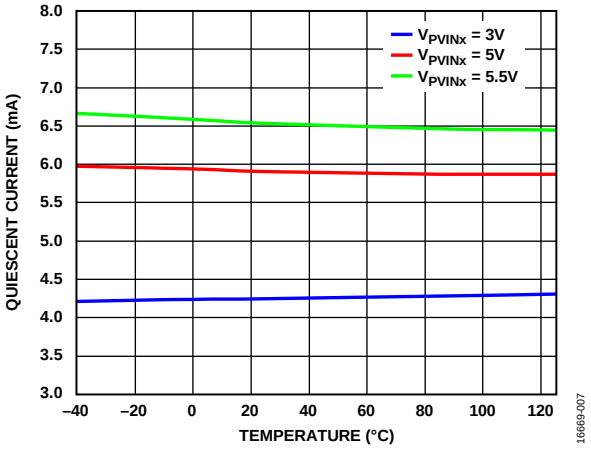


Figure 7. Quiescent Current vs. Temperature

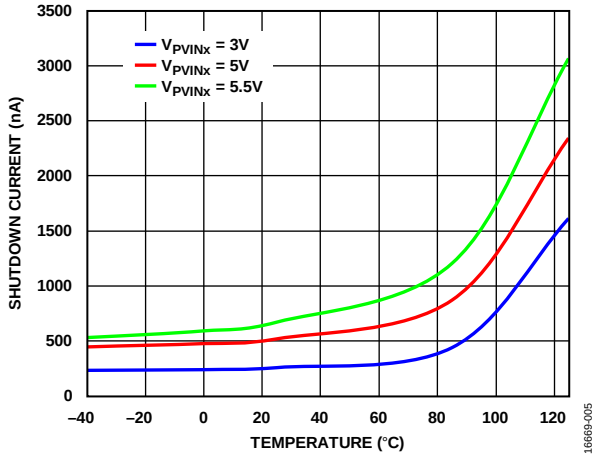


Figure 5. Shutdown Current vs. Temperature

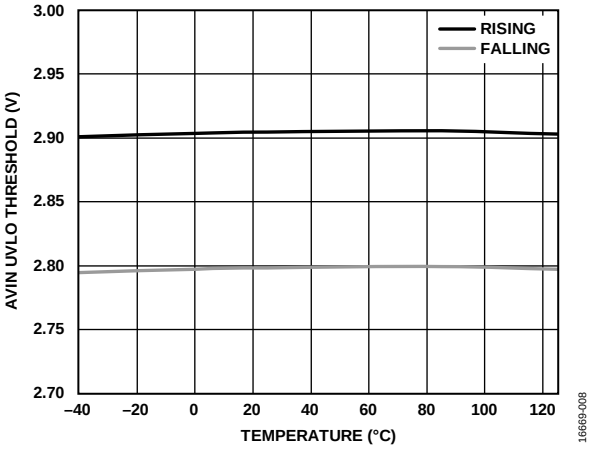


Figure 8. AVIN UVLO Threshold vs. Temperature

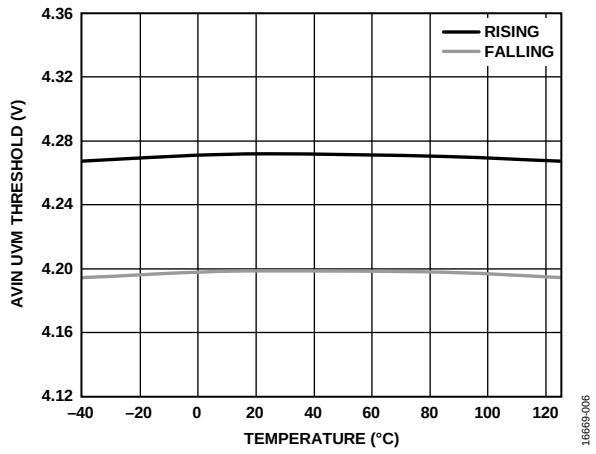


Figure 6. AVIN UVM Threshold vs. Temperature

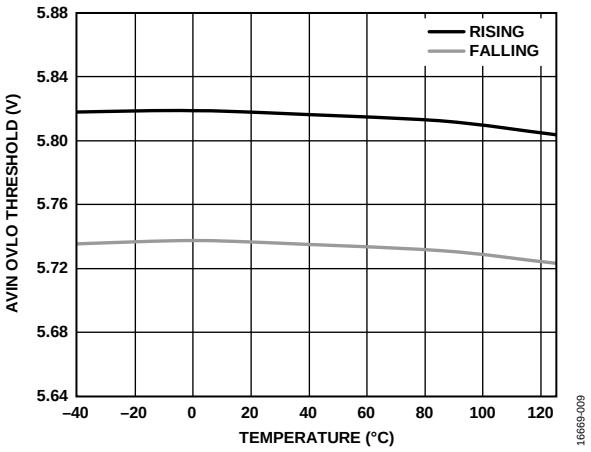


Figure 9. AVIN OVLO Threshold vs. Temperature

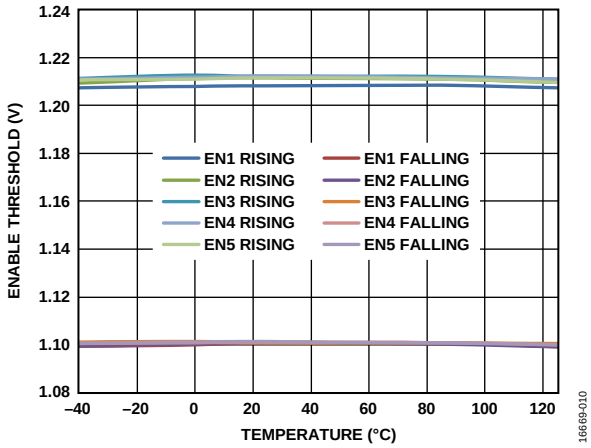


Figure 10. Enable Threshold vs. Temperature

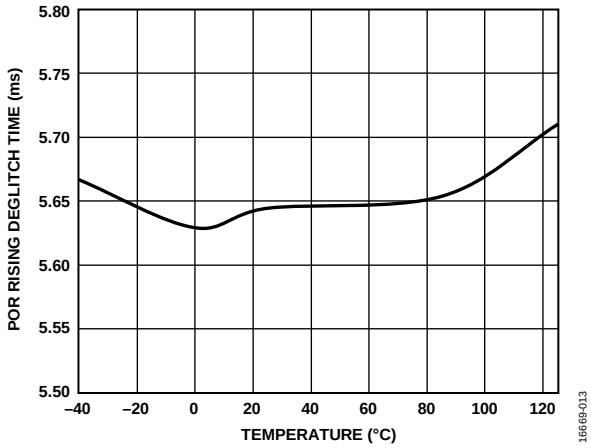


Figure 13. POR Rising Deglitch Time vs. Temperature

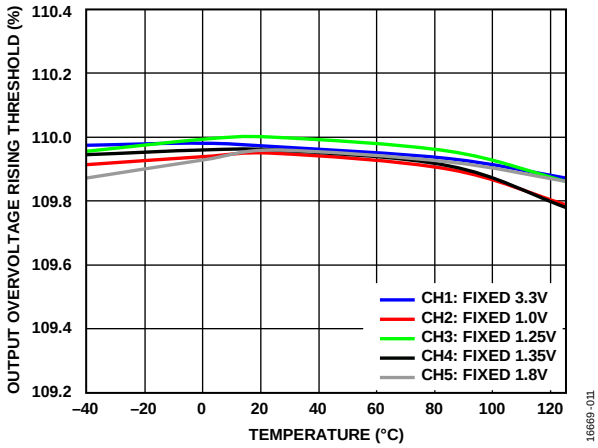


Figure 11. Output Overvoltage Rising Threshold vs. Temperature

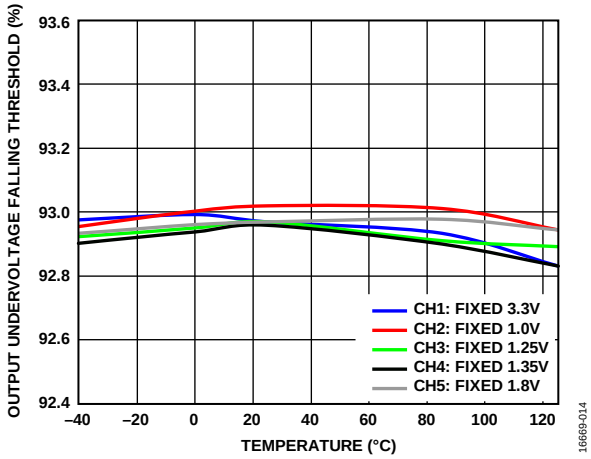


Figure 14. Output Undervoltage Falling Threshold vs. Temperature

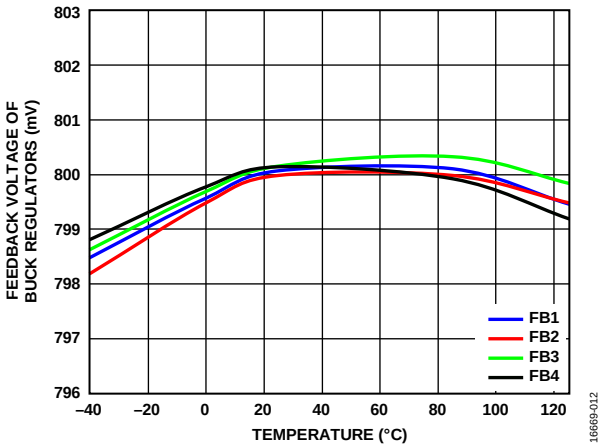


Figure 12. Feedback Voltage of Buck Regulators vs. Temperature

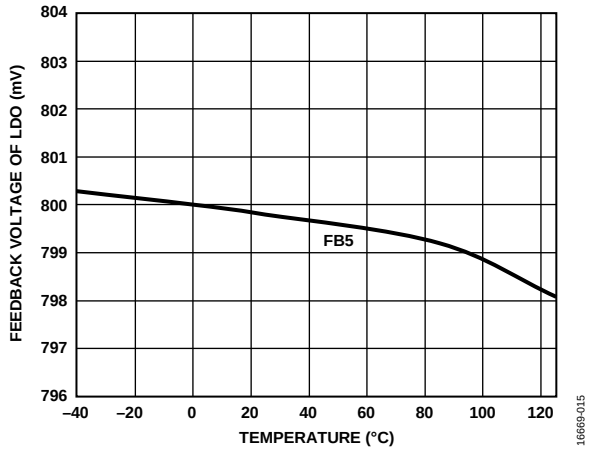


Figure 15. Feedback Voltage of LDO vs. Temperature

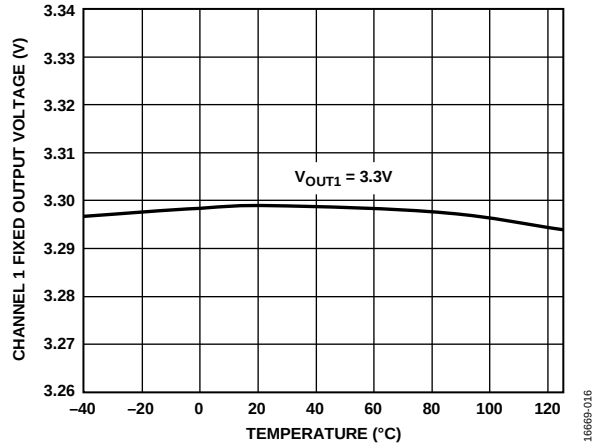


Figure 16. Channel 1 Fixed Output Voltage vs. Temperature

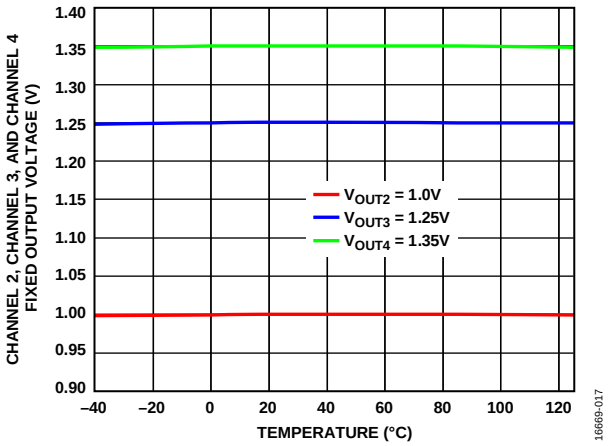


Figure 17. Channel 2, Channel 3, and Channel 4 Fixed Output Voltage vs. Temperature

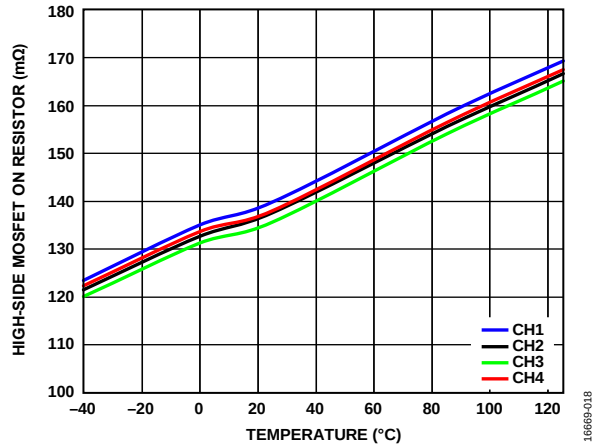


Figure 18. High-Side Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) On Resistor vs. Temperature

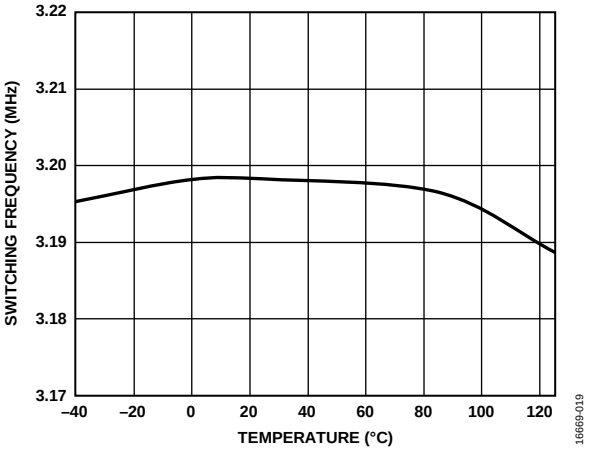


Figure 19. Switching Frequency vs. Temperature

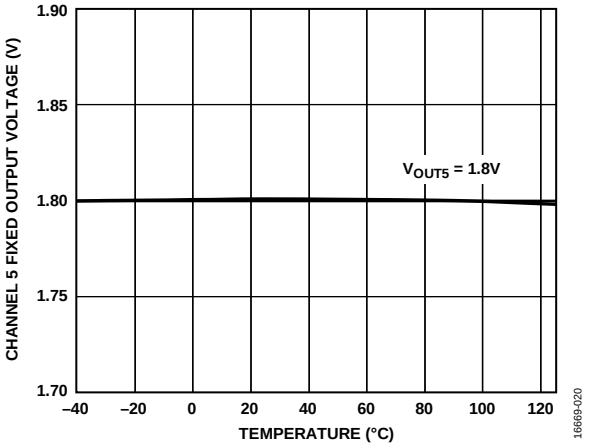


Figure 20. Channel 5 Fixed Output Voltage vs. Temperature

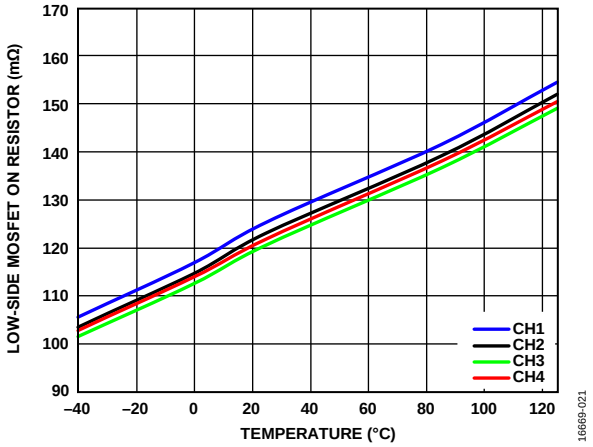


Figure 21. Low-Side MOSFET On Resistor vs. Temperature

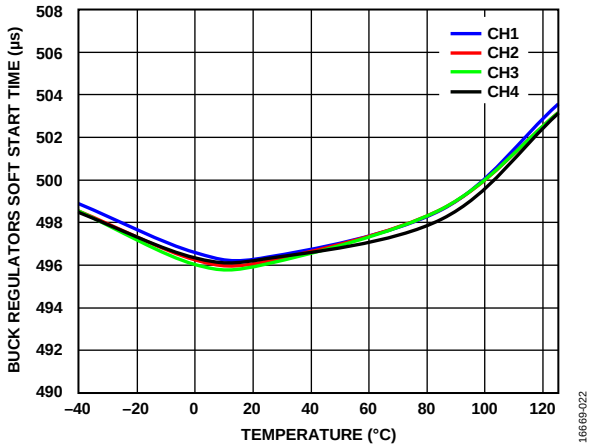


Figure 22. Buck Regulators Soft Start Time vs. Temperature

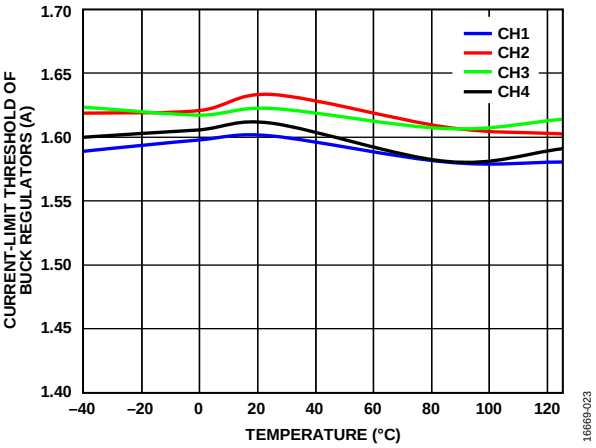


Figure 23. Current-Limit Threshold of Buck Regulators vs. Temperature

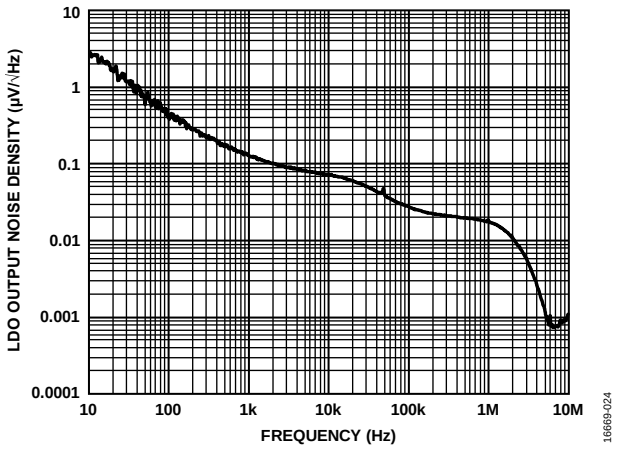


Figure 24. LDO Output Noise Density vs. Frequency at V_{PVIN5} = 5 V, I_{OUT5} = 250 mA, V_{OUT5} = 1.8 V, Adjustable Output Option

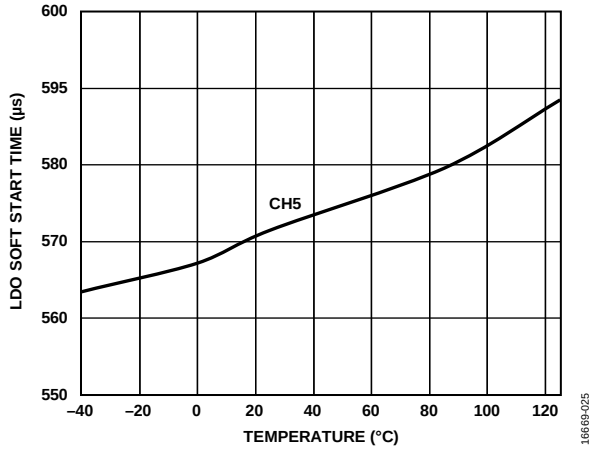


Figure 25. LDO Soft Start Time vs. Temperature

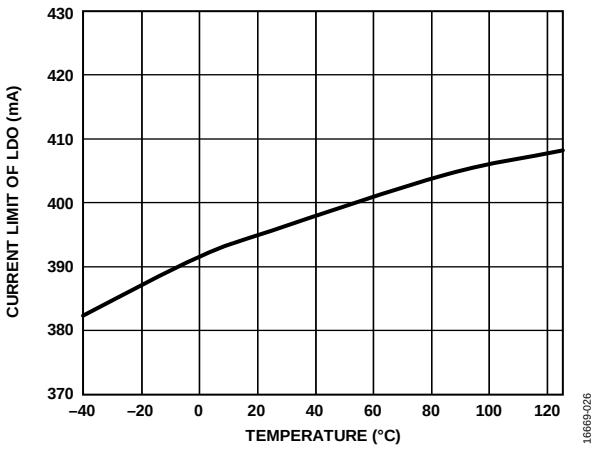


Figure 26. Current Limit of LDO vs. Temperature

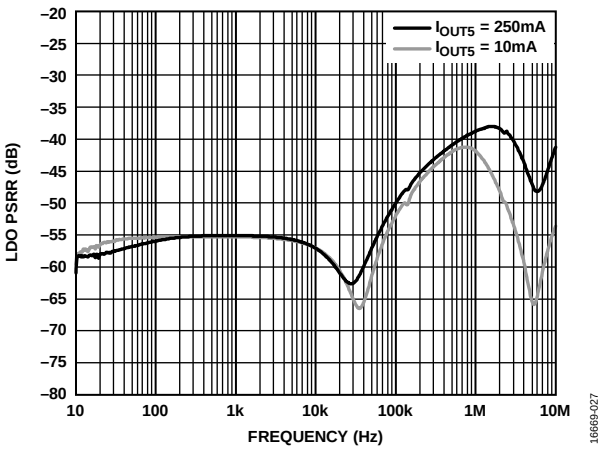


Figure 27. LDO PSRR vs. Frequency at V_{PVIN5} = 5 V, V_{OUT5} = 1.8 V, Adjustable Output Option

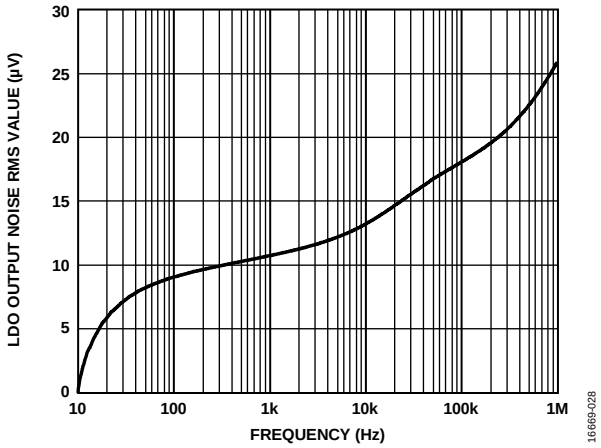


Figure 28. LDO Output Noise RMS Value vs. Frequency at V_{PVIN5} = 5 V, I_{OUT5} = 250 mA, V_{OUT5} = 1.8 V, Adjustable Output Option

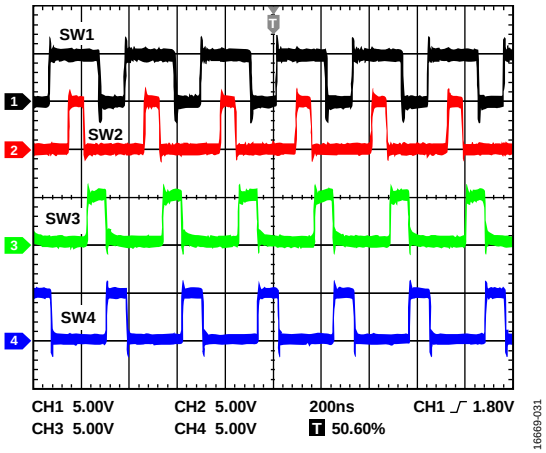


Figure 31. Phase Shift

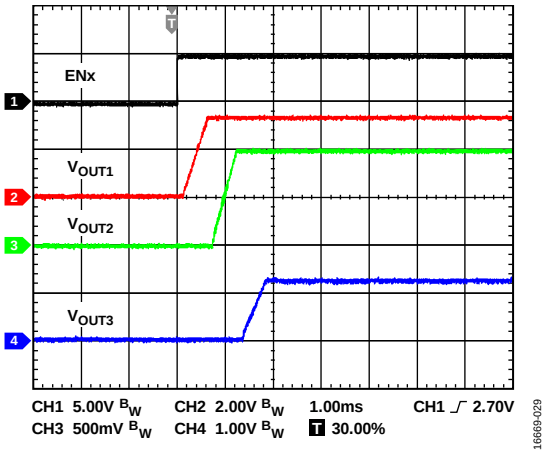


Figure 29. Startup with Full Load (ENx, V_{OUT1}, V_{OUT2}, and V_{OUT3})

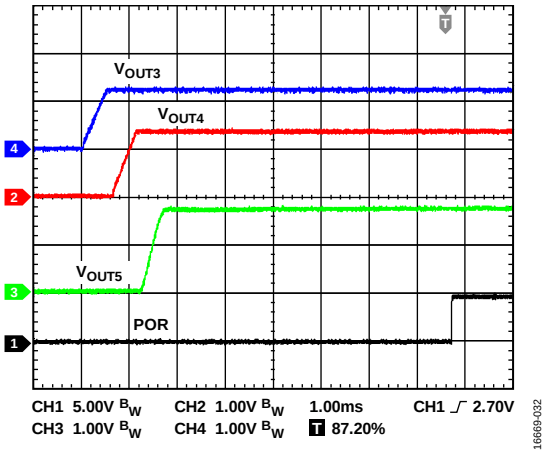


Figure 32. Startup with Full Load (V_{OUT3}, V_{OUT4}, V_{OUT5}, and POR)

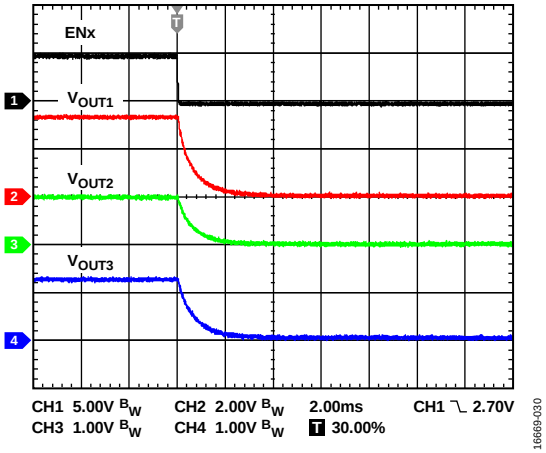


Figure 30. Shutdown at No Load (ENx, V_{OUT1}, V_{OUT2}, and V_{OUT3})

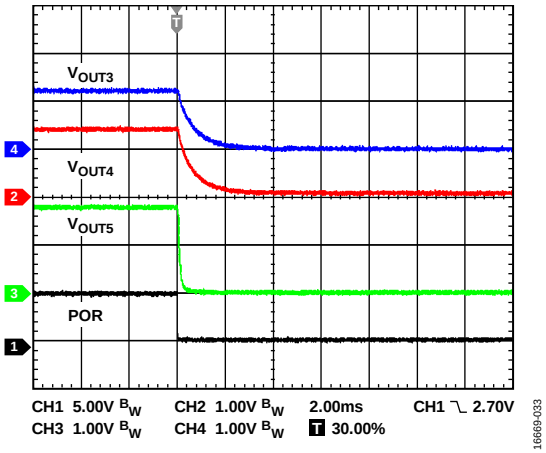


Figure 33. Shutdown at No Load (V_{OUT3}, V_{OUT4}, V_{OUT5}, and POR)

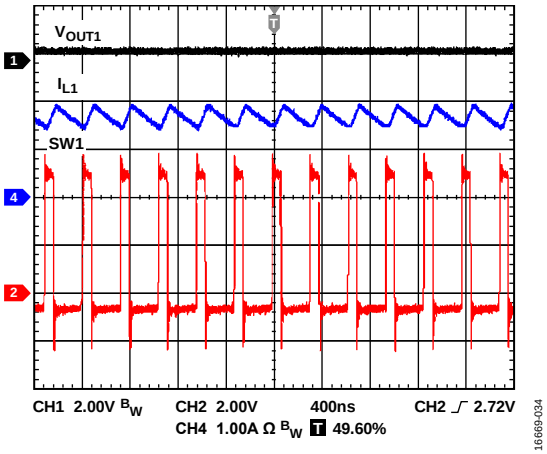


Figure 34. Overcurrent Protection (I_{L1} is Channel 1 Inductor Current)

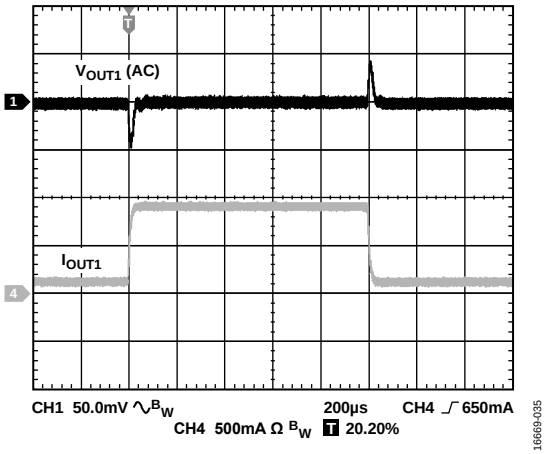


Figure 35. Load Transient Response of Channel 1 (3.3 V), 0.1 A to 0.9 A

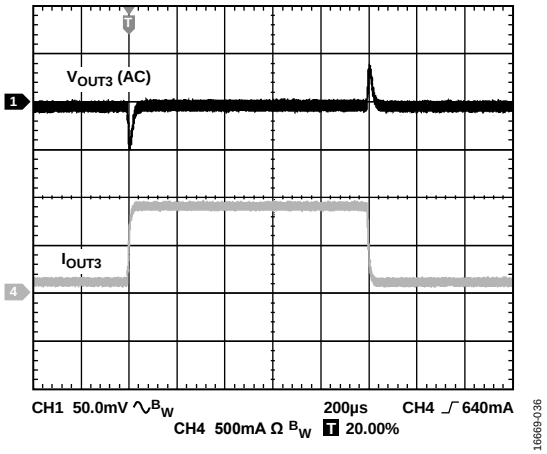


Figure 36. Load Transient Response of Channel 3 (1.25 V), 0.1 A to 0.9 A

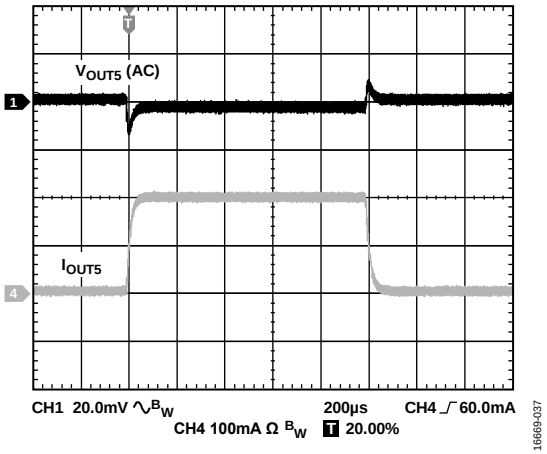


Figure 37. Load Transient Response of Channel 5 (1.8 V), 0 A to 0.2 A

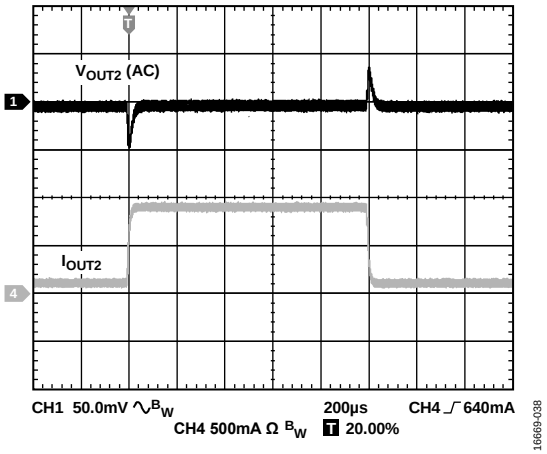


Figure 38. Load Transient Response of Channel 2 (1.0 V), 0.1 A to 0.9 A

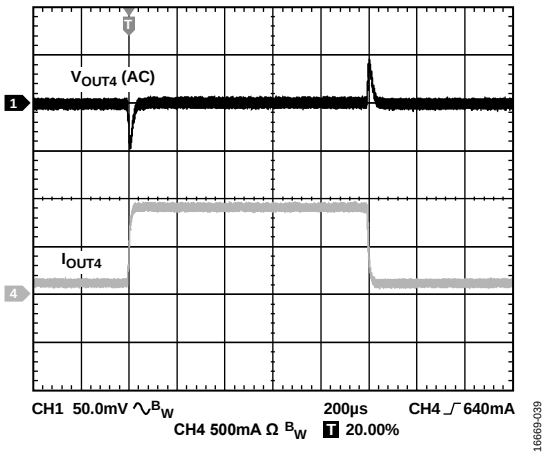


Figure 39. Load Transient Response of Channel 4 (1.35 V), 0.1 A to 0.9 A

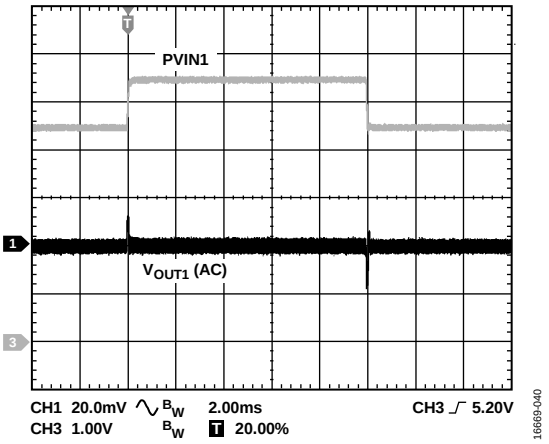


Figure 40. Line Transient Response of Channel 1 (3.3 V), PVIN1 from 4.5 V to 5.5 V, 1 A Load Current

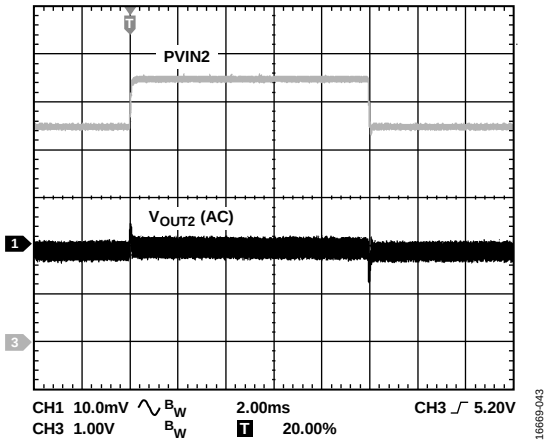


Figure 43. Line Transient Response of Channel 2 (1.0 V), PVIN2 from 4.5 V to 5.5 V, 1 A Load Current

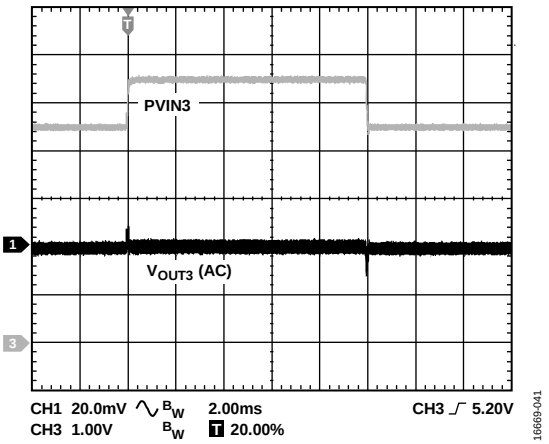


Figure 41. Line Transient Response of Channel 3 (1.25 V), PVIN3 from 4.5 V to 5.5 V, 1 A Load Current

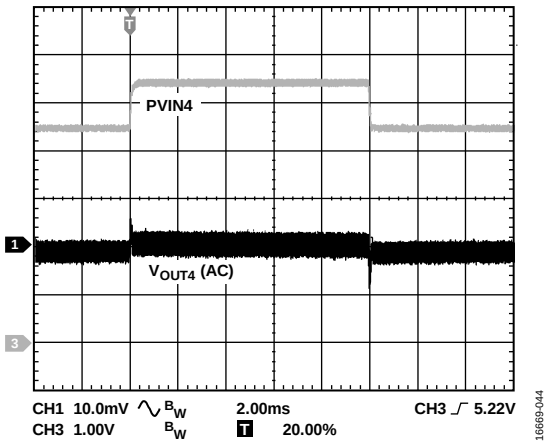


Figure 44. Line Transient Response of Channel 4 (1.35 V), PVIN4 from 4.5 V to 5.5 V, 1 A Load Current

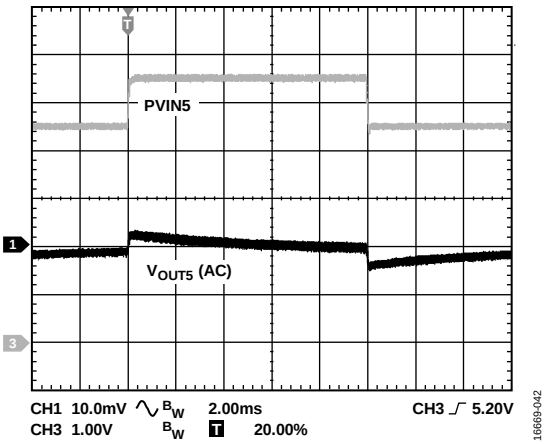


Figure 42. Line Transient Response of Channel 5 (1.8 V), PVIN5 from 4.5 V to 5.5 V, 250 mA Load Current

THEORY OF OPERATION

The ADP5138 is a power management IC that integrates four buck regulators and one low noise LDO in a 28-lead LFCSP package. The device can operate with a PVINx input voltage from 3 V to 5.5 V and can regulate the output voltage down to 0.8 V or set by factory. It provides input UVLO, OVLO, and UVM features. The ADP5138 also monitors the output voltage and provides the POR output.

CONTROL SCHEME

The ADP5138 uses a fixed frequency, peak current mode, PWM control architecture. At the start of each oscillator cycle, the high-side field effect transistor (FET) turns on, placing a positive voltage across the inductor. The inductor current increases until the current sense signal crosses the peak inductor current threshold that turns off the high-side FET and turns on the low-side FET, which, in turn, places a negative voltage across the inductor, causing the inductor current to reduce. The low-side FET stays on for the remainder of the cycle.

PRECISION ENABLE AND SHUTDOWN

The ADP5138 has five independent enable pins (ENx) for each channel. The ENx pins are precision analog inputs that enable the regulator when the voltage on ENx exceeds 1.2 V (typical). When the ENx voltage falls below 1.1 V (typical), the regulator turns off. An internal pull-down resistor (1 MΩ) prevents the regulator from being accidentally enabled if ENx is left floating.

To force the ADP5138 to automatically start when the input power is applied, connect ENx to PVINx.

OSCILLATOR AND PHASE SHIFT

The buck regulators in the ADP5138 run at a 3.2 MHz fixed switching frequency. For Channel 2 to Channel 4, the phase shift with respect to Channel 1 is set to 90°, which reduces the input ripple current and the input capacitance, thereby helping to lower system EMI.

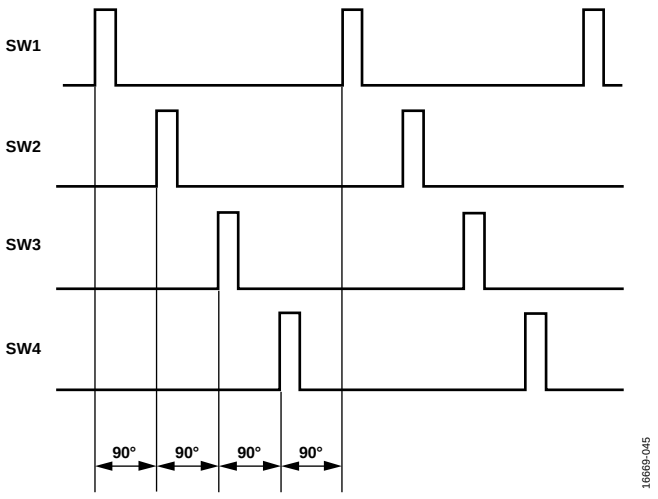


Figure 45. Even Phase Shift Between Channel 1 and Channel 4

SYNCHRONIZATION

To synchronize the ADP5138, connect an external clock to the SYNC pin. The external clock frequency can be in the 2.8 MHz to 3.5 MHz range. During synchronization, Channel 1 runs in phase with the external clock.

If the synchronization function is not used, connect the SYNC pin to ground.

INPUT OVERVOLTAGE LOCKOUT (OVLO)

The ADP5138 integrates an input overvoltage lockout circuit on the input supply. When the input voltage, V_{AVIN}, exceeds 5.8 V (typical), an OVLO event is detected, all the regulators are turned off, and the POR is pulled down to ground. When the input voltage falls back to 5.72 V (typical) or less, the OVLO releases and a soft start reinitializes.

INPUT UNDERVOLTAGE MONITOR (UVM)

The ADP5138 integrates an input undervoltage monitoring circuit on the input supply. When the input voltage, V_{AVIN}, drops below 4.2 V (typical), the POR pin pulls down to ground while the device still works until the input voltage drops down to the input voltage UVLO threshold. When the input voltage exceeds 4.28 V (typical), the POR pin pulls high after a POR rising delay time, $t_{POR\_DELAY\_R}$, if all other conditions are met.

INPUT UNDERVOLTAGE LOCKOUT (UVLO)

The ADP5138 integrates an input undervoltage lockout circuit on the input supply. When the input voltage, V_{AVIN}, drops below 2.8 V (typical), an input UVLO event is detected, all the regulators turn off, and the POR pin pulls down to ground. When the input voltage recovers from the UVLO event and the input voltage exceeds 2.9 V (typical), a soft start reinitializes.

OUTPUT VOLTAGE POWER-GOOD

Each of the five regulators integrates an output voltage power-good monitoring circuit.

When the output voltage drops below the undervoltage falling threshold (93% of the nominal output voltage), an output undervoltage event is detected, and the power-good signal becomes low. When the output voltage rises above the undervoltage rising threshold (95% of the nominal output voltage), the power-good signal becomes high.

When the output voltage exceeds the overvoltage rising threshold (110% of the nominal output voltage), an output overvoltage event is detected. During the output overvoltage, the corresponding regulator stops switching, and the power-good signal becomes low. When the output voltage drops below the overvoltage falling threshold (108% of the nominal output voltage), the corresponding regulator recovers to normal operation, and the power-good signal becomes high.

POWER-ON RESET (POR)

The ADP5138 integrates the POR circuit to monitor the input voltage and output voltage of the regulators. The POR pin is an active high, open-drain output that requires a resistor to pull the pin up to a voltage.

The ENx pin voltage determines which output voltage is monitored in the POR circuit. When the ENx pin voltage exceeds 1.2 V (typical), the POR circuit monitors the corresponding output voltage. When the ENx pin voltage is lower than 1.1 V (typical), the POR circuit does not monitor the corresponding output voltage.

The POR pin does not pull high until all of the following conditions are met followed by a 5.7 ms (typical) delay:

- The input voltage is greater than the undervoltage lockout threshold and undervoltage monitor threshold.
- The input voltage is less than the input overvoltage threshold.
- No thermal shutdown.
- All the power-good signals are high for these monitored output voltages.

The POR pin is pulled down when any of these conditions are not met with a 10 µs deglitch time.

If all the channels are disabled, the POR pin pulls down to ground.

The POR output is fully controlled when the voltage on AVIN is higher than V_{AVIN_POR}.

SOFT START AND POWER-UP SEQUENCE

The ADP5138 has integrated soft start circuitry for each channel to limit the output voltage rising time and to reduce the inrush current during startup. The soft start time is fixed at 500 µs (typical) for the buck regulators and 570 µs (typical) for the LDO regulator.

When the ADP5138 exits the input UVLO, input OVLO, or thermal shutdown event, there is a fixed delay time on each enable signal. This delay time prevents all the regulators from powering up at the same time and reduces the input inrush current. Table 7 shows the delay time for each channel.

Table 7. Enable Delay Time for Each Channel

Channel	Delay Time
Channel 1	15 µs
Channel 2	t_{SS_D}
Channel 3	$2 \times t_{SS\_D}$
Channel 4	$3 \times t_{SS\_D}$
Channel 5	$4 \times t_{SS\_D}$

Figure 46 shows the power-up sequence when the ENx pins are pulled up at the same time. Channel 1 powers up first, followed by Channel 2, Channel 3, Channel 4, and Channel 5.

Figure 47 shows the power-up sequence when the channels are enabled at different times.

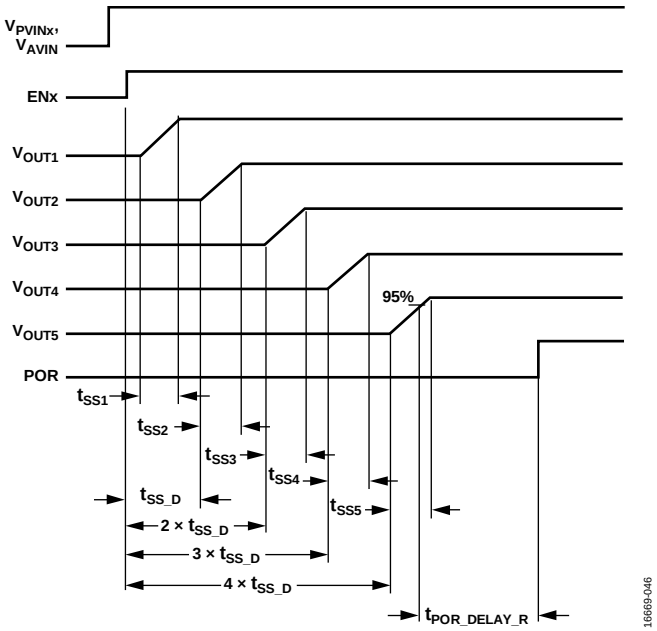


Figure 46. Power-Up Sequence with All Channels Enabled at Same Time

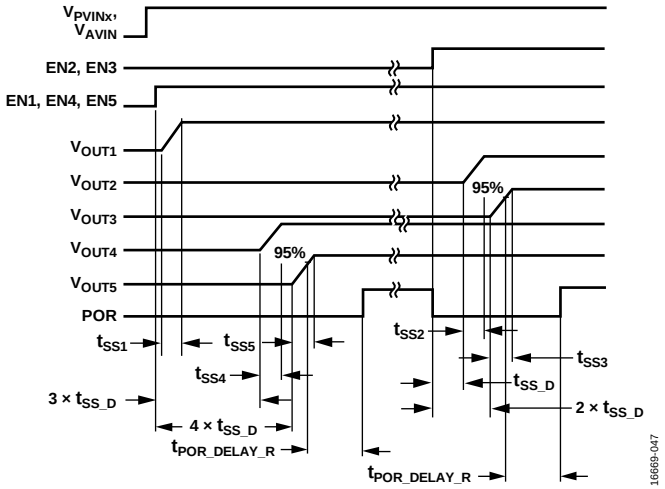


Figure 47. Power-Up Sequence with Channels Enabled at Different Times

CURRENT-LIMIT AND SHORT-CIRCUIT PROTECTION

The ADP5138 integrates a cycle by cycle, peak current-limit protection circuit to prevent current runaway for each buck regulator. The high-side FET peak current is limited to 1.6 A (typical). When the peak inductor current reaches the current-limit threshold, the high-side FET turns off, the low-side FET turns on, and the output reference voltage decreases.

The low-side FET in the buck regulator can also sink current from the load. If the low-side sink current limit is exceeded, both the low-side and high-side FETs are turned off until the next cycle starts.

The LDO is designed to current limit when the output load reaches the current-limit threshold. When the output load exceeds the current-limit threshold, the output voltage is reduced to maintain a constant current limit.

ACTIVE OUTPUT DISCHARGE

Each of the five regulators in the ADP5138 integrates a discharge switch from the switching node to ground. This switch is turned on when its associated ENx pin is low, which helps to discharge the output capacitor quickly. The typical value of the discharge switch is 64 Ω for the buck regulators and 83 Ω for the LDO regulator.

THERMAL SHUTDOWN

In the event that the ADP5138 junction temperature exceeds 150°C, the thermal shutdown circuit turns off the device. A 15°C hysteresis is included so that the ADP5138 does not recover from thermal shutdown until the on-chip temperature drops below 135°C. Upon recovery, a soft start and the power-up sequence are initiated prior to normal operation.

APPLICATIONS INFORMATION

INPUT CAPACITOR SELECTION

The input capacitor reduces the input voltage ripple caused by the switch current on PVINx. Place the input capacitor as close as possible to the PVINx pin. A ceramic capacitor in the 10 µF to 47 µF range is recommended. The loop composed of the input capacitor, the high-side MOSFET, and the low-side MOSFET must be kept as small as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. Ensure that the rms current rating of the input capacitor is larger than the value calculated from the following equation:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

where:
I_{OUT} is the output current.
D is the duty cycle ($D = V_{OUT}/V_{IN}$).

OUTPUT VOLTAGE SETTING

The output voltage (V_{OUT}) of the ADP5138 can be factory set or programmed by an external resistor divider.

If the output voltage is factory set, connect the FBx pin to the output voltage directly.

If the output voltage is programmable, use the following equation to set the output voltage:

$$V_{OUT} = 0.8 \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

where:
R_{TOP} is the top resistor of the resistor divider.
R_{BOT} is the bottom resistor of the resistor divider.

Table 8. Resistor Divider Values for Various Output Voltages

V_{OUT} (V)	R_{TOP} ± 1% (kΩ)	R_{BOT} ± 1% (kΩ)
1.0	4.99	20
1.2	10	20
1.5	10	11.5
1.8	18.7	15
2.5	24.3	11.5
3.3	35.7	11.5

INDUCTOR SELECTION

The inductor value is determined by the operating frequency, input voltage, output voltage, and inductor ripple current. Using a small inductor value leads to a faster transient response but degrades efficiency due to a larger inductor ripple current. Using a large inductor value leads to a smaller ripple current and better efficiency but results in a slower transient response.

As a guideline, an inductor with its value in the range from 0.68 µH to 2.2 µH is recommended for the best balance between transient and efficiency performance. The inductor ripple current, ΔI_L, is typically set to one-third of the maximum load current.

Use the following equation to calculate the inductor value:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

where:
V_{IN} is the input voltage.
V_{OUT} is the output voltage.
D is the duty cycle ($D = V_{OUT}/V_{IN}$).
ΔI_L is the inductor current ripple.
f_{SW} is the switching frequency.

Use the following equation to calculate the peak inductor current:

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

The saturation current of the inductor must be larger than the peak inductor current. For ferrite core inductors with a quick saturation characteristic, the saturation current rating of the inductor must be higher than the current-limit threshold of the switch to prevent the inductor from reaching saturation.

Use the following equation to calculate the rms current of the inductor:

$$I_{RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}}$$

Shielded ferrite core materials are recommended for low core loss and low EMI.

OUTPUT CAPACITOR SELECTION

The output capacitor selection affects both the output voltage ripple and the loop dynamics of the regulator. The ADP5138 operates with small ceramic capacitors that have low equivalent series resistance (ESR) and low equivalent series inductance (ESL) and can, therefore, easily meet the output voltage ripple specifications.

When the regulator operates in continuous conduction mode, the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by the charging and discharging of the output capacitor.

$$\Delta V_{RIPPLE} = \Delta I_L \times \left(\frac{1}{8 \times f_{SW} \times C_{OUT}} + ESR_{C_{OUT}}\right)$$

where:
ΔV_{RIPPLE} is the output voltage ripple.
C_{OUT} is the output capacitance.

Capacitors with lower ESR are preferable to guarantee low output voltage ripple, as shown in the following equation:

$$ESR_{C_{OUT}} \leq \frac{\Delta V_{RIPPLE}}{\Delta I_L}$$

Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. X5R or X7R dielectrics are recommended for best performance due to the low ESR and small temperature coefficients.

APPLICATION CIRCUIT

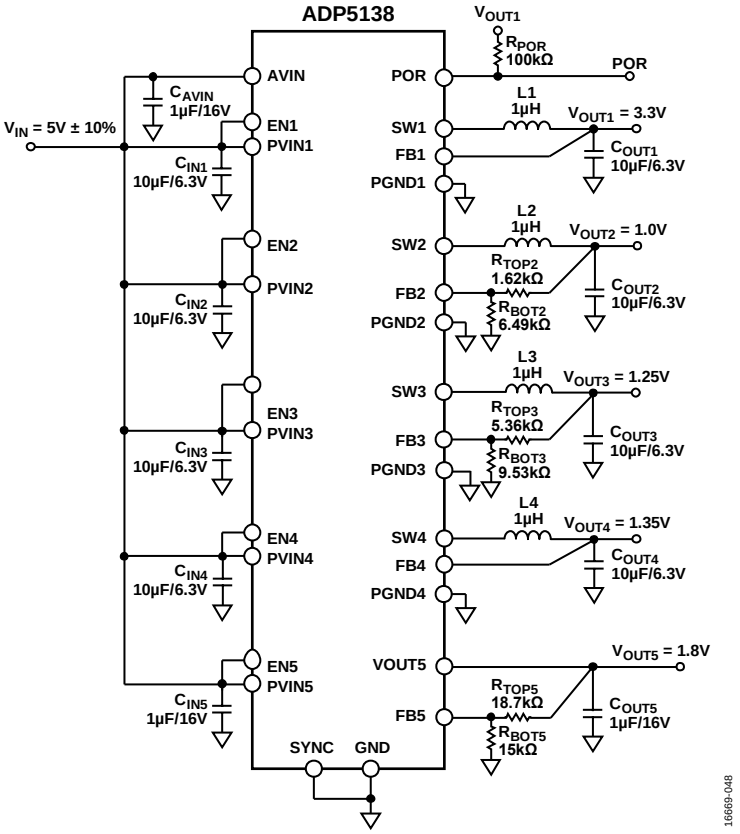


Figure 48. Application Circuit

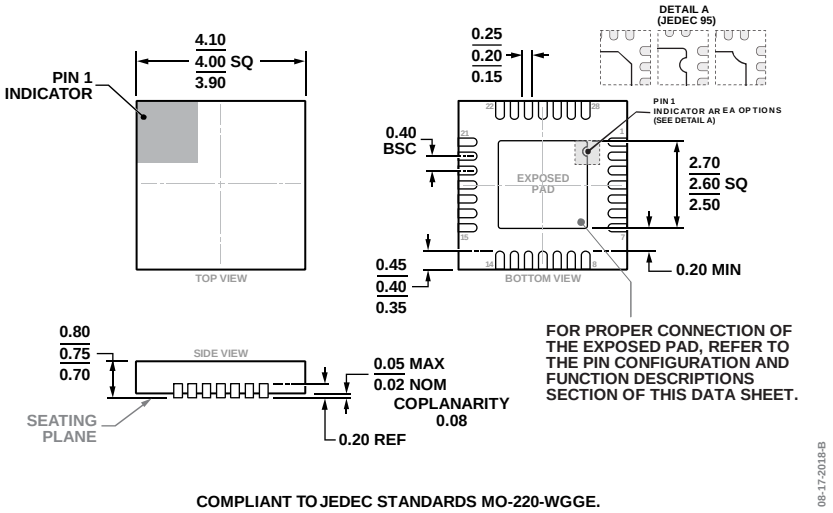
FACTORY-PROGRAMMABLE OPTIONS

The output of each buck regulator and the LDO can be preset to one of the options listed in Table 9. There are 15 fixed options and one adjustable option. To order a device with options other than the default options listed in the Ordering Guide, contact a local Analog Devices, Inc., sales or distribution representative.

Table 9. Output Voltage Fuse-Selectable Trim Options

Parameter	Output Voltage Trim Options (V)
Buck Regulator 1	Adjustable, 0.9, 0.95, 1.0, 1.05, 1.1, 1.15, 1.2, 1.25, 1.35, 1.5, 1.8, 2.5, 2.65, 3.0, 3.3
Buck Regulator 2	Adjustable, 0.9, 0.95, 1.0, 1.05, 1.1, 1.15, 1.2, 1.25, 1.35, 1.5, 1.8, 2.5, 2.65, 3.0, 3.3
Buck Regulator 3	Adjustable, 0.9, 0.95, 1.0, 1.05, 1.1, 1.15, 1.2, 1.25, 1.35, 1.5, 1.8, 2.5, 2.65, 3.0, 3.3
Buck Regulator 4	Adjustable, 0.9, 0.95, 1.0, 1.05, 1.1, 1.15, 1.2, 1.25, 1.35, 1.5, 1.8, 2.5, 2.65, 3.0, 3.3
LDO	Adjustable, 1.0, 1.05, 1.1, 1.15, 1.2, 1.25, 1.3, 1.5, 1.8, 2.5, 2.65, 2.8, 2.85, 3.0, 3.3

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGE.

Figure 49. 28-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-28-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Output Voltage (V)[4]					Temperature Range	Package Description	Package Option
	Buck 1	Buck 2	Buck 3	Buck 4	LDO			
ADP5138WACPZ-1-R7	3.3	ADJ	ADJ	1.35	ADJ	−40°C to +125°C	28-Lead LFCSP	CP-28-5
ADP5138ACPZ-2-R7	ADJ	ADJ	ADJ	ADJ	ADJ	−40°C to +125°C	28-Lead LFCSP	CP-28-5
ADP5138W-1-EVALZ	3.3	ADJ	ADJ	1.35	ADJ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] To order a device with options other than the two default options listed in the ordering guide, contact a local Analog Devices sales or distribution representative.
[4] ADJ means adjustable.

AUTOMOTIVE PRODUCTS

The ADP5138W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for this model.

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