Dual-Channel, 1.8 GHz to 2.8 GHz, Receiver Front End

Data Sheet **ADRF5549**

FEATURES

- Integrated dual-channel RF front end
  - 2-stage LNA and high power SPDT switch
  - On-chip bias and matching
  - Single-supply operation
- Gain
  - High gain mode: 35 dB typical at 2.3 GHz
  - Low gain mode: 17 dB typical at 2.3 GHz
- Low noise figure
  - High gain mode: 1.4 dB typical at 2.3 GHz
  - Low gain mode: 1.4 dB typical at 2.3 GHz
- High isolation
  - Between RxOUT-ChA and RxOUT-ChB: 50 dB typical
  - Between TERM-ChA and TERM-ChB: 62 dB typical
- Low insertion loss: 0.6 dB typical at 2.3 GHz
- High power handling at T_{CASE} = 105°C
  - Full lifetime
    - LTE average power (9 dB PAR): 40 dBm
  - Single event (<10 sec operation)
    - LTE average power (9 dB PAR): 43 dBm
- High OIP3: 32 dBm typical
- Power-down mode and low gain mode for LNA
- Low supply current
  - High gain mode: 85 mA typical at 5V
  - Low gain mode: 35 mA typical at 5 V
  - Power-down mode: 12 mA typical at 5 V
- Positive logic control
- 6 mm × 6 mm, 40-lead LFCSP

APPLICATIONS

- Wireless Infrastructure
- TDD massive multiple input and multiple output (MIMO) and active antenna systems
- TDD-based communication systems

GENERAL DESCRIPTION

The ADRF5549 is a dual-channel, integrated, RF front-end multichip module designed for time division duplexing (TDD) applications that operates from 1.8 GHz to 2.8 GHz. The ADRF5549 is configured in dual channels with a cascading, two-stage, low noise amplifier (LNA) and a high power, silicon single-pole, double-throw (SPDT) switch.

In high gain mode, the cascaded two-stage LNA and switch offer a low noise figure of 1.4 dB and a high gain of 35 dB with an output third-order intercept point (OIP3) of 32 dBm typical.

FUNCTIONAL BLOCK DIAGRAM

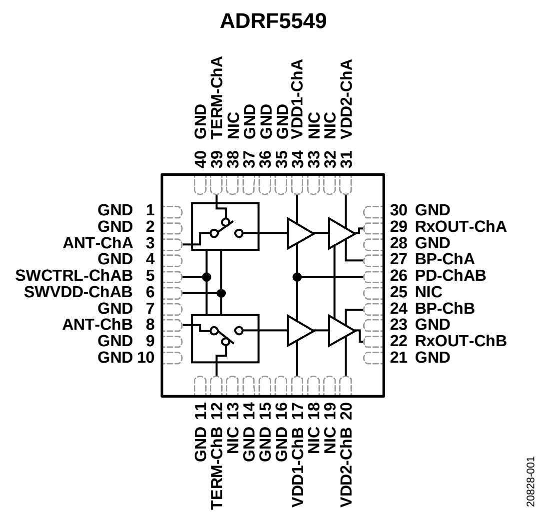

Figure 1.

In low gain mode, one stage of the two-stage LNA is in bypass mode providing 17 dB of gain at a lower current of 35 mA. In power-down mode, the LNAs are turned off, and the device draws 12 mA.

In transmit operation, when RF inputs are connected to a termination pin (TERM-ChA or TERM-ChB), the switch provides a low insertion loss of 0.6 dB and handles a long-term evolution (LTE) full lifetime average (9 dB peak to average ratio (PAR)) of 40 dBm and 43 dBm for a 9 dB PAR LTE single event (<10 sec) average. The device comes in a RoHS-compliant, compact, 6 mm × 6 mm, 40-lead, lead frame chip-scale package (LFCSP).

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TABLE OF CONTENTS

REVISION HISTORY

6/2020—Rev. 0 to Rev. A

Changes to Theory of Operation Section ... 13
Changes to Applications Information Section and Figure 28 ... 14

9/2019—Revision 0: Initial Version

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD1-ChA, VDD1-ChB, VDD2-ChA, VDD2-ChB, and SWVDD-ChAB = 5 V, SWCTRL-ChAB = 0 V or SWVDD-ChAB, BP-ChA = VDD1-ChA or 0 V, BP-ChB = VDD1-ChB or 0 V, PD-ChAB = 0 V or VDD1-ChA, and T_{CASE} = 25°C on a 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		1.8		2.8	GHz
GAIN[1]	Receive operation at 2.3 GHz				
High Gain Mode			35		dB
Low Gain Mode			17		dB
GAIN FLATNESS[1]	Receive operation in any 100 MHz bandwidth				
High Gain Mode			0.6		dB
Low Gain Mode			0.2		dB
NOISE FIGURE[1]	Receive operation at 2.3 GHz				
High Gain Mode			1.4		dB
Low Gain Mode			1.4		dB
OUTPUT THIRD-ORDER INTERCEPT POINT (OIP3)[1]	Receive operation, two-tone output power = 8 dBm per tone at 1 MHz tone spacing				
High Gain Mode			32		dBm
Low Gain Mode			25		dBm
OUTPUT 1 dB COMPRESSION (OP1dB)					
High Gain Mode			19		dBm
Low Gain Mode			13		dBm
INSERTION LOSS[1]	Transmit operation at 2.3 GHz		0.6		dB
Channel to Channel Isolation[1]	At 2.3 GHz				
Between RxOUT-ChA and RxOUT-ChB	Receive operation		50		dB
Between TERM-ChA and TERM-ChB	Transmit operation		62		dB
SWITCH ISOLATION					
ANT-ChA to TERM-ChA and ANT-ChB to TERM-ChB[1]	Transmit operation, PD-ChAB = 0 V		25		dB
SWITCHING CHARACTERISTICS (t_{ON}, t_{OFF})	50% control voltage to 90%, 10% of RxOUT-ChA or RxOUT-ChB in receive operation		860		ns
	50% control voltage to 90%, 10% of TERM-ChA or TERM-ChB in transmit operation		800		ns
RF INPUT POWER AT ANT-ChA, ANT-ChB[1]	Receive operation, LTE average (9 dB PAR)			15	dBm
RECOMMENDED OPERATING CONDITIONS					
Bias Voltage Range	VDD1-ChA, VDD1-ChB, VDD2-ChA, VDD2-ChB, and SWVDD-ChAB	4.75	5	5.25	V
Control Voltage Range[2]	SWCTRL-ChAB, BP-ChA, BP-ChB, PD-ChAB	0		VDD	V
RF Input Power at ANT-ChA, ANT-ChB	SWCTRL-ChAB = 5 V, PD-ChAB = 5 V, BP-ChA = BP-ChB = 0 V, T_{CASE} = 105°C[3]				
	Continuous wave			40	dBm
	9 dB PAR LTE full lifetime average			40	dBm
	9 dB PAR LTE single event (<10 sec) average			43	dBm
T_{CASE}[3]		−40		+105	°C
Junction Temperature at Maximum T_{CASE}[3]	Receive operation[1]			132	°C
	Transmit operation[1]			134	°C

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUTS					
SWCTRL-ChAB and PD-ChAB					
Low (V_{IL})		0		0.7	V
High (V_{IH})[2]		1.4		VDD	V
BP-ChA and BP-ChB					
Low (V_{IL})		0		0.3	V
High (V_{IH})[2]		1.0		VDD	V
SUPPLY CURRENT (I_{DD})	VDD1-Chx and VDD2-Chx = 5 V per channel				
High Gain Mode			85		mA
Low Gain Mode			35		mA
Power-Down Mode			12		mA
Transmit Current (Switch)	SWVDD-ChAB = 5 V		4.3		mA
DIGITAL INPUT CURRENTS	SWCTRL-ChAB, PD-ChAB, BP-ChA, and BP-ChB = 5 V per channel				
SWCTRL-ChAB			0.0004		mA
PD-ChAB			0.2		mA
BP-ChA and BP-ChB			0.4		mA

[1] See Table 5 and Table 6.
[2] V_{DD} (shown in the maximum column) is the voltage of the SWVDD-CHAB, VDD1-CHA, VDD1-CHB, VDD2-CHA, and VDD2-CHB pins.
[3] T_{CASE} is measured at the exposed pad.

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ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Positive Supply Voltage	
VDD1-ChA, VDD1-ChB, VDD2-ChA, VDD2-ChB	7 V
SWVDD-ChAB	5.4 V
Digital Control Input Voltage	
SWCTRL-ChAB	−0.3 V to V_{DD}[1] + 0.3 V
BP-ChA, BP-ChB, and PD-ChAB	−0.3 V to V_{DD}[1] + 0.3 V
RF Input Power (LTE Peak)	
Transmit	53 dBm
Receive	25 dBm
Temperature	
Storage	−65°C to +150°C
Reflow (Moisture Sensitivity Level (MSL) 3 Rating)	260°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	1 kV, Class 1C
Charge Device Model (CDM)	1 kV

[1] V_{DD} is the voltage of the SWVDD-ChAB, VDD1-CHA, VDD1-CHB, VDD2-CHA, and VDD2-CHB pins.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operation environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-40-15		
High Gain Mode and Low Gain Mode	30	°C/W
Power-Down Mode	8.7	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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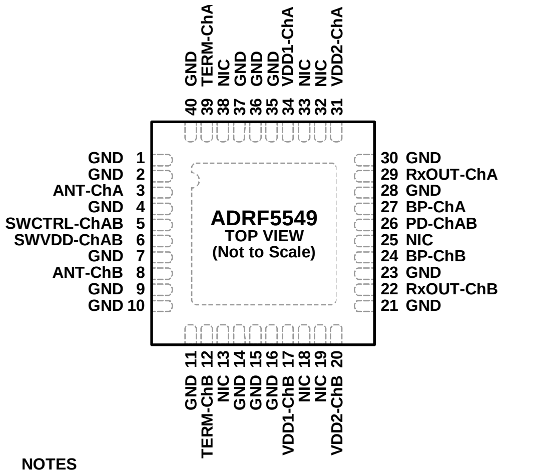
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED. IT IS RECOMMENDED TO CONNECT NIC TO THE RF GROUND OF THE PCB.
2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO RF OR DC GROUND.

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4, 7, 9 to 11, 14 to 16, 21, 23, 28, 30, 35 to 37, 40	GND	Ground. See Figure 3 for the interface schematic.
3	ANT-ChA	RF Input to Channel A.
5	SWCTRL-ChAB	Control Voltage for Switches on Channel A and Channel B. See Figure 7 for the interface schematic.
6	SWVDD-ChAB	Supply Voltage for Switches on Channel A and Channel B. See Figure 7 for the interface schematic.
8	ANT-ChB	RF Input to Channel B.
12	TERM-ChB	Termination Output. This pin is the transmitter path for Channel B.
13, 18, 19, 25, 32, 33, 38	NIC	Not Internally Connected. It is recommended to connect NIC to the RF ground of the PCB.
17	VDD1-ChB	Supply Voltage for Stage 1 LNA on Channel B. See Figure 5 for the interface schematic.
20	VDD2-ChB	Supply Voltage for Stage 2 LNA on Channel B. See Figure 5 for the interface schematic.
22	RxOUT-ChB	RF Output. This pin is the receiver path for Channel B. See Figure 4 for the interface schematic.
24	BP-ChB	Bypass Second Stage LNA of Channel B. See Figure 6 for the interface schematic.
26	PD-ChAB	Power-Down All Stages of LNA for Channel A and Channel B. See Figure 6 for the interface schematic.
27	BP-ChA	Bypass Second Stage LNA of Channel A. See Figure 6 for the interface schematic.
29	RxOUT-ChA	RF Output. This pin is the receiver path for Channel A. See Figure 4 for the interface schematic.
31	VDD2-ChA	Supply Voltage for Stage 2 LNA on Channel A. See Figure 5 for the interface schematic.
34	VDD1-ChA	Supply Voltage for Stage 1 LNA on Channel A. See Figure 5 for the interface schematic.
39	TERM-ChA	Termination Output. This pin is the transmitter path for Channel A.
	EPAD	Exposed Pad. The exposed pad must be connected to RF or dc ground.

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INTERFACE SCHEMATICS

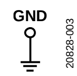

Figure 3. GND Interface Schematic

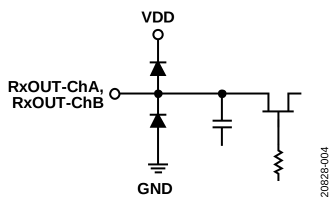

Figure 4. RxOUT-Chx Interface Schematic

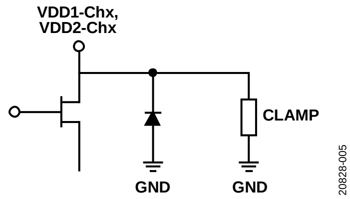

Figure 5. VDD1-Chx and VDD2-Chx Interface Schematic

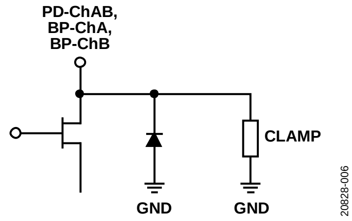

Figure 6. PD-ChAB and BP-Chx Interface Schematic

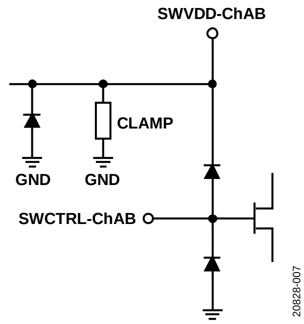

Figure 7. SWCTRL-ChAB and SWVDD-ChAB Interface Schematic

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TYPICAL PERFORMANCE CHARACTERISTICS

RECEIVE OPERATION

High Gain Mode

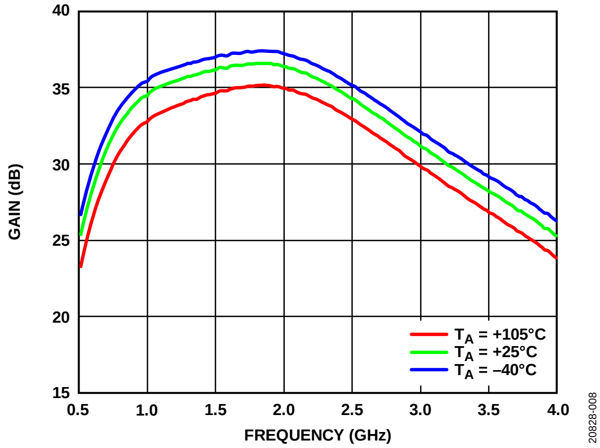

Figure 8. Gain vs. Frequency at Various Temperatures

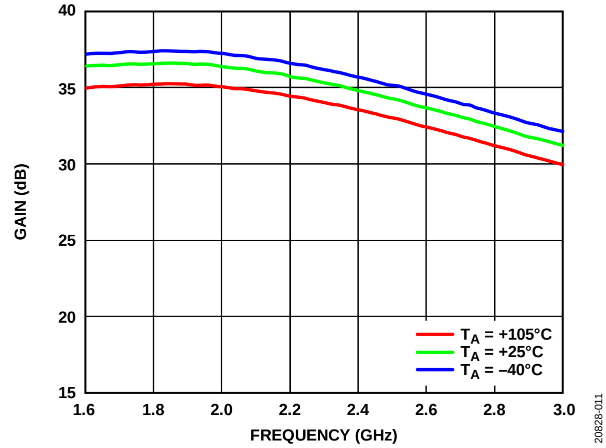

Figure 11. Gain vs. Frequency at Various Temperatures, 1.6 GHz to 3.0 GHz

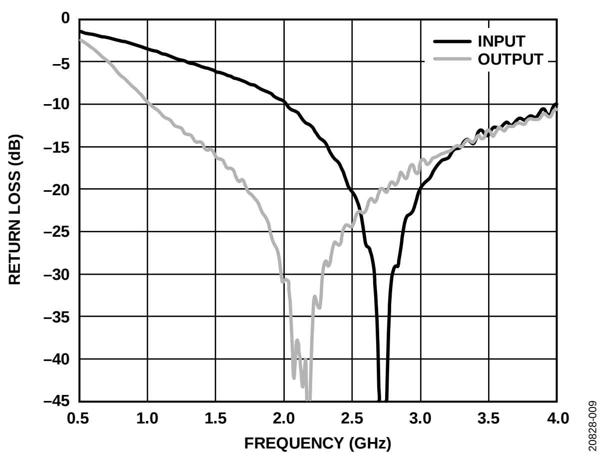

Figure 9. Return Loss vs. Frequency

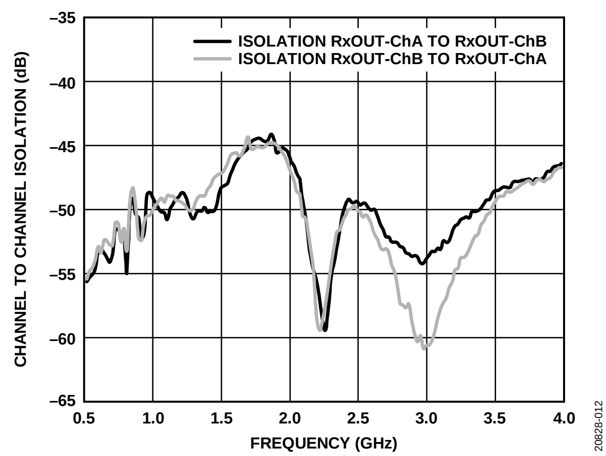

Figure 12. Channel to Channel Isolation vs. Frequency

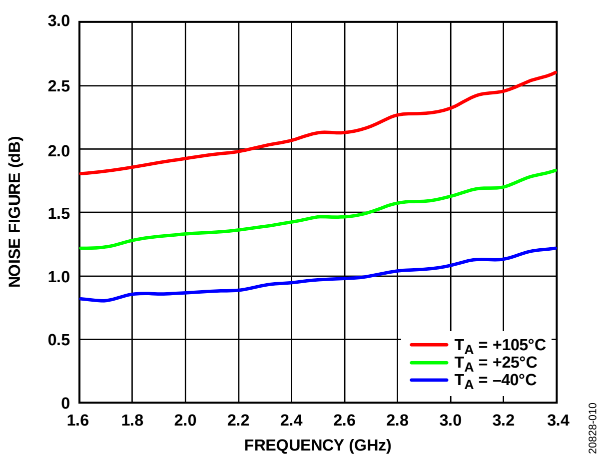

Figure 10. Noise Figure vs. Frequency at Various Temperatures

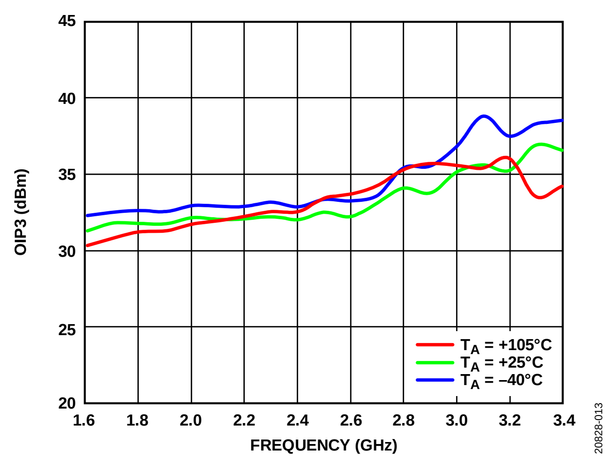

Figure 13. OIP3 vs. Frequency, 8 dBm Output Tone Power

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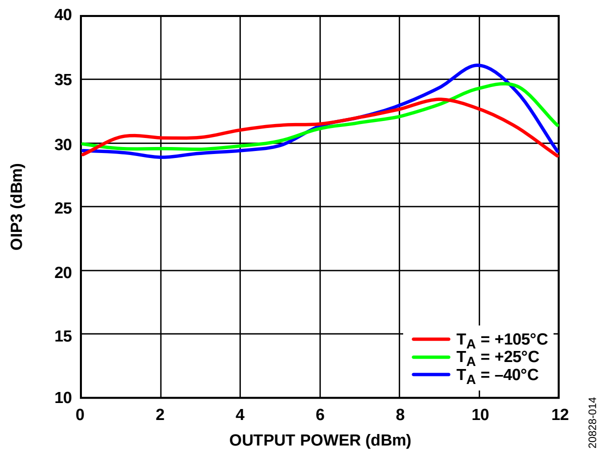

Figure 14. OIP3 vs. Output Power, 2.3 GHz

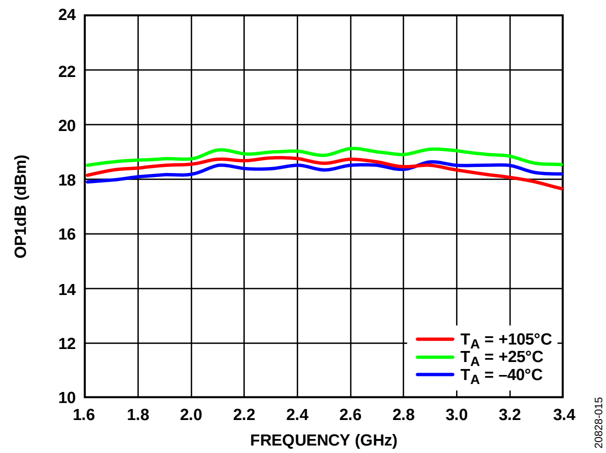

Figure 15. OP1dB vs. Frequency at Various Temperatures

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Low Gain Mode

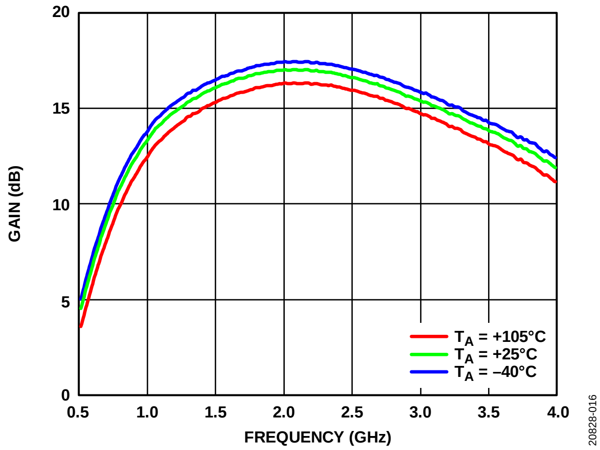

Figure 16. Gain vs. Frequency at Various Temperatures

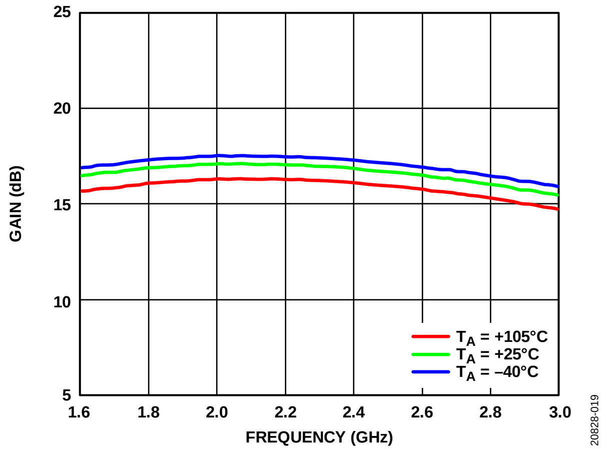

Figure 19. Gain vs. Frequency at Various Temperatures, 1.6 GHz to 3.0 GHz

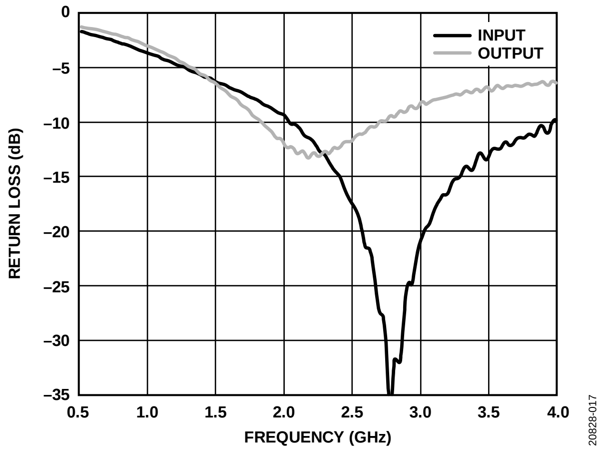

Figure 17. Return Loss vs. Frequency

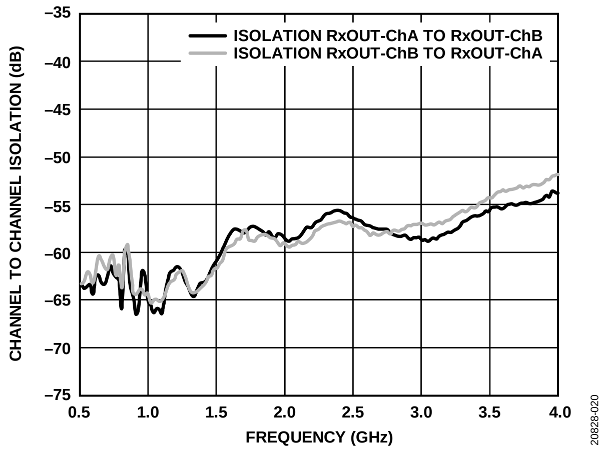

Figure 20. Channel to Channel Isolation vs. Frequency

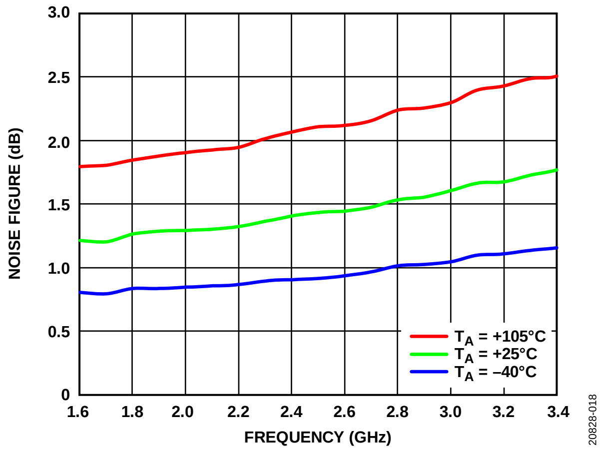

Figure 18. Noise Figure vs. Frequency at Various Temperatures

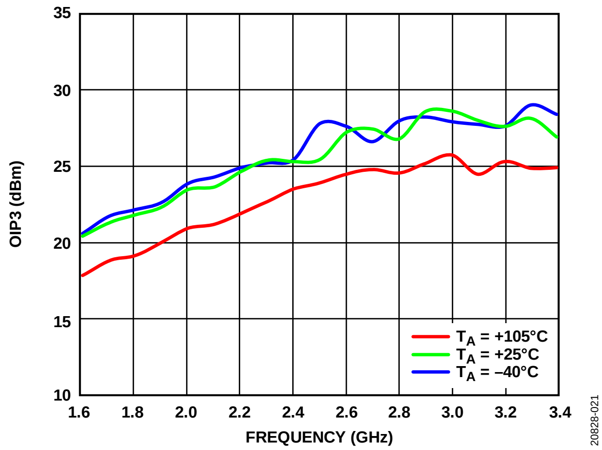

Figure 21. OIP3 vs. Frequency at −8 dBm Output Tone Power

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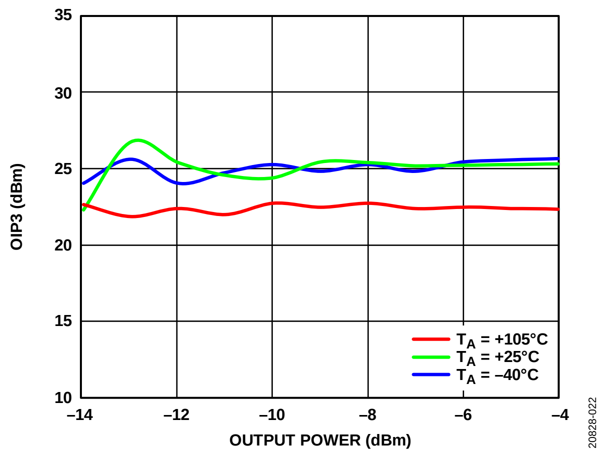

Figure 22. OIP3 vs. Output Power, 2.3 GHz

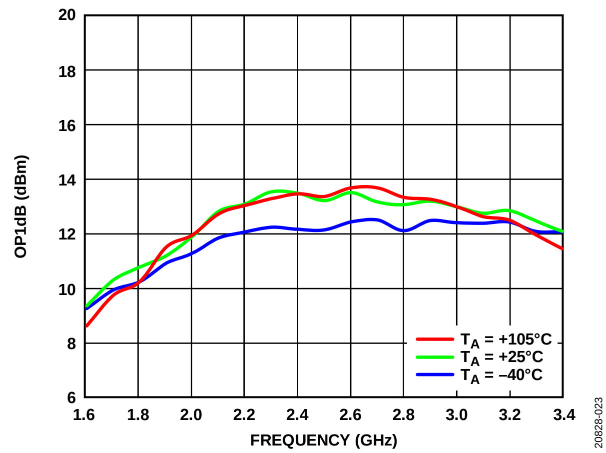

Figure 23. OP1dB vs. Frequency at Various Temperatures

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TRANSMIT OPERATION

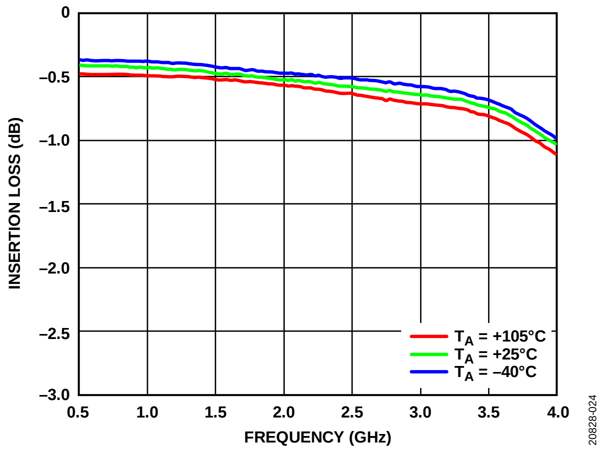

Figure 24. Insertion Loss vs. Frequency at Various Temperatures

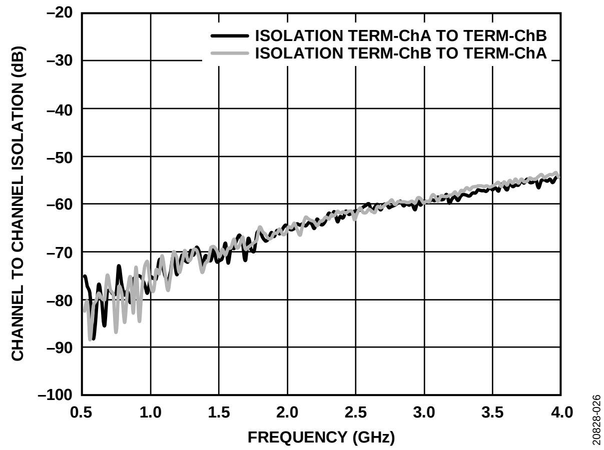

Figure 26. Channel to Channel Isolation vs. Frequency

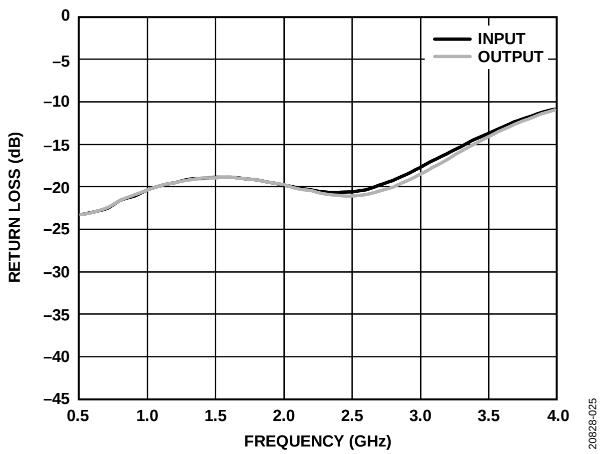

Figure 25. Return Loss vs. Frequency

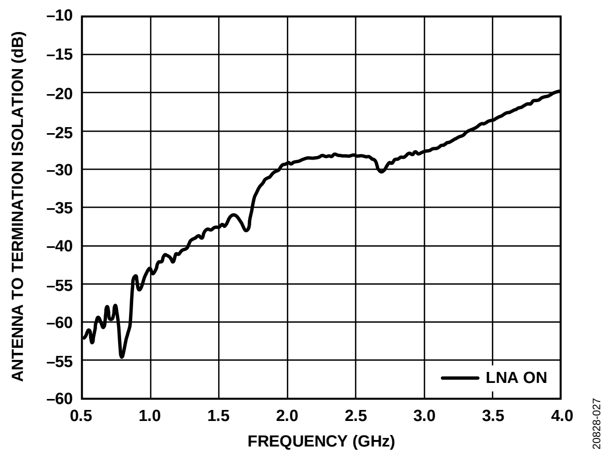

Figure 27. Antenna to Termination Isolation vs. Frequency, LNA On

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THEORY OF OPERATION

The ADRF5549 requires a positive supply voltage applied to VDD1-ChA, VDD2-ChA, VDD1-ChB, VDD2-ChB, and SWVDD-ChAB. Use bypassing capacitors on the supply lines to filter noise and use 300 Ω series resistors on the BP-Chx and PD-ChAB digital control pins for glitch and overcurrent protection.

SIGNAL PATH SELECT

When SWCTRL-ChAB is set to high, the ADRF5549 supports transmit operations. During this operation, when applying an RF input to ANT-ChA and ANT-ChB, the signal paths connect from ANT-ChA to TERM-ChA and from ANT-ChB to TERM-ChB.

When SWCTRL-ChAB is set to low, the ADRF5549 supports receive operations. During this operation, applying an RF input at ANT-ChA and ANT-ChB connects ANT-ChA to RxOUT-ChA and ANT-ChB to RxOUT-ChB.

Receive Operation

The ADRF5549 supports high gain mode, low gain mode, power-down high isolation mode, and power-down low isolation mode during receive operations (see Table 6).

When PD-ChAB is set to low, the LNA powers up and the user can select high gain mode or low gain mode. To select high gain mode, set BP-ChA or BP-ChB to low. To select low gain mode, set BP-ChA or BP-ChB to high.

When PD-ChAB is set to high, the ADRF5549 enters power-down mode. To select power-down high isolation mode, set BP-ChA or BP-ChB to low. To select power-down low isolation mode, set BP-ChA or BP-ChB to high.

BIASING SEQUENCE

To power-up the ADRF5549, perform the following steps:

1. Connect GND to ground.
2. Power up VDD1-ChA, VDD2-ChA, VDD1-ChB, VDD2-ChB, and SWVDD-ChAB.
3. Power up SWCTRL-ChAB.
4. Power up PD-ChAB.
5. Power up BP-ChA and BP-ChB.
6. Apply an RF input signal to ANT-ChA and ANT-ChB.

To power-down the device, perform these steps in the reverse order.

Table 5. Truth Table: Signal Path

	Signal Path Select[1]	
SWCTRL-ChAB	**Transmit Operation**	**Receive Operation**
Low	Off	On
High	On	Off

[1] See the signal path descriptions in Table 6.

Table 6. Truth Table: Receive Operation, SWCTRL-CHAB=Low

Operation and Mode	PD-ChAB	BP-ChA or BP-ChB	Signal Path
Receive Operation			ANT-ChA to RxOUT-ChA or ANT-ChB to RxOUT-ChB
High Gain Mode	Low	Low	
Low Gain Mode	Low	High	
Power-Down High Isolation Mode	High	Low	
Power-Down Low Isolation Mode	High	High	

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APPLICATIONS INFORMATION

To generate the evaluation PCB used in the typical application circuit shown in Figure 28, use proper RF circuit design techniques. Signal lines at the RF port must have a 50 Ω impedance, and the package ground leads and the backside ground slug must connect directly to the ground plane. Use 300 Ω series resistors on the BP-Chx and PD-ChAB digital control pins for glitch and overcurrent protection.

See the ADRF5549-EVALZ user guide for additional information on the evaluation board.

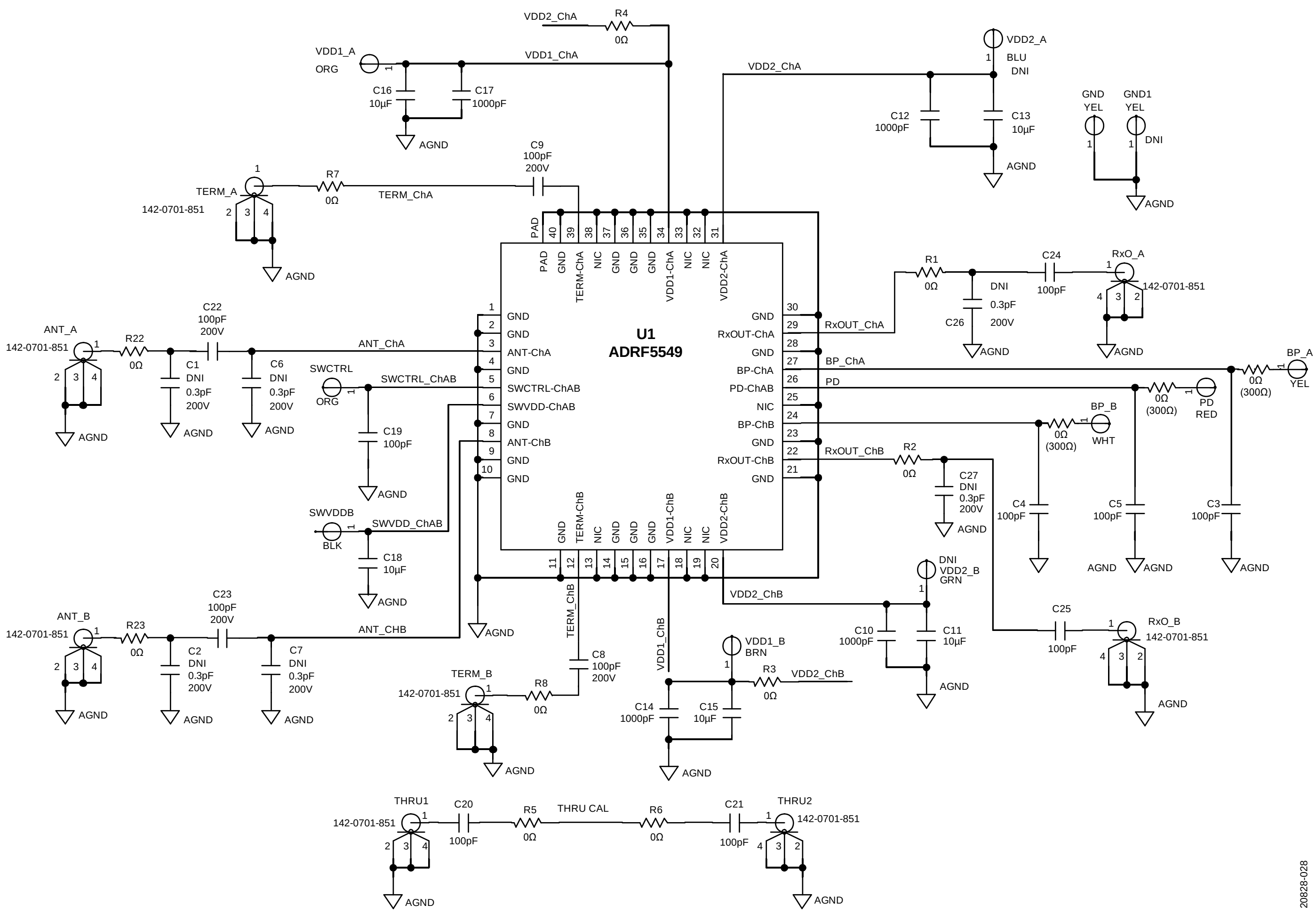

Figure 28. Typical Application Circuit

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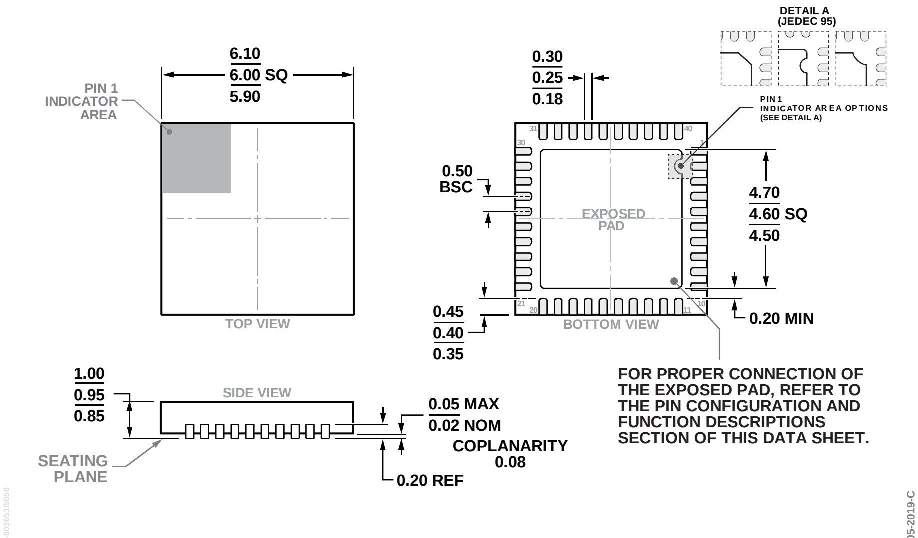
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-5

Figure 29. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.95 mm Package Height
(CP-40-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF5549BCPZN	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15
ADRF5549BCPZN-R7	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15
ADRF5549BCPZN-RL	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15
ADRF5549-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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