EVAL-ADG5421FEBZ Evaluation Board User Guide

UG-1887

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Evaluating the ADG5421F ±60 V Fault Protection and Detection, 11 Ω R_{ON}, Dual SPST Switch

FEATURES

- Supply voltages
  - Dual supply: ±5 V to ±22 V
  - Single supply: 8 V to 44 V
- Protected against overvoltage on the source pins
  - Signal voltages up to −60 V and +60 V
- LED for visual overvoltage indication
- Parallel interface compatible with 1.8 V logic

EVALUATION KIT CONTENTS

- EVAL-ADG5421FEBZ evaluation board

DOCUMENTS NEEDED

- ADG5421F data sheet
- EVAL-ADG5421FEBZ user guide

EQUIPMENT NEEDED

- DC voltage source
  - ±5 V to ±22 V for dual supply
  - 8 V to 44 V for single supply
- Optional digital voltage source: 5 V
- Analog signal source
- Method to measure voltage, such as a digital multimeter (DMM)

GENERAL DESCRIPTION

The EVAL-ADG5421FEBZ is the evaluation board for the ADG5421F, which features two SPST switch channels. The ADG5421F has overvoltage fault detection and protection circuitry on the source pins and is protected against signals up to −60 V and +60 V in both the powered and unpowered states.

Figure 1 shows the EVAL-ADG5421FEBZ in a typical evaluation setup. The ADG5421F is soldered to the center of the evaluation board, and 2-wire screw terminals are provided to connect to each of the source and drain pins. Three screw terminals are used to power the device, with a fourth terminal used to provide a user defined digital voltage to supply the LED, which is mounted to provide visual indication of the fault status of the switch.

For full details on the ADG5421F, see the ADG5421F data sheet, which must be consulted in conjunction with this user guide when using this evaluation board.

TYPICAL EVALUATION BOARD SETUP

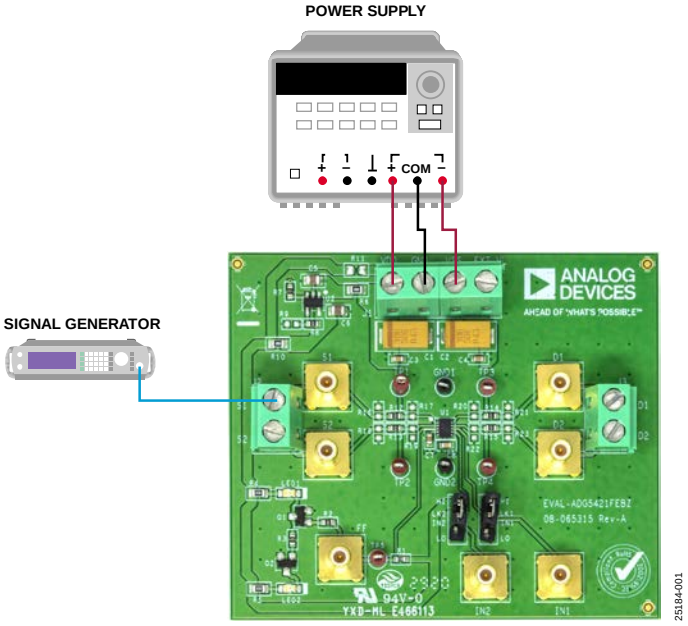

Figure 1. EVAL-ADG5421FEBZ (on Right), Power Supply, and Signal Generator

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REVISION HISTORY

10/2020—Revision 0: Initial Version

GETTING STARTED

EVALUATION BOARD SETUP PROCEDURE

The EVAL-ADG5421FEBZ operates independently and does not require any additional evaluation boards or software to operate. An on-board ADP7142 low dropout (LDO) linear regulator is provided as the digital power supply for the light emitting diodes (LEDs) and to manually control the ADG5421F.

The J1 connector supplies the EVAL-ADG5421FEBZ with a dual power supply of ±5 V to ±22 V or a single supply of +8 V to +44 V. For single supply, connect the EVAL-ADG5421FEBZ VSS pin and GND pin together on J1. If the VDD pin voltage is greater than 40 V, remove the R6 resistor to protect the on-board ADP7142 LDO linear regulator and move the R10 resistor to the R11 pad (where the R11 resistor can be populated, if required) to use an alternative digital voltage supply connected to the EXT_VL pin on J1.

To set up the EVAL-ADG5421FEBZ to perform a functionality test, take the following steps:

1. Connect a power supply to the J1 connector. If a single supply is required, connect the EVAL-ADG5421FEBZ VSS pin and GND pin together on J1.
2. Control the digital signals for the switch channel on the ADG5421F by using the LK1 and LK2 switches.
   a. In Position LO, the switches are open and present as an open-circuit.
   b. In Position HI, the switches are closed and present with a resistance of approximately 11 Ω.
3. The green LED lights up to indicate that the switch is operating normally.

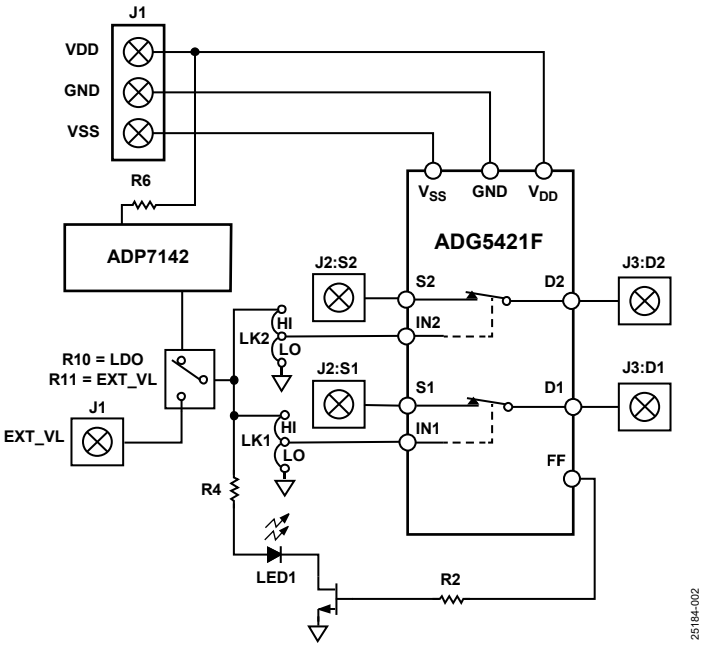

Figure 2. EVAL-ADG5421FEBZ Block Diagram

EVALUATION BOARD HARDWARE

Use the EVAL-ADG5421FEBZ to evaluate the operation of the ADG5421F. Figure 1 shows a typical evaluation setup where only a power supply and signal generator are required. Figure 2 shows the block diagram of the main components of the evaluation board.

By using the EVAL-ADG5421FEBZ, the ADG5421F can pass signals from either the source or drain connectors. The source pins have fault detection circuitry that reacts to an overvoltage event. During an overvoltage event, the switches turn off, and the FF pin pulls low. See the ADG5421F data sheet for more details.

POWER SUPPLY

Connector J1 provides access to the supply pins of the ADG5421F. VDD, GND, and VSS link to the appropriate pins on the ADG5421F. For dual-supply voltages, the EVAL-ADG5421FEBZ can be powered from ±5 V to ±22 V. For single-supply voltages, the GND and VSS terminals must be connected together, and the EVAL-ADG5421FEBZ can be powered from 8 V to 44 V. The on-board ADP7142 LDO linear regulator is provided for the digital control voltage. A secondary voltage source can be connected to the EXT_VL terminal of the EVAL-ADG5421FEBZ and used as the digital control voltage. To use the EXT_VL terminal of the EVAL-ADG5421FEBZ, move the R10 resistor to the R11 pad. Do not expose the on-board ADP7142 LDO linear regulator to voltages greater than 40 V. Remove the R6 resistor and supply an alternative digital voltage via the EXT_VL terminal of the EVAL-ADG5421FEBZ, if required.

INPUT SIGNALS

Two 2-pin screw connectors (J2 and J3) are provided to connect to both the source and drain pins of the ADG5421F. Additional Subminiature Version B (SMB) connectors are available if extra connections are required. The ADG5421F is overvoltage protected on the source side, and each source terminal (S1 and S2) can be presented with a voltage of up to +60 V or −60 V. See the ADG5421F data sheet for more details.

Each trace on the source and drain side includes two sets of 0603 pads, which can be used to place a load on the signal path to ground. A 0 Ω resistor is placed in the signal path and can be replaced with a user defined value. The resistor combined with the gold pin connectors can be used to create a simple RC filter.

The ADG5421F uses a parallel interface to control the operation of the switch channel. The switch operation can be manually controlled using the headers on LK1 and LK2, or an external controller can be interfaced directly to the control pins by using the SMB connectors (IN1 and IN2) and removing the link headers on LK1 and LK2.

OUTPUT SIGNALS

The FF pin is an open-drain output that indicates when the device is operating normally or whether there is an overvoltage fault on one of the source pins. For visual indication, LEDs are mounted on the EVAL-ADG5421FEBZ. When the device operates normally, the FF pin remains high (with a pull-up resistor required), and LED1 illuminates green. If an overvoltage occurs at any of the source pins, the FF pin pulls low, and LED2 illuminates red.

JUMPER SETTINGS

LINK HEADERS AND 0 Ω RESISTORS

The on-board link headers (LK1 to LK2) can control the ADG5421F manually. On-board 0 Ω, 300 Ω, and 1 kΩ resistors configure the digital control voltage and isolate the LEDs from the rest of the system. Table 1 lists the link headers and resistors and explains how each is used on the EVAL-ADG5421FEBZ.

The LK1 and LK2 link headers control the ADG5421F switch channels. Place the link header in Position LO to open the switch and place the link header in Position HI to close the switch.

The R6 resistor connects the VIN pin of the on-board ADP7142 LDO linear regulator to the VDD terminal supply of the EVAL-ADG5421FEBZ. Remove the R6 resistor to protect the LDO linear regulator from voltages higher than 40 V. Move the 0 Ω R10 resistor to the R11 pad to use an alternative digital voltage connected to the EXT_VL terminal of the EVAL-ADG5421FEBZ.

The R2 and R3 resistors connect the FF pin of the ADG5421F to the LED controls, and the R4 and R5 resistors connect the LEDs to the digital power supply node, VL

Table 1. Link Headers and Resistors Descriptions

Label	Position	Description
LK1	LO	S1/D1 switch open
	HI	S1/D1 switch closed
LK2	LO	S2/D2 switch open
	HI	S2/D2 switch closed
R1	Inserted	1 kΩ pull-up resistor at the FF pin
	Removed	No external pull-up resistor at the FF pin
R2, R3	Inserted	FF pin connected to LED1 and LED2
	Removed	FF pin disconnected from LED1 and LED2
R4, R5	Inserted	LED1 and LED2 connected to the VL node
	Removed	LED1 and LED2 disconnected from VL node
R6	Inserted	LDO regulator powered up
	Removed	LDO regulator unpowered
R10	Inserted	On-board LDO regulator digital voltage
R11	Inserted	EXT_VL digital voltage

SMB CONNECTORS

The parallel interface of the ADG5421F can either be controlled manually using the LK1 and LK2 link headers or accessed by using the IN1 and IN2 SMB connectors. To use the SMB connectors, remove the LK1 and LK2 link headers. To access the ADG5421F FF digital output, use the FF SMB connector.

EVALUATION BOARD SCHEMATICS AND ARTWORK

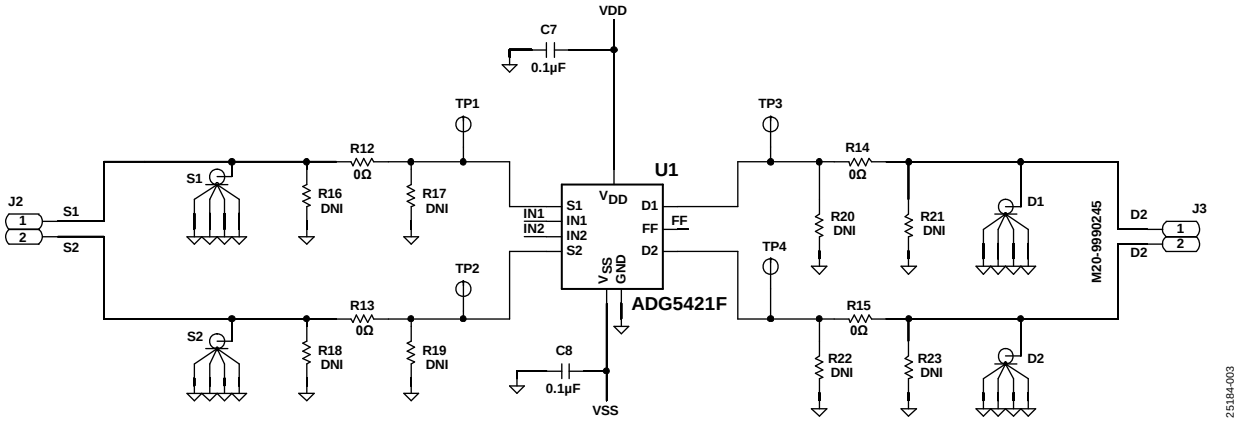

Figure 3. EVAL-ADG5421FEBZ Evaluation Board Schematic—Page 1

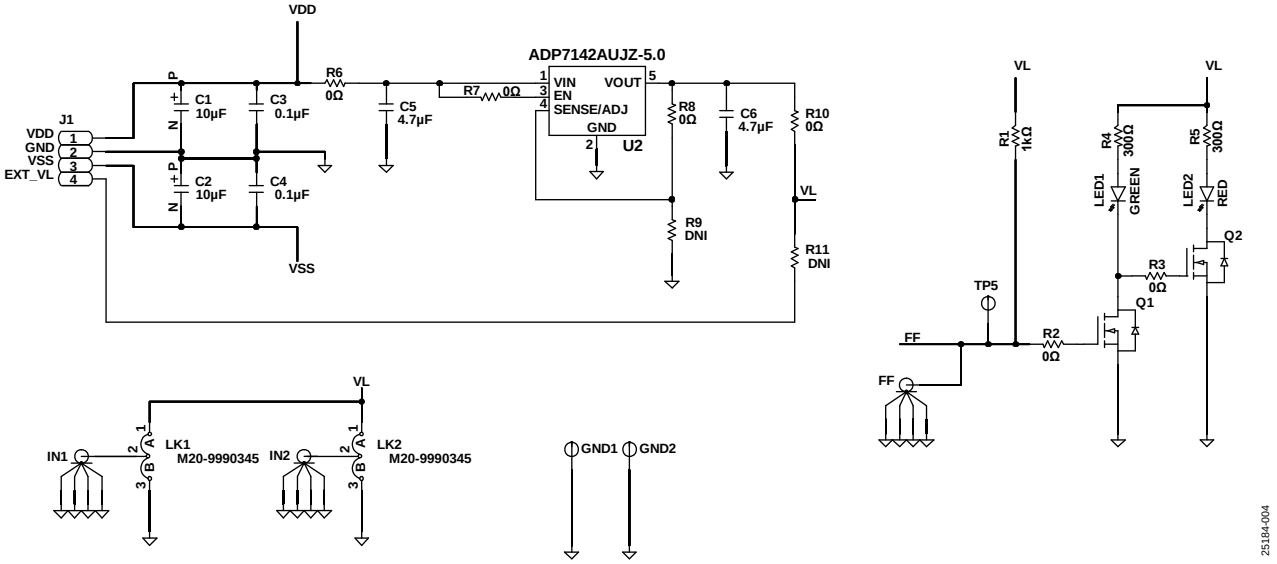

Figure 4. EVAL-ADG5421FEBZ Evaluation Board Schematic—Page 1

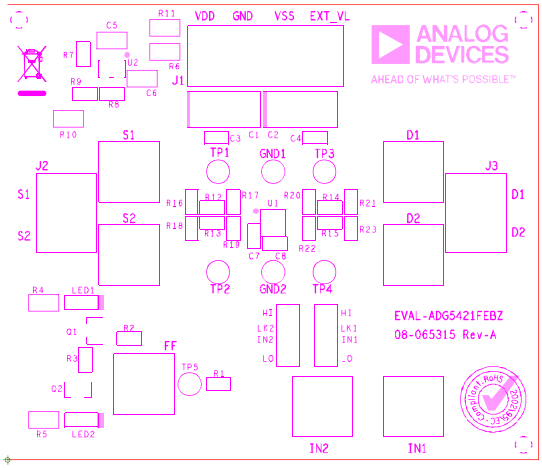

Figure 5. EVAL-ADG5421FEBZ Silkscreen

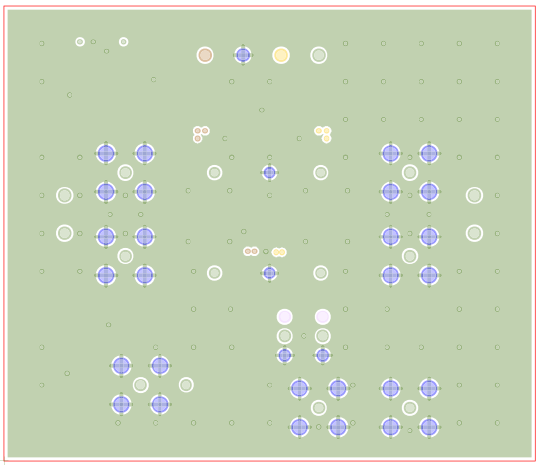

Figure 8. EVAL-ADG5421FEBZ Layer 3

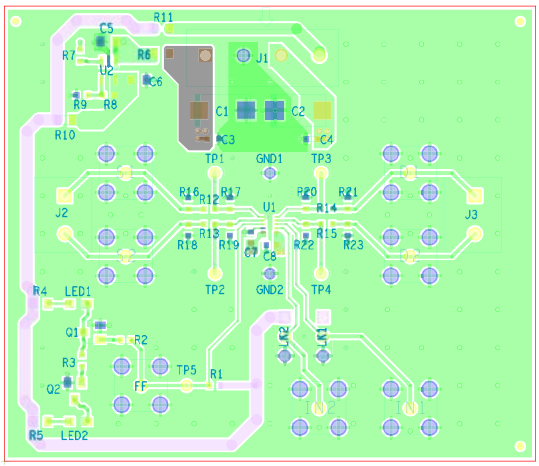

Figure 6. EVAL-ADG5421FEBZ Top Layer

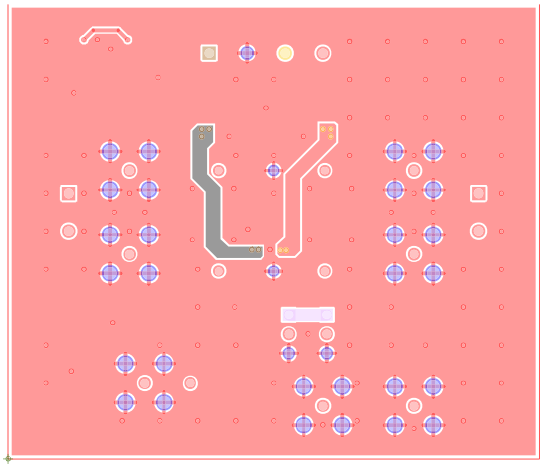

Figure 9. EVAL-ADG5421FEBZ Bottom Layer

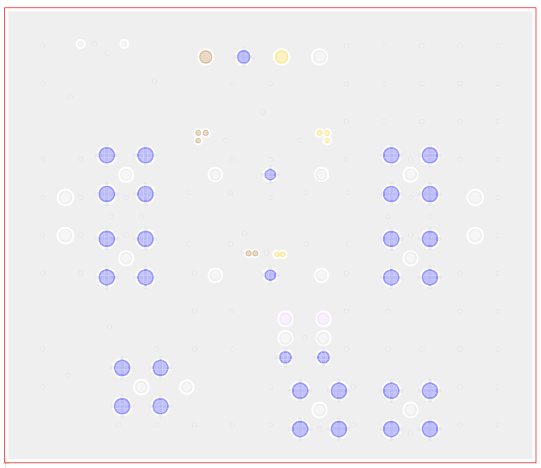

Figure 7. EVAL-ADG5421FEBZ Layer 2

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Reference Designator	Description	Manufacturer	Part Number
C1, C2	10 µF tantalum capacitors, 50 V, Size D	AVX	TAJD106K050RNJ
C3, C4, C7, C8	0.1 µF, multilayer, ceramic capacitors, 50 V	Murata	GRM188R71H104KA93D
C5, C6	4.7 µF, multilayer, ceramic capacitors	TDK	C2012X5R1H475K125AB
D1, D2, FF, IN1, IN2, S1, S2	50 Ω, SMB sockets	Amphenol	SMB1251B1-3GT30G-50
GND1, GND2	Test points, black	Vero Technologies	20-2137
J1	4-pin terminal block, 5 mm pitch	Camdenboss LTD	CTB5000/4
J2, J3	2-pin terminal blocks, 5 mm pitch	Camdenboss LTD	CTB5000/2
LED1	LED, surface-mount diode (SMD), green	Kingbright	KP-2012SGC
LED2	LED, SMD, red	Kingbright	KP-2012EC
LK1, LK2	3-pin headers and shorting links	Harwin	M20-9990345
Q1, Q2	Transistors, N-channel enhancement mode field effect transistor (MOSFET), 60 V, 0.23 A, SOT-23	ONSEMI	NDS7002A
R1	Resistor, 1 kΩ, 0.063 W	Multicomp (SPC)	MC0063W060311K
R6, R10	0 Ω resistors	Panasonic	ERJ-6GEY0R00V
R2, R3, R7, R8, R12 to R15	0 Ω resistors	Multicomp (SPC)	MC0603WG00000T5E-TC
R4, R5	Resistors, 300 Ω, 0.1 W	Yageo	RC0805JR-07300RL
TP1 to TP5	Test points, red	Vero Technologies	20-313137
U1	±60 V fault protection and detection, 11 Ω R_{ON}, dual SPST switch	Analog Devices, Inc.	ADG5421F
U2	40 V, 200 mA, low noise, CMOS LDO linear regulator	Analog Devices	ADP7142AUJZ-5.0