



AD5162 FMC-SDP Interposer & Evaluation Board / Xilinx KC705 Reference Design

Supported Devices

- [AD5162](#)

Evaluation Boards

- [EVAL-AD5162SDZ](#)

Overview

This document presents the steps to setup an environment for using the [EVAL-AD5162SDZ](#) evaluation board together with the Xilinx KC705 FPGA board and the Xilinx Embedded Development Kit (EDK). Below is presented a picture of the EVAL-AD5162SDZ Evaluation Board with the Xilinx KC705 board.



For component evaluation and performance purposes, as opposed to quick prototyping, the user is directed to use the part evaluation setup. This consists of:

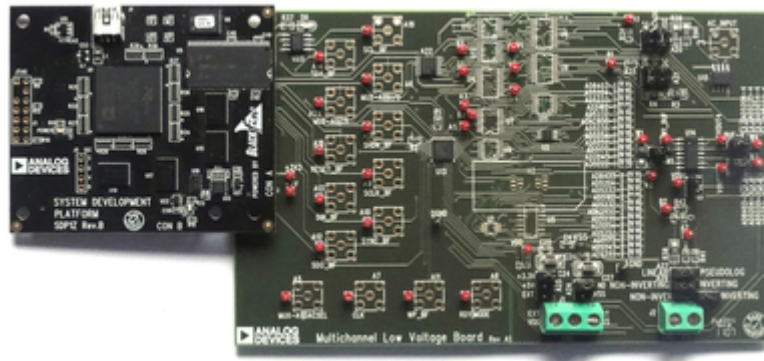
- 1. A controller board like the SDP-B (EVAL-SDP-CS1Z)
- 2. The component SDP compatible product evaluation board
- 3. Corresponding PC software (shipped with the product evaluation board)

The SDP-B controller board is part of Analog Devices System Demonstration Platform (SDP). It provides a high speed USB 2.0 connection from the PC to the component evaluation board. The PC runs the evaluation software. Each evaluation board, which is an SDP compatible daughter board, includes the necessary installation file required for performance testing.

Note: it is expected that the analog performance on the two platforms may differ.

28 Sep 2012 09:32 · [Adrian Costina](#)

Below is presented a picture of **SDP-B** Controller Board with the **EVAL-AD5162SDZ** Evaluation Board.



The EVAL-AD5162SDZ evaluation board is a member of a growing number of boards available for the SDP. Designed to help customers evaluate performance or quickly prototype new AD5162 circuits and reduce design time, the EVAL-AD5162SDZ evaluation board can operate in single-supply and incorporates an internal power supply powered from the USB.

The AD5162 provides a compact 3 mm x 4.9 mm packaged solution for dual 256 position adjustment applications. This device performs the same electronic adjustment function as a 3-terminal mechanical potentiometer. Available in four different end-to-end resistance values (2.5 k, 10 k, 50 k, 100 k), this low temperature coefficient device is ideal for high accuracy and stability-variable resistance adjustments. The wiper settings are controllable through the SPI compatible digital interface. The resistance between the wiper and either end point of the fixed resistor varies linearly with respect to the digital code transferred into the RDAC latch. Operating from a 2.7 V to 5.5 V power supply and consuming less than 6 μ A allows the AD5162 to be used in portable battery-operated applications.

More information

- [AD5162 Product Info](#) - pricing, samples, datasheet
- [EVAL-AD5162SDZ evaluation board user guide](#)
- [Xilinx KC705 FPGA board](#)

Getting Started

The first objective is to ensure that you have all of the items needed and to install the software tools so that you are ready to create and run the evaluation project.

Required Hardware

- [Xilinx KC705 FPGA board](#)
- FMC-SDP adapter board

- **EVAL-AD5162** evaluation board

Required Software

- Xilinx ISE 14.6.
- UART Terminal (Termite/Tera Term/Hyperterminal), baud rate 115200.

Downloads



- **AD5162 Driver:**
https://github.com/analogdevicesinc/no-OS/tree/master/device_drivers/AD5172
- **AD5162 Commands:**
https://github.com/analogdevicesinc/no-OS/tree/master/device_commands/AD5172
- **Xilinx Boards Common Drivers:**
https://github.com/analogdevicesinc/no-OS/tree/master/platform_drivers/Xilinx/SDP_Common
- **EDK KC705 Reference project:**
https://github.com/analogdevicesinc/fpga_hdl_xilinx/tree/master/cf_sdp_kc705

Hardware setup



Before connecting the ADI evaluation board to the Xilinx KC705 make sure that the VADJ_FPGA voltage of the KC705 is set to 3.3V. For more details on how to change the setting for VADJ_FPGA visit the Xilinx KC705 product page.

- Use the FMC-SDP interposer to connect the ADI evaluation board to the Xilinx KC705 board on the FMC LPC connector.
- Connect the JTAG and UART cables to the KC705 and power up the FPGA board.

Reference Project Overview

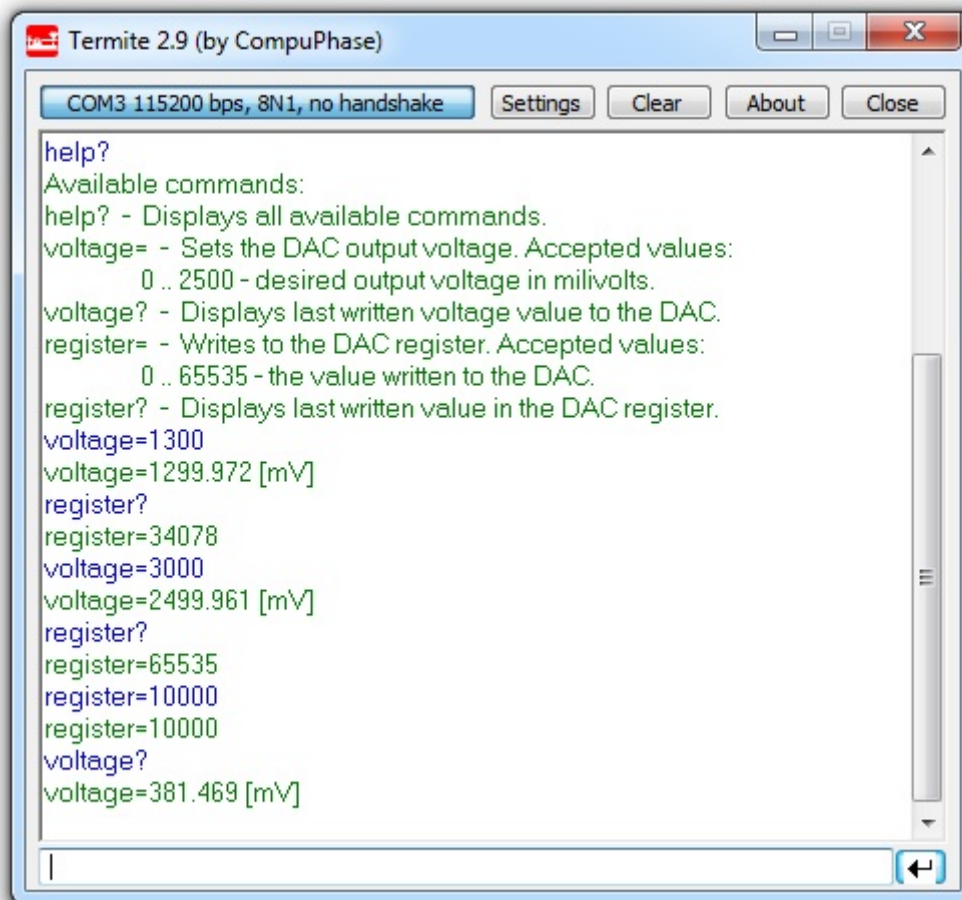


The following commands were implemented in this version of EVAL-AD5162 reference project for Xilinx KC705 FPGA board.

Command	Description
help?	Displays all available commands.
rdac=	Load the wiper register with a give value. Accepted values: channel: 0 - select RDAC 1 wiper register. 1 - select RDAC 2 wiper register. value: 0 .. 255 - value to be written in register.
rdac?	Read back the value of the wiper register. Accepted values: channel: 0 - select RDAC 1 wiper register. 1 - select RDAC 2 wiper register.
wbuf1?	Read back the value of the Wiper Buffer in voltage. (VDD=3.2V)
shutdown=	Shutdown connects wiper to B terminal and open circuits the A terminal. This command is not supported by this device.
shutdown?	Notify about the state of the selected RDAC. This command is not supported by this device.

Commands can be executed using a serial terminal connected to the UART peripheral of Xilinx KC705 FPGA.

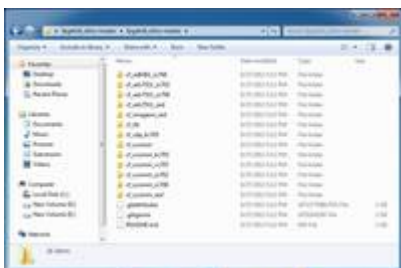
The following image shows a generic list of commands in a serial terminal connected to Xilinx KC705 FPGA's UART peripheral.



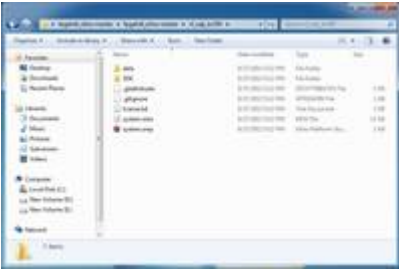
Software Project Setup

The hardware platform for each reference projects with FMC-SDP interposer and KC705 evaluation board is common. The next steps should be followed to recreate the software project of the reference design:

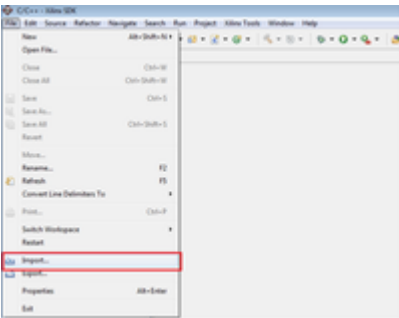
- First download the **KC705 Reference project** from Github on your computer. You can do this by cloning this repository: https://github.com/analogdevicesinc/fpga_hdl_xilinx.



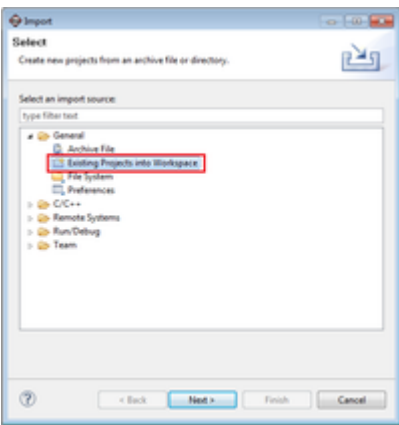
- From this entire repository you will use **cf_sdpsdp_kc705** folder. This is common for all KC705 projects.



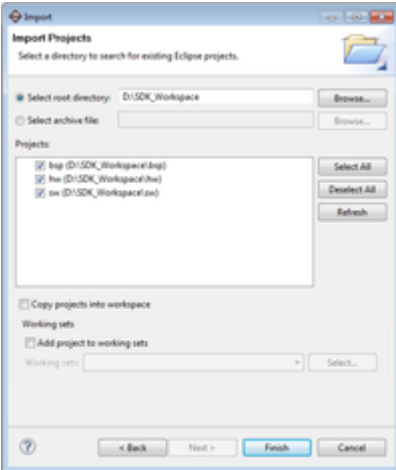
- Open the Xilinx SDK. When the SDK starts, it asks you to provide a folder where to store the workspace. Any folder can be provided. Make sure that the path where it is located does not contain any spaces.
- In the SDK select the **File→Import** menu option to import the software projects into the workspace.



- In the *Import* window select the **General→Existing Projects into Workspace** option.



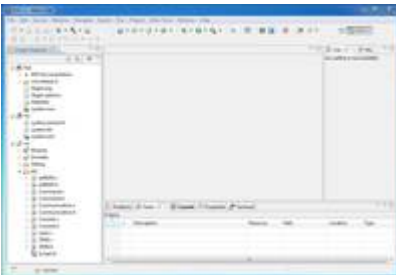
- In the *Import Projects* window select the **cf_sdp_kc705** folder as root directory and check the **Copy projects into workspace** option. After the root directory is chosen the projects that reside in that directory will appear in the *Projects* list. Press *Finish* to finalize the import process.



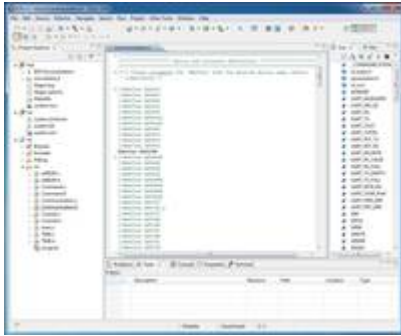
- The *Project Explorer* window now shows the projects that exist in the workspace without software files.



- Now the software must be added in your project. For downloading the software, you must use 3 links from Github given in **Downloads** section. From there you'll download the specific driver, the specific commands and the Xilinx Boards Common Drivers(which are commons for all Xilinx boards). All the software files downloaded must be copied in **src** folder from **sw** folder.



- Before compilation in the file called **Communication.h** you have to uncomment the name of the device that you currently use. In the picture below there is an example of this, which works only with AD5629R project. For another device, uncomment only the respective name. You can have one driver working on multiple devices, so the drivers's name and the uncommented name may not be the same for every project.



- The SDK should automatically build the project and the *Console* window will display the result of the build. If the build is not done automatically, select the **Project→Build Automatically** menu option.
- If the project was built without any errors, you can program the FPGA and run the software application.

13 Aug 2013 08:22 · [Lucian Sin](#)

More information

- [ask questions about the FPGA reference design](#)
- Example questions:
 - [What's the width and depth of the FIFO in Fmcomms2 adc_dmac?](#) by l312361206
 - [Have you any JESD204B reference design that has not microblaze and MIG7 Axi_ddr_cntrl?](#) by [saban](#)
 - [FMCOMMS3 and ethernet data extraction](#) by [Cman](#)
 - [AD-FMCDAQ2 AD9680-1000 Noise Floor](#) by [Ed_V](#)
 - [FMCOMMS1 AD9548 clock derivation explanation](#) by [cherif.chibane@ll.mit.edu](#)

28 May 2012 14:18

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