

## SMPTE-259M/DVB-ASI Descrambler/Framer-Controller

### Features

- Fully compatible with SMPTE-259M
- Fully compatible with DVB-ASI
- Operates from a single +5V supply
- 100-pin TQFP package
- Decodes 10-bit parallel digital streams for 27M characters/sec (270 Mbits/sec serial)
- Operates with CY7B9334 SMPTE HOTLink® deserializer/receiver
- $X^9 + X^4 + 1$  descrambler and NRZI-to-NRZ decoder may be bypassed for raw data output

### Functional Description

#### SMPTE-259M Operation

The CY7C9335A is a CMOS integrated circuit designed to decode SMPTE-125M bit-parallel digital characters (or other data formats) using the SMPTE-259M decoding rules. Following decoding, the characters are framed by locating the 30-bit TRS pattern in the parallel character stream. The framed characters are then output.

The inputs of the CY7C9335A are designed to be directly mated to a CY7B9334 HOTLink receiver, which converts the SMPTE-259M compatible high-speed serial data stream into 10-bit parallel characters.

This device performs both TRS (sync) detection and framing, data descrambling with the SMPTE-259M  $X^9 + X^4 + 1$  algorithm, and NRZI-to-NRZ decoding. These functions operate at a 27 MHz character rate. For those systems operating with non-SMPTE-259M compliant video streams (or for diagnostic purposes), the descrambler and NRZI decoding functions can be disabled.

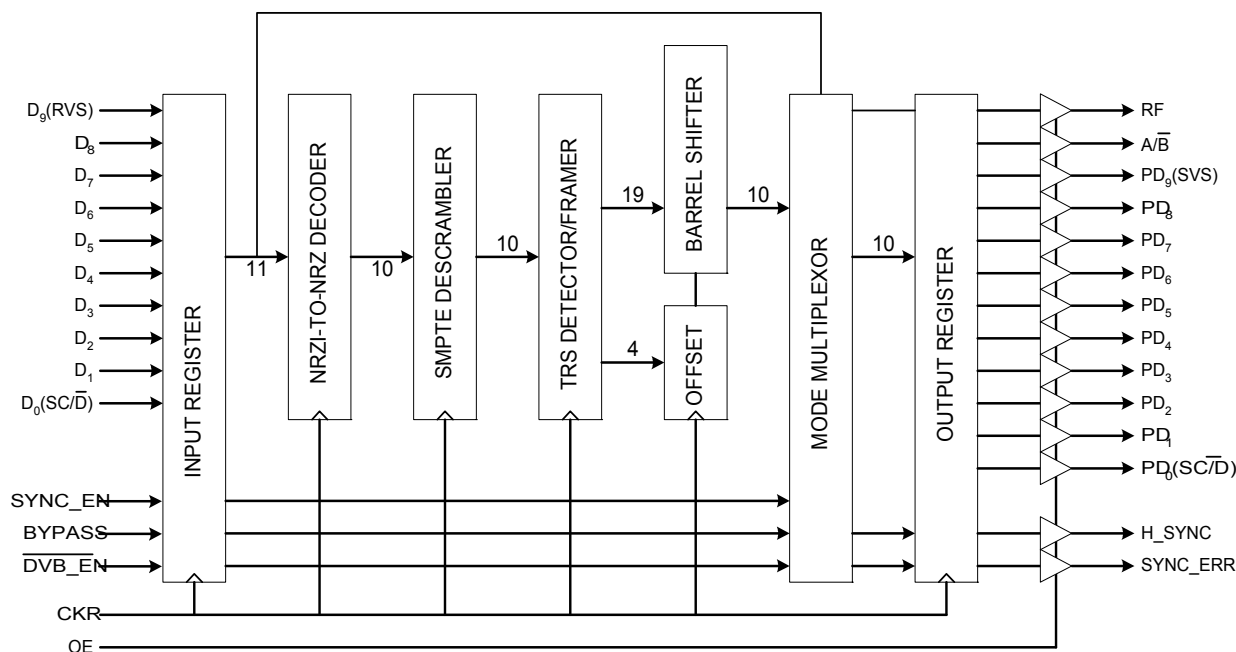
#### DVB-ASI Operation

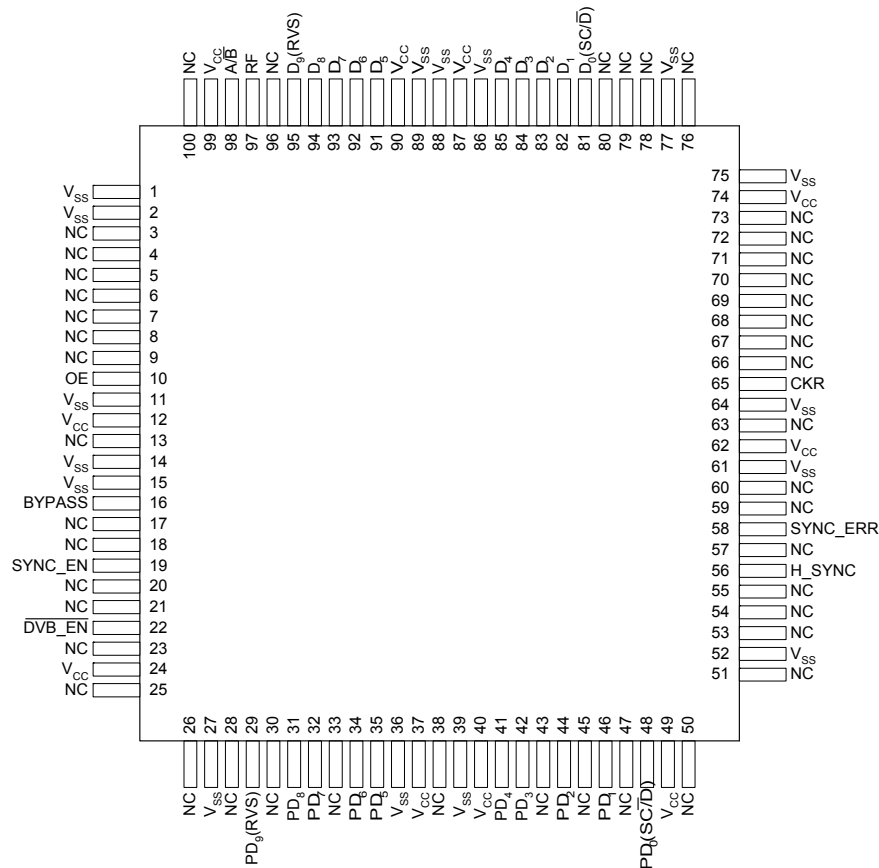
The CY7C9335A also contains the necessary multiplexers, control inputs and outputs, to control a DVB-ASI-compliant video stream. DVB-ASI operation is enabled through activation of a single input signal. This allows a single serial-to-parallel input port to support both SMPTE and DVB data streams under software or hardware control.

In DVB-ASI mode the CY7C9335A automatically enables both the 8B/10B decoder and multibyte framer present in the CY7B9334 receiver/deserializer. All error detection, fill, and command codes are detected and output by the CY7C9335A.

The CY7C9335A operates from a single +5V supply. It is available in a 100-pin TQFP space saving package.

### Logic Block Diagram





Name	I/O	Description
BYPASS	Input	<b>Bypass SMPTE decoding.</b> BYPASS is ignored if $\overline{\text{DVB\_EN}}$ is active (LOW). If BYPASS is HIGH at the rising edge of CKR (and $\overline{\text{DVB\_EN}}$ is HIGH), the data latched into the input register is routed around both the NRZI decoder and the SMPTE descrambler and presented to the output register. If BYPASS is LOW at the rising edge of the CKR clock (and $\overline{\text{DVB\_EN}}$ is HIGH), the data present in the input register is routed through the NRZI decoder and SMPTE scrambler.
RF	Output	<b>Reframe.</b> This output is the inverted DVB-EN signal.
A/B	Output	<b>CY7B9334 Port Select.</b> When in DVB-ASI mode, this output will alternately select either the $\text{INA}_{\pm}$ or $\text{INB}_{\pm}$ receiver port based on errors detected in the data stream. This allows CY7C9335A to operate with normal and inverted DVB-ASI data streams (as would be commonly found on DVB-ASI streams routed through SMPTE switches). This requires the CY7B9334 $\text{INA}_{\pm}$ and $\text{INB}_{\pm}$ inputs to be connected to the same signal, but with $\text{INB}_{\pm}$ connected to invert the signal.
H_SYNC	Output	<b>Horizontal Sync.</b> This output toggles once every time that the TRS field is recognized. It changes state one clock cycle prior to the first character of the TRS field (3FF in 10-bit hex) appearing at the $\text{PD}_{0-9}$ outputs. This output also toggles to indicate detection of a TRS sequence, even when the TRS characters are at a different offset from the present offset and SYNC_EN is active (HIGH). This toggling action is disabled when $\overline{\text{DVB\_EN}}$ is active (LOW).

**Pin Descriptions** CY7C9335A SMPTE-259M Decoder (continued)

Name	I/O	Description
SYNC_EN	Input	<b>Sync Filtering Enabled.</b> This input controls the operation of the SMPTE framer. When this signal is active (HIGH) and a TRS sequence is detected, if the 10-bit character boundary is different from the previously received TRS, the H_SYNC output is toggled, but the character offset is not updated. If the immediately following TRS also has a different offset, the H_SYNC output is again toggled and the character offset is updated to match that of the detected TRS sequence. When this signal is inactive (LOW), the framer will update the character offset and toggle H_SYNC on every detected TRS sequence.
SYNC_ERR	Output	<b>Sync Error.</b> This output pulses HIGH for one CKR clock period when a TRS sequence is detected that is offset from its previous 10-bit character offset. This pulse starts at the same time as the H_SYNC signal toggles, but only occurs when SYNC_EN is active (HIGH) and the character offset is not updated.
PD <sub>9</sub> (RVS)	Output	<b>Parallel Data 9 or Received Violation Symbol.</b> This is the MSB of the framed output data bus. It is latched in the output register at the rising edge of CKR. When DVB_EN is active (LOW), this output indicates that the character present on PD <sub>8-0</sub> identifies the type of error detected in the character stream. When DVB_EN is disabled (HIGH), the character in the output register bits PD <sub>9-0</sub> is a descrambled and framed character of the SMPTE data stream.
PD <sub>8-1</sub>	Output	<b>Parallel Data 8 through 1.</b> The signals present at the PD <sub>8-1</sub> outputs are latched in the output register at the rising edge of CKR. When DVB_EN is disabled (HIGH), these signals are the middle eight bits of the descrambled and framed SMPTE 10-bit data character. When DVB_EN is active (LOW), these signals are full DVB-ASI data bus.
PD <sub>0</sub> (SC/D)	Output	<b>Parallel Data 0 or Special Code/Data Select.</b> This is the LSB of the output data field. It is latched in the output register at the rising edge of CKR. When DVB_EN is active (LOW), this output identifies that the character present in PD <sub>8-1</sub> is either a command (HIGH) or data (LOW) character. When DVB_EN is inactive (HIGH), this output data bit is the LSB of the descrambled and framed SMPTE data character.
D <sub>9</sub> (RVS)	Input	<b>Input Bit 9.</b> This is the MSB of the input register. It should be connected directly to the CY7B9334 deserializer output signal RVS(Q <sub>i</sub> ).
D <sub>8-1</sub>	Input	<b>Input Bits 8 through 1.</b> These signals should be connected directly to the CY7B9334 deserializer output signals Q <sub>7-0</sub> respectively.
D <sub>0</sub> (SC/D)	Input	<b>Input Bit 0.</b> This is the LSB of the input register. It should be connected directly to the CY7B9334 deserializer output signal SC/D(Q <sub>a</sub> ).
DVB_EN	Input	<b>DVB Mode Enable.</b> This signal is sampled by the rising edge of the CKR clock. If DVB_EN is active (LOW), the data present on the D <sub>0-9</sub> inputs are latched and routed to the PD <sub>0-9</sub> outputs.
CKR	Input	<b>Recovered Clock Read.</b> This clock controls all synchronous operations of the CY7C9335A. It operates at the character rate which is equivalent to one tenth the deserialized bit-rate. This clock is driven directly by the CKR output of the CY7B9334 deserializer.
OE	Input	<b>Output Enable.</b> When this signal is HIGH all outputs are driven to their normal logic levels. When LOW, all outputs are placed in a High-Z state.
V <sub>CC</sub>		<b>Power.</b>
V <sub>SS</sub>		<b>Ground.</b>

## CY7C9335A Description

### Input Register

The input register is clocked by the rising edge of CKR. This register captures the data present at the D<sub>0-9</sub> inputs on every clock cycle. In addition to the data inputs, all control inputs except OE are also captured at each rising edge of CKR. This includes BYPASS, DVB\_EN, and SYNC\_EN.

### NRZI-to-NRZ Decoder

The data in the input register is routed through an NRZI-to-NRZ decoder prior to being fed to the SMPTE descrambler. This removes the extra transitions added to the data stream by the NRZI encoder at the transmit end of the interface.

### SMPTE Descrambler

Once the data has been converted back to NRZ, it is then routed through a linear feed-forward descrambler. It decodes the data present in the NRZ decode register using the  $X^9 + X^4 + 1$  polynomial to remove the extra transitions added to the data stream at the transmit end of the interface.

### TRS Framer

The TRS Framer is used to detect all 30-bit TRS sequences (3FF, 000, 000 in 10-bit hex) in the character stream. Anytime this sequence is detected, the H\_SYNC output toggles.

This sequence is also used to frame the received characters so that the characters delivered to the output register are on their correct 10-bit boundaries. If SYNC\_EN is disabled (LOW) and the TRS sequence is detected in the decoded data stream, the character offset register is set to match the offset of the TRS sequence, and both the TRS sequence and the following characters are output on their proper 10-bit boundaries.

If SYNC\_EN is enabled, and a TRS sequence is detected whose character offset does not match that in the offset register, an internal flag is set but the offset register is not updated. On the next consecutive TRS sequence this flag is cleared and the offset register is updated.

### DVB-ASI Operation

The CY7C9335A is designed to operate in both SMPTE-259M and DVB-ASI environments. When operated in SMPTE-only environments, the DVB\_EN inputs must be tied to V<sub>CC</sub> or driven HIGH.

DVB-ASI operation is enabled by asserting DVB\_EN LOW. This signal is latched by the rising edge of the CKR clock. When the CY7C9335A is placed in DVB mode, the SMPTE and NRZI decoders are bypassed, and the data latched into the input register is routed directly to the output register.

### Error Detected

Errors detected in the DVB-ASI data stream are indicated by the Q<sub>9</sub> bit being HIGH. The specific type of error is identified by the remaining Q<sub>8-0</sub> bits in the output register.

### Command Code Reception

The DVB-ASI interface does not normally transmit any command characters other than the K28.5 code that is used both for synchronization and as a fill character when data is not being transmitted. These K28.5 characters are normally received as C5.0 characters. If other command characters are also transmitted, these characters are identified by Q<sub>0</sub> being HIGH, and by the bits present on Q<sub>8-1</sub>.

### DVB Invert Controller

DVB-ASI data streams are use 8B/10B encoded characters. If these characters are routed through SMPTE switches or repeaters, the signals may be inverted causing them to decode into incorrect or illegal characters. The CY7C9335A contains a state machine that, in conjunction with the CY7B9334 SMPTE HOTLink receiver, allows inverted DVB-ASI data streams to be decoded into their correct characters.

This state machine is only enabled when in DVB mode. It monitors the data stream for errors, and inverts the data stream at the CY7B9334 if it exceeds a preset statistical error rate. For this to operate the A/B output of the CY7C9335A needs to be connected to the A/B input of the CY7B9334 SMPTE HOTLink receiver (through the appropriate resistive divider).

If the CY7C9335A is not used for DVB-ASI operation, the A/B output may be left open.

## Maximum Ratings<sup>[1]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -40°C to +125°C

Supply Voltage to Ground Potential ..... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High-Z State ..... -0.5V to +7.0V

Output Current Into Outputs ..... 16 mA

DC Input Voltage ..... -0.5V to +7.0V

Static Discharge Voltage ..... > 2001 V  
(per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 5%

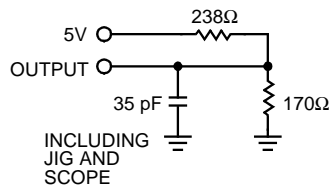
## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -3.2 mA, V <sub>CC</sub> = Min.	2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 16.0 mA, V <sub>CC</sub> = Min		0.5	V
V <sub>IH</sub>	Input HIGH Voltage	Note 2	2.0	7.0	V
V <sub>IL</sub>	Input LOW Voltage	Note 2	-0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	+10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-50	+50	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[3,4]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V	-30	-160	mA

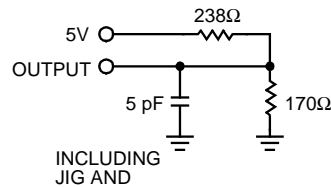
## Capacitance<sup>[4]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	f = 1 MHz, V <sub>CC</sub> = 5.0V	10	pF
C <sub>OUT</sub>	Output Capacitance		12	pF
C <sub>CLK</sub>	Clock Signal Capacitance		12	pF

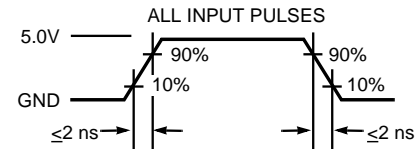
## AC Test Loads and Waveforms



(a)

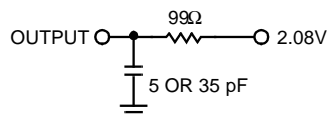


(b)



(c)

Equivalent to: THÉVENIN EQUIVALENT

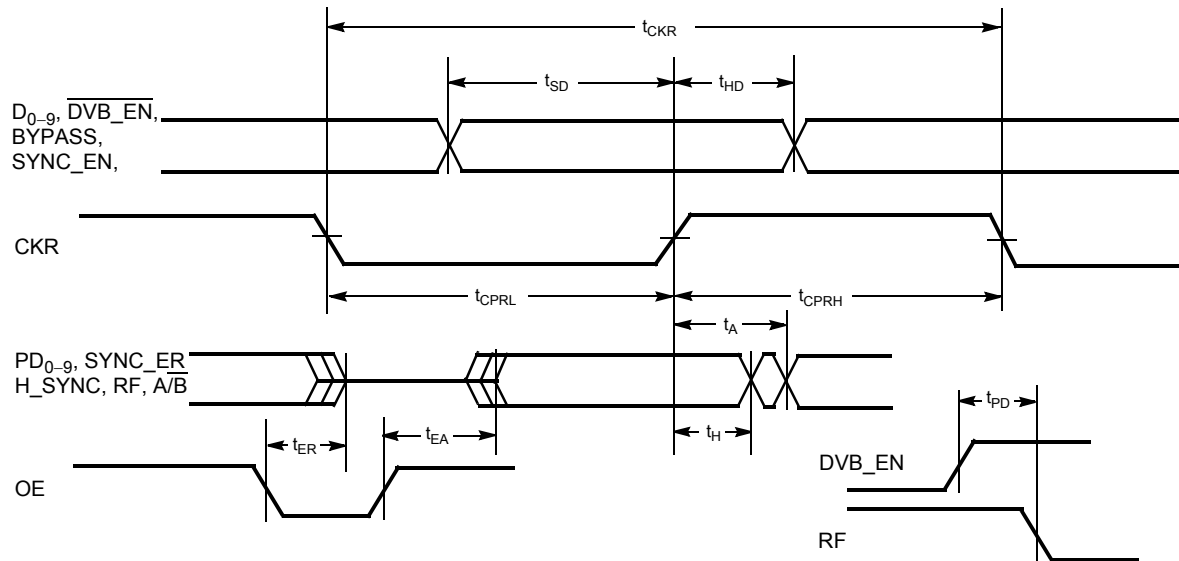


### Notes:

1. Single Power Supply: The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. These are absolute values with respect to device ground. All overshoots with respect to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V<sub>OUT</sub> = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Tested initially and after any design or process changes that may effect these parameters.

**Switching Characteristics Over the Operating Range** <sup>[5]</sup>

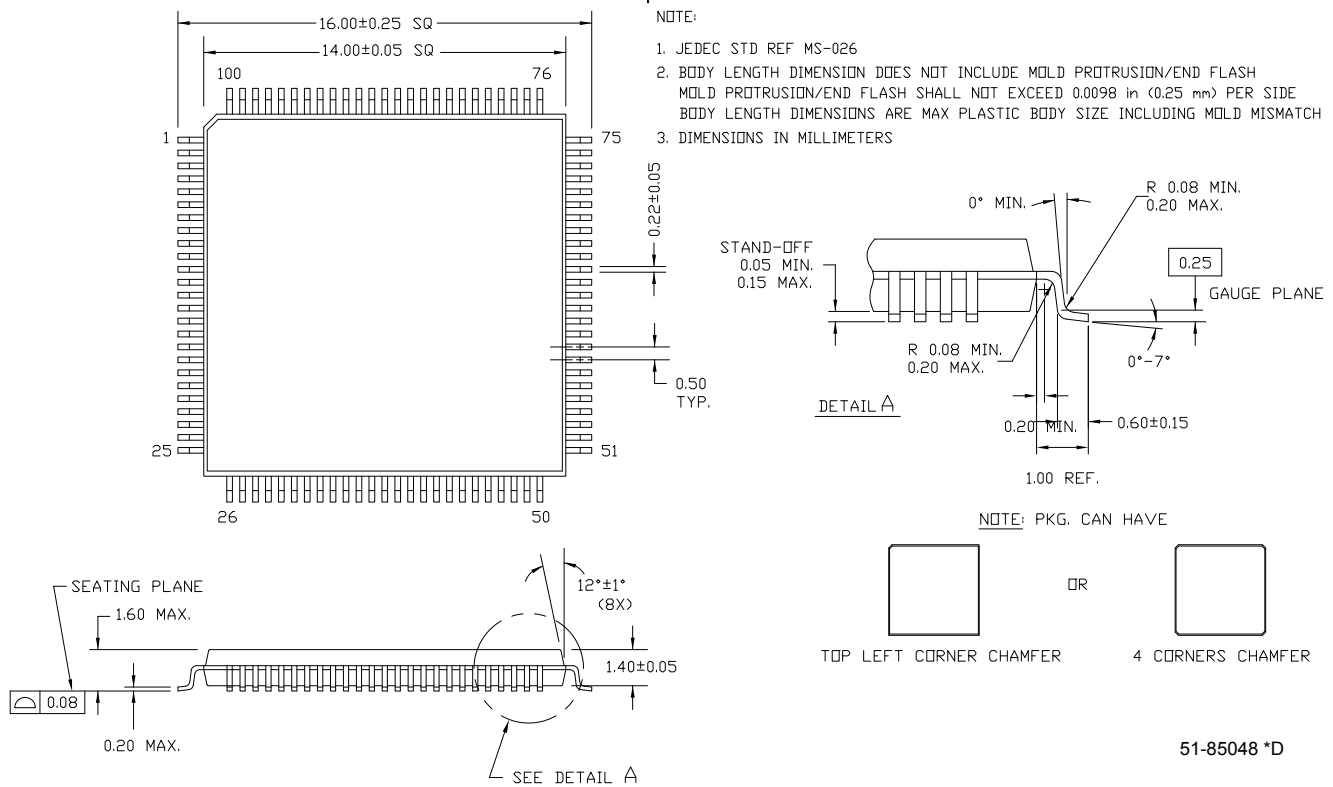
Parameter	Description	Min.	Max.	Unit
$t_{PD}$	Input to Output (DVB_EN to RF only)		20	ns
$t_{SD}$	Input Data Set-up Time to CKR	10		ns
$t_{HD}$	Input Data Hold Time to CKR	0		ns
$t_{CPRH}$	CKR Pulse Width HIGH	14.5		ns
$t_{CPRL}$	CKR Pulse Width LOW	14.5		ns
$t_{CKR}$	Read Clock Cycle <sup>[6]</sup>	30	62.5	ns
$t_A$	Output Access Time from CKR		10	ns
$t_H$	Output Hold Time from CKR	1		ns
$t_{EA}$	Input to Output Enable		24	ns
$t_{ER}$	Input to Output Disable <sup>[7]</sup>		24	ns

**Switching Waveform**

**Ordering Information**

Ordering Code	Package Name	Package Type	Operating Range
CY7C9335A-270AXC	A100	100-pin Thin Quad Flat Pack	Commercial
CY7C9335A-270AXCT	A100	100-pin Thin Quad Flat Pack (Tape and Reel)	

**Notes:**

5. All AC parameters are with all outputs switching.
6. The clock period may be extended by up to 90% for a single clock cycle when framing occurs in DVB-ASI mode.
7. Test load (b) used for this parameter. Test load (a) used for all other AC parameters.

**Package Diagram**
**Figure 1. 100-Pin TQFP (14X14X1.4 mm)**


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**Document History Page**

<b>Document Title: CY7C9335A SMPTE-259M/DVB-ASI Descrambler/Framer-Controller</b> <b>Document Number: 38-02083</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	129112	12/09/03	LAR	Pin-to-pin compatible with CY7C9335
*A	2896245	03/19/10	CGX	Updated Ordering information and package diagram.