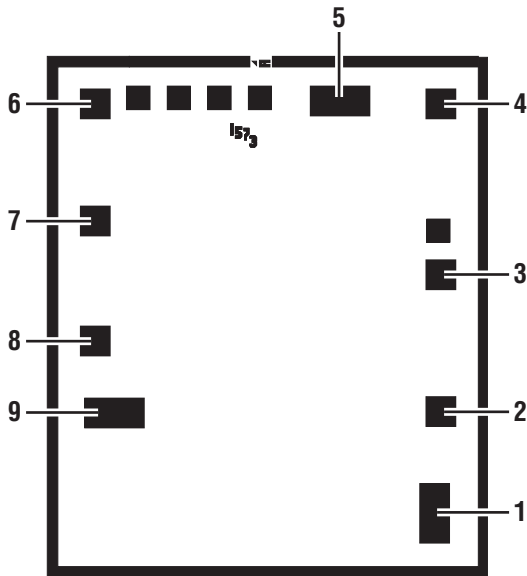


RH1573K
Low Dropout PNP
Regulator Driver

PAD FUNCTION

1. DRIVE
2. V_{IN}
3. V_{OUT}
4. COMP
5. GND1**
6. FB
7. LATCH
8. SHDN
9. GND2**

**GND1 and GND2 are connected together to form GND

DIE CROSS REFERENCE

LTC Finished Part Number	Order Part Number
RH1573K [†]	RH1573KDICE [†]
RH1573K [†]	RH1573KDWF ^{*†}


Please refer to LTC standard product data sheet for other applicable product information.

*DWF = DICE in wafer form.

61mils × 72mils,
12mils thick.

[†]Backside metal: Alloyed gold layer
(K designator)

Backside potential: lowest (GND) voltage

 LT, LTC and LTM are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

DICE/DWF ELECTRICAL TEST LIMITS $T_A = 25^\circ\text{C}$.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Reference Voltage	$I_{DRIVE} = 20\text{mA}$, $T_J = 25^\circ\text{C}$	1.252	1.278	V
Line Regulation (V_{FB})	$I_{DRIVE} = 20\text{mA}$, $3\text{V} < V_{IN} < 7\text{V}$		2	mV
Load Regulation (V_{FB})	$I_{DRIVE} = 20\text{mA}$ to 250mA		18	mV
FB Pin Bias Current	$V_{FB} = 1.265\text{V}$		4	μA
DRIVE Pin Current	$V_{FB} = 1.35\text{V}$, $V_{DRIVE} = 7\text{V}$ $V_{FB} = 1.15\text{V}$, $V_{DRIVE} = 1.5\text{V}$	290	1.2	mA mA
DRIVE Pin Saturation Voltage	$I_{DRIVE} = 20\text{mA}$, $V_{FB} = 1.15\text{V}$ $I_{DRIVE} = 250\text{mA}$, $V_{FB} = 1.15\text{V}$		0.2 1	V V

DICE/DWF SPECIFICATION

RH1573K

DICE/DWF ELECTRICAL TEST LIMITS $T_A = 25^\circ\text{C}$.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
SHDN Pin Threshold Voltage		1	1.5	V
SHDN Pin Current	$V_{\text{SHDN}} = 5\text{V}$		300	μA
LATCH Pin Latch-Off Threshold Voltage		1.1	1.8	V
LATCH Pin Charging Current		4	10	μA
LATCH Pin Latching Current			0.85	mA
V_{IN} to V_{OUT} Differential Threshold for Latch Disable		0.55	0.8	V
Input Quiescent Current	$V_{\text{IN}} = 7\text{V}$		2.8	mA
Minimum Input Voltage for Bias Operation		2.4		V

Note 1: For circuit operation and application information refer to LT1573 data sheet.

Note 2: For post radiation performance contact factory.


Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

I.D.No. 66-13-rh1573

2

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT 0808 • PRINTED IN USA
LINEAR
TECHNOLOGY

© LINEAR TECHNOLOGY CORPORATION 2008