Modem/Telephony Codec

AD1803

FEATURES

- Low power modem/telephony codec
- 16-bit oversampling Σ-Δ converter technology
- Intel® AC '97 Rev 2.1-compliant modem codec implementation
- AC '97 or DSP style serial interface
- Supports all modem/fax standards, including V.90
- Multiple crystal/clock rates supported
- Programmable gain, attenuation, and mute
- On-chip signal filters
  - Digital interpolation and decimation filters
  - Analog output low pass
- Programmable sample rates
  - From 6.4 kHz to 16 kHz
  - With 1 Hz, 8/7 Hz, and 10/7 Hz resolution
- Digital codec engine with variable sample rate conversion
- Digital monitor speaker output
- 24-lead TSSOP
- 0.6 µm CMOS technology
- Operation from 3.3 V or 5 V supply
- Advanced power management

APPLICATIONS

- Modems (PC and embedded)
- Voice and telephony
- Fax machines, answering machines, speakerphones
- PBX systems
- Smart appliances

FUNCTIONAL BLOCK DIAGRAM

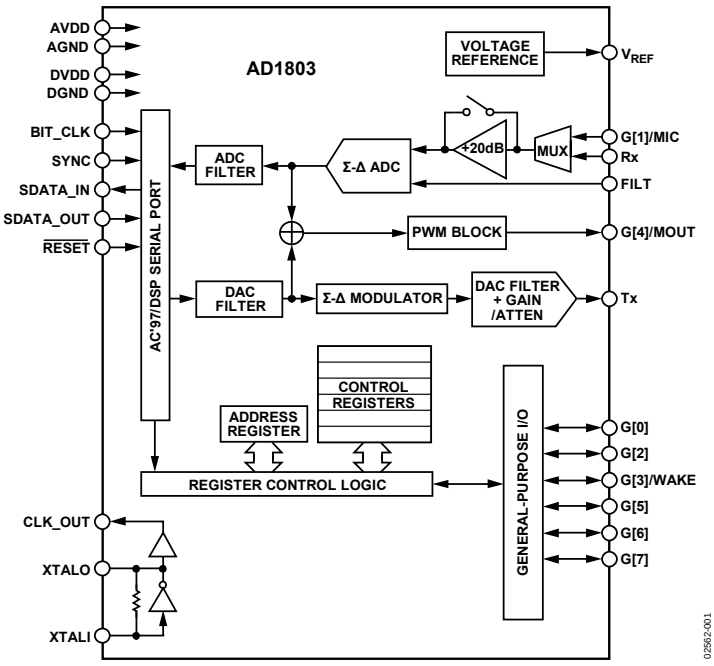

Figure 1.

GENERAL DESCRIPTION

The AD1803 is a low power, 16-bit codec for modem, voice/handset, and telephony applications. It can also be used as a cellular telephone interface.

The AD1803 is an Intel AC '97 Rev 2.1-compliant modem codec (refer to documentation about the Intel AC '97) with selectable AC '97 or a DSP-style serial interface.

The AD1803 codec uses high performance Σ-Δ ADCs and DACs with programmable gain/attenuation. It has a digital Σ-Δ monitor output with selectable mix from ADC and DAC channels for call progress monitoring.

The AD1803 supports advanced power management with several power saving modes. The codec supports seven general-purpose input/output (GPIO) pins and a wake interrupt signaling mechanism on GPIO events.

The AD1803JRUZ is a lead-free environmentally friendly product. It is manufactured using the most up-to-date mate rials and processes. The coating on the leads of each device is 100% pure tin electroplate. The device is suitable for lead-free applications and can withstand surface-mount soldering at up to 255°C (±5°C). In addition, it is backward compatible with conventional tin-lead soldering processes. This means that the electroplated tin coating can be soldered with tin-lead solder pastes at reflow temperatures of 220°C to 235°C.

Rev. A

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REVISION HISTORY

12/06—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to Figure 18 ... 28
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8/01—Revision 0: Initial Version

SPECIFICATIONS

TEST CONDITIONS

Test conditions for the AD1803 are as follows, unless otherwise noted.

General Test Conditions

Temperature at 25°C
Digital supply at 3.3 V/5 V
Analog supply at 3.3 V/5 V
Sample rate (f_S) at 8 kHz
Input signal at 1008 Hz
Analog output pass band at 20 Hz to 4 kHz
ADC FFT size at 512
DAC FFT size at 4096
V_{IH} @ 2.1 V
V_{IL} @ 1.2 V
V_{OH} @ 2.9 V
V_{OL} @ 0.3 V
I_{OH} @ −2.0 mA
I_{OL} @ +2.0 mA

DAC Output Test Conditions

0 dB attenuation relative to full scale
Input 0 dB
Mute Off
10 kΩ output load

ADC Input Test Conditions

Autocalibrated
0 dB PGA gain
Mute off
Input: 1.0 dB relative to full scale

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC RECEIVE PATH					
Full-Scale Input Voltage[1]	PGA gain = 0 dB, offset error = 0% of FS		1.56		V rms
AD1803 Rx Input	0 dBm	2.1	2.2	2.3	V p-p
Resistance—Rx Input[2]					
0 dB Gain			110		kΩ
+20 dB Gain			10		kΩ
Capacitance—Rx Input[2]			15		pF
Rx Programmable Gain					
Gain Step Size[3]	0 dB to 42.5 dB	1.0	1.5	2.0	dB
Input Gain Span[4]		41.5	42.5	43.5	dB
Analog-to-Digital Converter					
Dynamic Range[5]	−60 dB input, PGA gain = 0 dB	85	90		dB
Dynamic Range[2, 5]	−60 dB input, PGA gain = 6 dB		90		dB
Dynamic Range[2, 5]	−60 dB input, PGA gain = +12 dB		90		dB
THD + N	−1 dB input referenced to full scale		−90	−85	dB
Signal-to-Intermodulation Distortion[2]	CCIF method		80		dB
Offset Error	0 V analog input, PGA gain = 0 dB		1	5	% of FS
DAC TRANSMIT PATH					
Digital-to-Analog Converter					
Dynamic Range[5]	−60 dB input, output gain = 0 dB		85		dB
THD + N	−1 dB input referenced to full scale		−75		dB
Signal-to-Intermodulation Distortion[2]	CCIF method		80		dB
Total Out-of-Band Energy[2]	Measured from 0.555 × f_S to 100 kHz			−40	dB
DC Offset			100		mV
Programmable Gain/Attenuator					
Step Size[3]	+12 dB to −34.5 dB	1.0	1.5	2.0	dB
Output Attenuation Span		45.5	46.5	48	dB
Full-Scale Output Voltage					
Tx Output	0 dBm	2.1	2.2	2.3	V p-p
Tx Pin Capacitance			15		pF
Tx Load Capacitance			100		pF

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MONITOR OUTPUT					
Digital-to-Analog Converter					
Dynamic Range[2, 5]	−60 dB input, A-weighted		50		dB
THD + N[2, 5]			0.316	1	%
			−50	−40	dB
Programmable Gain/Attenuator					
Step Size[2]	−18 dB to +45 dB	2.4	3.0	3.6	dB
Output Attenuation Span[2]			63		dB
DIGITAL DECIMATION AND INTERPOLATION FILTERS[2]					
Pass-Band Edge	−0.22 dB point			$0.445 \times f_S$	Hz
Pass-Band	−3.0 dB point			$0.490 \times f_S$	Hz
Pass-Band Ripple		0.0		−0.2	dB
Transition Band		$0.445 \times f_S$		$0.555 \times f_S$	Hz
Stop-Band Edge[6]		$0.555 \times f_S$			Hz
Stop-Band Rejection	Plus 3 dB roll-off	78.0			dB
Group Delay				$21/f_S$	s
Group Delay Variation Over Pass Band					
0 kHz to 4 kHz				0.45	µs
0 kHz to 8 kHz				1.30	µs
Sample Rate		6.4		16	kHz
STATIC DIGITAL					
V_{IH}, High Level Input Voltage	Digital Inputs	0.65 × DVDD			V
V_{IL}, Low Level Input Voltage			0.35 × DVDD		V
V_{OH}, High Level Output Voltage	I_{OH} = −0.5 mA	0.9 × DVDD			V
V_{OL}, Low Level Output Voltage	I_{OL} = +0.5 mA		0.1 × DVDD		V
Input Leakage Current		−10	+10		µA
Output Leakage Current		−10	+10		µA
POWER SUPPLY					
AVDD Range	3.3 V/5 V	3.0/4.75		3.6/5.25	V
DVDD Range	3.3 V/5 V	3.0/4.75		3.6/5.25	V
Analog and Digital Supply Current	5 V, see Table 2				
Analog and Digital Supply Current	3.3 V, see Table 2				
Power Supply Rejection[7]	100 mV p-p, signal @ 1 kHz		40		dB
CLOCK					
Input Clock Frequency		12.288	24.576	32.768	MHz
Recommended Clock Duty Cycle		45	50	55	%

[1] RMS values assume sine wave input.
[2] Guaranteed by design, not production tested.
[3] All steps tested.
[4] The ADC gain is achieved using a 0 dB to 22.5 dB variable gain stage and a 20 dB fixed gain stage. The 22.5 dB to 42.5 dB gain steps are achieved by enabling the 20 dB gain stage.
[5] THD + N referenced to full scale.
[6] The stop band repeats itself at multiples of $64 \times f_S$, where f_S is the sampling frequency. The digital filter attenuates to −78.0 dB or better across the frequency spectrum, except for a range $\pm 0.555 \times f_S$ wide at multiples of $64 \times f_S$.
[7] At both analog and digital supply pins (both ADCs and DACs).

TYPICAL SUPPLY CURRENT

Typical supply current is for most common modes of operation. All currents in mA, unless otherwise noted.

Table 2.

Resource	3.3 V	5.0 V	Register Writes to Enter Mode
GPIO Weak Pull-Up Current per Pin	~100	~140 µA	Default settings after power-on $\overline{\text{RESET}}$
$\overline{\text{RESET}}$ is Asserted			
XTALI Off (All Down)[1]	<30.0	<40.0 µA	Default settings after power-on $\overline{\text{RESET}}$
XTALI Enabled: Nominal Power	1.4	2.4	5C:R34P4 = 1
XTALI Enabled: Low Power	1.0	1.7	5C:R34P4 = 1, 64b1:XTLP = 1
CLK_OUT Pin Running[2]	1.6	3.2	5C:CLKEA = 1
$\overline{\text{RESET}}$ is Deasserted and Analog and Digital Codec in Full Power Mode			
SPORT and CLK_OUT Active[2, 3]	2.6	6.4	Default settings after power-on $\overline{\text{RESET}}$
XTALI in Low Power Mode[2, 3]	2.2	5.7	64b1:XTLP = 1
CLK_OUT Inactive (Low)[3]	1.7	4.3	5C:CLKED = 0
V_{REF} Powered Up[3]	1.9	4.5	3E:VPDN = 0
ADC Enabled	7.3	12.4	3E:APDN = 0
DAC Enabled[3, 5]	8.2	13.7	3E:DPDN = 0
ADC + DAC Enabled[3, 5]	9.2	14.7	3E:APDN = DPDN = 0
ADC, DAC, + MON Enabled[3, 4, 5]	9.3	14.9	3E:APDN = DPDN = 0, 5E:GPMON = 1
ADC, DAC, + MON Enabled[3, 5, 6]	10.2	16.3	3E:APDN = DPDN = 0, 5E:GPMON = 1

[1] Assumes all inputs are static (not switching) and all output loads are capacitive (nonresistive).
[2] Excludes current drawn by CLK_OUT pin board loading.
[3] Assumes the serial interface is configured in AC '97 primary mode with 20 pF loads on the SDATA_IN pin and BIT_CLK pin. Typical current is approximately 0.8 mA less if the serial interface is configured in DSP mode with 20 pF loads on the SYNC pin, BIT_CLK pin, and SDATA_IN pin (due to a lower BIT_CLK frequency).
[4] Assumes a 20 pF load on the G[4]/MOUT pin.
[5] Assumes no DAC load, 0.6 mA should be added if a 600 Ω load is used.
[6] Assumes the G[4]/MOUT pin is loaded with a 1 kΩ resistor in series with a parallel 4.7 kΩ resistor and 100 nF capacitor combination tied to digital ground. This filter, with the output taken from the middle node, has a 1500 Hz corner to filter out high-frequency Σ-Δ noise. It generates an approximate 1 V p-p output when using a 5 V digital supply with the monitor output configured as first order (Bit MMD1 and Bit MMD0 set to 10 in Register 0x60 Bank 2) if the filter output load is greater than or equal to 20 kΩ.

TIMING SPECIFICATIONS

Table 3.

Parameter[1]	Symbol	Min	Typ	Max	Unit
SERIAL PORT— AC '97 MODE					
$\overline{\text{RESET}}$ Active Low Pulse Width	t_{RST_LOW}	1.0			µs
$\overline{\text{RESET}}$ Inactive to BIT_CLK Start-Up Delay	$t_{RST2CLK}$	162.8			ns
SYNC Active High Pulse Width (Warm $\overline{\text{RESET}}$)	t_{SYNC_HIGH}		1.3		µs
SYNC Inactive to BIT_CLK Start-Up Delay (Warm $\overline{\text{RESET}}$)	$t_{SYNC2CLK}$	162.8			ns
BIT_CLK Frequency			12.288		MHz
BIT_CLK Period	t_{CLK_PERIOD}		81.4		ns
BIT_CLK Output Jitter[2]				750	ps
BIT_CLK High Pulse Width	t_{CLK_HIGH}	36.62	40.69	44.76	ns
BIT_CLK Low Pulse Width	t_{CLK_LOW}	36.62	40.69	44.76	ns
SYNC Frequency			48.0		kHz
SYNC Period	t_{SYNC_PERIOD}		20.8		µs
Setup to Falling Edge of BIT_CLK	t_{SETUP}	10.0			ns
Hold from Falling Edge of BIT_CLK	t_{HOLD}	10.0			ns
Propagation Delay	t_{CO}			15	ns
BIT_CLK Rise Time	$t_{RISECLK}$	2	4	6	ns
BIT_CLK Fall Time	$t_{FALLCLK}$	2	4	6	ns
SYNC Rise Time	$t_{RISESYNC}$	2	4	6	ns
SYNC Fall Time	$t_{FALLSYNC}$	2	4	6	ns
SDATA_IN Rise Time	$t_{RISEDIN}$	2	4	6	ns
SDATA_IN Fall Time	$t_{FALLDIN}$	2	4	6	ns
SDATA_OUT Rise Time	$t_{RISEDOUT}$	2	4	6	ns
SDATA_OUT Fall Time	$t_{FALLOUT}$	2	4	6	ns
End of Slot 2 to BIT_CLK, SDATA_IN Low (MLNK Set)	t_{S2_PDOWN}	2		1000	ns
Setup to Trailing Edge of $\overline{\text{RESET}}$ (Applies to SYNC, SDATA_OUT)	$t_{SETUP2RST}$	15			ns
Rising Edge of $\overline{\text{RESET}}$ to Hi-Z Delay (ATE Test Mode)	t_{OFF}			25	ns
SERIAL PORT—DSP MODE					
$\overline{\text{RESET}}$ Active Low Pulse Width	t_{RST_LOW}	1.0			µs
$\overline{\text{RESET}}$ Inactive to BIT_CLK Start-Up Delay	$t_{RST2CLK}$	162.8			ns
BIT_CLK Frequency			4.096		MHz
BIT_CLK Period	t_{CLK_PERIOD}		244.14		ns
BIT_CLK Output Jitter[2]				750	ps
SYNC Frequency			8		kHz
SYNC Period	t_{SYNC_PERIOD}		125		µs
Setup to Falling Edge of BIT_CLK	t_{SETUP}	10.0			ns
Hold from Falling Edge of BIT_CLK	t_{HOLD}	10.0			ns
Propagation Delay	t_{CO}			15	ns
BIT_CLK Rise Time	$t_{RISECLK}$	2	4	6	ns
BIT_CLK Fall Time	$t_{FALLCLK}$	2	4	6	ns
SYNC Rise Time	$t_{RISESYNC}$	2	4	6	ns
SYNC Fall Time	$t_{FALLSYNC}$	2	4	6	ns
SDATA_IN Rise Time	$t_{RISEDIN}$	2	4	6	ns
SDATA_IN Fall Time	$t_{FALLDIN}$	2	4	6	ns
SDATA_OUT Rise Time	$t_{RISEDOUT}$	2	4	6	ns
SDATA_OUT Fall Time	$t_{FALLDOUT}$	2	4	6	ns
Setup to Trailing Edge of RESET (Applies to SYNC, SDATA_OUT)	$t_{SETUP2RST}$	15			ns
Rising Edge of RESET to Hi-Z Delay (ATE Test Mode)	t_{OFF}			25	ns

[1] Guaranteed over operating temperature range and supply power.
[2] Output jitter is directly dependent on crystal input jitter.

TIMING DIAGRAMS

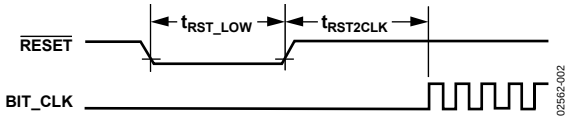

Figure 2. Cold $\overline{RESET}$

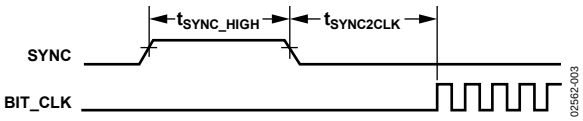

Figure 3. Warm $\overline{RESET}$

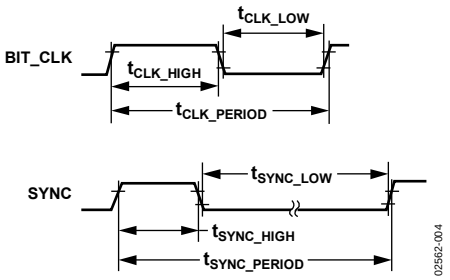

Figure 4. Clock Timing

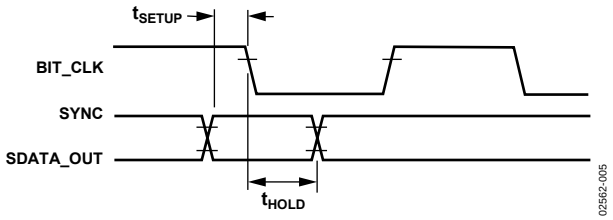

Figure 5. Data Setup and Hold

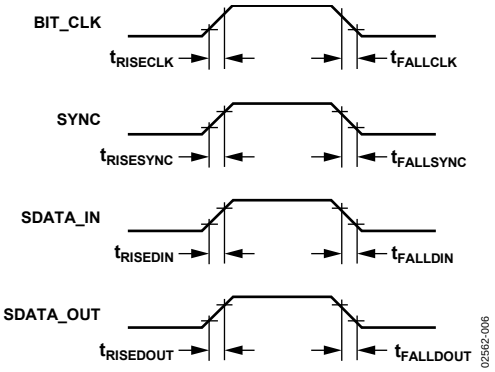

Figure 6. Signal Rise and Fall Time

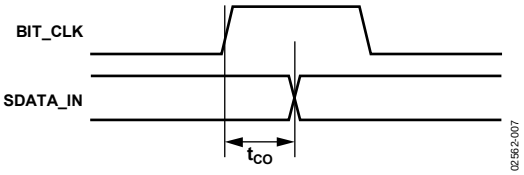

Figure 7. Propagation Delay

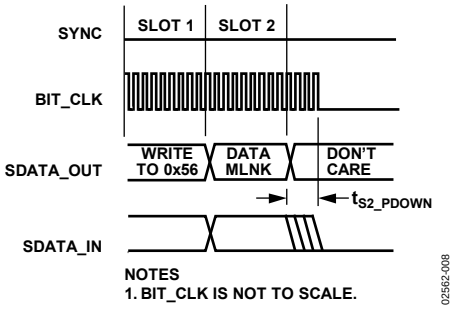

Figure 8. AC Link Low Power Mode Timing

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Power Supplies	
Digital (DVDD)	−0.3 V to +6.0 V
Analog (AVDD)	−0.3 V to +6.0 V
Input Current (Except Supply Pins)	±10.0 mA
Analog Input Voltage (Signal Pins)	−0.3 V to AVDD + 0.3 V
Digital Input Voltage (Signal Pins)	−0.3 V to DVDD + 0.3 V
Operating Ambient Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating

$T_{AMB} = T_{CASE} - (P_D \times \theta_{CA})$

where:
T_{CASE} is the case temperature in °C,
P_D is the power dissipation in W,
θ_{CA} is the thermal resistance (case-to-ambient),
θ_{JA} is the thermal resistance (junction-to-ambient),
θ_{JC} is the thermal resistance (junction-to-case).

PACKAGE CHARACTERISTICS

Table 5.

Package	θ_{JA}	θ_{JC}	θ_{CA}
TSSOP	83.8°C/W	15.6°C/W	68.2°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

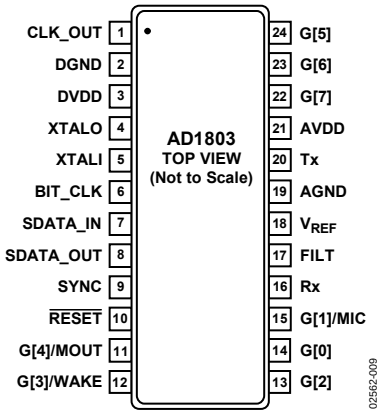

Figure 9. Pin Configuration

Table 6. Pin Function Descriptions

Mnemonic	Pin No.	I/O	Description
ANALOG SIGNALS			
DVDD	3	I	Digital Supply. Range: 5.0 V ± 10% or 3.3 V ± 10% (independent of AVDD).
DGND	2	I	Digital Ground. Must be at same potential as AGND.
AVDD	21	I	Analog Supply. Range is 5.5 V through 3.0 V (independent of DVDD).
AGND	19	I	Analog Ground. Must be at same potential as DGND.
Rx	16	I	Receive (ADC) input.
Tx	20	O	Transmit (DAC) output.
FILT	17	I	ADC Filter Bypass. Requires 1 µF capacitor to AGND.
V_{REF}	18	I	Voltage Reference. Requires 1 µF capacitor to AGND.
CLOCK SIGNALS			
XTALI	5	I	Crystal or Clock Input (12.288 MHz, 24.576 MHz, or 32.768 MHz). This clock input is necessary only if the AD1803 is configured in either AC '97 primary or DSP mode, or if a wake interrupt from an event is required (in any mode). This pin must be tied to DVDD or DGND (not floated) when clock input is not necessary. If a crystal is used, it must be parallel resonant first harmonic, and tied between this pin and the XTALO pin with load capacitance specified by the crystal supplier. See the XTAL1 bit and the XTAL0 bit in Register 0x5C for further details.
XTALO	4	O	Crystal Output. This pin should be floated when a crystal is not used.
CLK_OUT	1	O	Buffered version of clock present on the XTALI pin, unless disabled. See the CLKED bit and CLKEA bit in Register 0x5C for further details.
SERIAL INTERFACE SIGNALS[1]			
$\overline{\text{RESET}}$	10	I	Active Low Power-Down. Level of power-down is determined by bits in Register 0x5C. This pin must be asserted (driven low) as power is first applied until the supply is stable. The AD1803 is $\overline{\text{RESET}}$ exclusively by an internal power-on $\overline{\text{RESET}}$ circuit.
BIT_CLK	6	I/O	Serial Data Clock. Output if the AD1803 configured in AC '97 primary or DSP mode. Input if the AD1803 is configured in any AC '97 secondary mode.
SYNC	9	I/O	Serial Data Frame Sync. Output if the AD1803 is configured in DSP mode. Input if the AD1803 is configured in any AC '97 mode.
SDATA_IN	7	O	Serial Data Output from AD1803.
SDATA_OUT	8	I	Serial Data Input to AD1803.

Mnemonic	Pin No.	I/O	Description
GENERAL-PURPOSE I/O AND BARRIER INTERFACE SIGNALS[2]			
G[0][3, 4]	14	I/O	General-Purpose I/O.
G[1]/MIC[3, 5]	15	I	General-Purpose I/O.
		I	Analog MIC Input. See Bit GPMIC in Register 0x5E.
G[2][3, 4, 6]	13	I/O	General-Purpose I/O. Also used to select serial interface mode.
G[3]/WAKE[3, 4, 6]	12	I/O	General-Purpose I/O.
		O	Wake Interrupt Output (see the GPWAK bit in Register 0x5E). This pin selects the serial interface mode. When serving as WAKE, this pin is driven high if selected GPIO pins receive selected logic levels (see Register 0x52 and Register 0x4E).
G[4]/MOUT[3, 4]	11	I/O	General-Purpose I/O.
		O	Monitor Output. See the Configuration 2 Register section.
G[5][3, 4]	24	I/O	General-Purpose I/O.
G[6][3, 4]	23	I/O	General-Purpose I/O.
G[7][3, 4]	22	I/O	General-Purpose I/O.

[1] See the G[3]/WAKE pin and the G[2] pin for serial interface mode selection.
[2] See Register 0x4C through Register 0x54 and Bank 1 Register 0x60 for the general-purpose I/O pin control.
[3] By default the G[7] pin, G[6] pin, G[5] pin, G[4] pin, G[3] pin, G[2] pin, and G[1] pin serve as inputs with weak (~30 kΩ equivalent) internal pull-up devices enabled.
[4] Input voltage on the G[7] pin, G[6] pin, G[5] pin, G[4] pin, G[3] pin, G[2] pin, and G[0] pin must not exceed DVDD by more than 0.3 V.
[5] Input voltage on Pin G[1] must not exceed AVDD by more than 0.3 V.
[6] The states of the G[3/WAKE] pin and G[2] pin are sampled when $\overline{\text{RESET}}$ is deasserted (driven from low to high) for the first time after power is applied to select AD1803 serial interface mode. Once sampled, serial interface mode can be changed only by removing power from the AD1803.

G[3]/WAKE	G[2]	Serial interface mode
High/High	AC '97	Mode, primary device (ID: 00)
High Low	AC '97	Mode, secondary device (ID: 01)
Low High	AC '97	Mode, secondary device (ID: 10)
Low	Low	DSP mode

THEORY OF OPERATION

SERIAL INTERFACE MODE SELECTION

When power is first applied to the AD1803, $\overline{\text{RESET}}$ must be asserted ($\overline{\text{RESET}}$ pin driven low), and kept asserted until the power has stabilized. While $\overline{\text{RESET}}$ is asserted, the AD1803's serial interface mode is chosen by the state of Pin 12 (G[3]/WAKE) and Pin 13 (G[2]).

Table 7.

Pin 12	Pin 13	Mode Chosen
High	High	AC '97 Mode—Primary Device (ID: 00)
High	Low	AC '97 Mode—Secondary Device (ID: 01)
Low	High	AC '97 Mode—Secondary Device (ID: 10)
Low	Low	DSP Mode

Note that Pin 12 and Pin 13 have weak pull-up devices internal to the AD1803 that are enabled by default. Therefore, if these pins are floated, AC '97 primary mode is chosen. When $\overline{\text{RESET}}$ is deasserted ($\overline{\text{RESET}}$ pin driven high) for the first time after power is applied, the states of Pin 12 and Pin 13 are latched, locking in serial interface mode. Subsequent changes of the logic level presented on Pin 12 and Pin 13 have no effect on serial port mode until power is removed from the AD1803. After this first deassertion of $\overline{\text{RESET}}$, Pin 12 and Pin 13 take on new roles and serve as general-purpose I/O control pins. The AD1803 does not need an active clock source for proper operation during this mode selection.

SERIAL INTERFACE BEHAVIOR AND PROTOCOL WHEN IN AC '97 MODE

The AD1803 serial interface is compatible with the AC '97 Rev 2.1 specification as either a primary or a secondary modem/handset codec device. Consult this specification for complete behavioral details.

By default the AD1803 uses Slot 5 to send and receive sample data, but this can be changed to Slot 10 or Slot 11. See the SPCHN bit, SPGBP bit, SPDSS bit, SPISO bit, SPDL1 bit, and SPDL0 bit in Register 0x5E for additional AC '97 mode configuration enhancements.

AC '97 INTERFACE MODES

Primary Mode

Entered if G[3] pin and G[2] pin are high when the $\overline{\text{RESET}}$ pin is deasserted for the first time:

- AD1803 is the timing master: drives BIT_CLK at 12.288 MHz.
- AD1803 accepts the 48 kHz SYNC timing signal.
- AD1803 requires a crystal or clock on XTALI (see the XTAL1 bit and XTAL0 bit in Register 0x5C for frequency).

Secondary Mode

Entered if the G[3] pin is high and G[2] pin is low when the $\overline{\text{RESET}}$ pin is deasserted for the first time or if the G[3] pin is low and the G[2] pin is high when the $\overline{\text{RESET}}$ pin is deasserted for the first time:

- AD1803 is the timing slave: accepts BIT_CLK at 12.288 MHz.
- AD1803 accepts the 48 kHz SYNC timing signal.
- AD1803 does not require a crystal or clock on XTALI (see the XTAL1 bit and XTAL0 bit in Register 0x5C for frequency), unless wake from an event during $\overline{\text{RESET}}$ is desired. XTALI okay here?

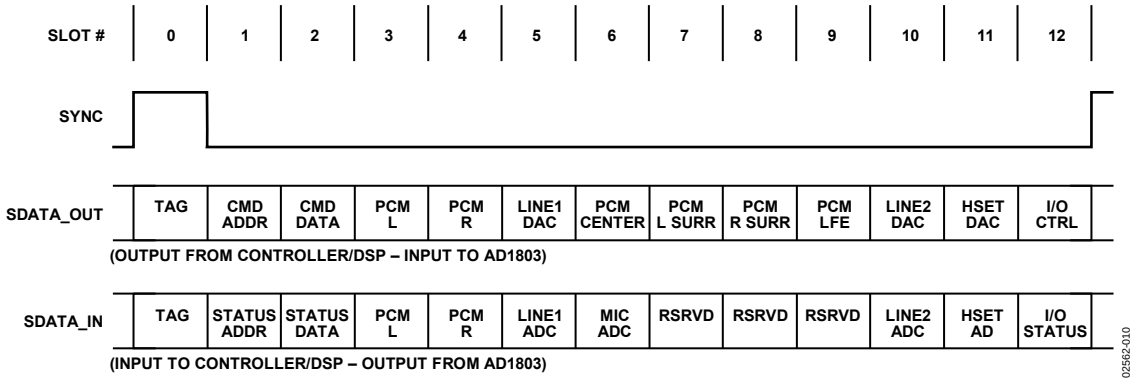

Figure 10. AC '97 Interface Timing

SERIAL INTERFACE BEHAVIOR AND PROTOCOL WHEN IN DSP MODE

In DSP mode, the AD1803 requires a clock on XTALI to function properly. This clock can be created by placing a crystal between Pin XTALI and Pin XTALO with appropriate trim capacitors. Alternatively, a clock can be driven directly onto the XTALI pin from an external source, in which case XTALO must be floated. When the AD1803 serial interface is configured in DSP mode, the clock presented on the XTALI pin is assumed to be 24.576 MHz. However, a 12.288 MHz or 32.768 MHz clock could be used instead, providing

- A register write informs the AD1803 of the true clock frequency before the codec is enabled.
- It is acceptable to have the serial port bit clock and frame sync run at rates different from the start-up nominal until the AD1803 is informed of the true XTALI clock frequency.

Within 1 ms after $\overline{\text{RESET}}$ is deasserted and the AD1803 receives a clock on XTALI, the AD1803 begins driving a 4.096 MHz bit clock onto the BIT_CLK pin (assuming a 24.576 MHz XTALI clock). Approximately 100 µs later, the AD1803 begins driving an 8 kHz frame sync onto the SYNC pin (again assuming a 24.576 MHz XTALI clock). If the AD1803 receives an XTALI clock that is higher/lower than the expected 24.576 MHz default, these frequencies are scaled up/down (lineally) until the AD1803 is informed of the actual XTALI clock frequency by a write to the XTAL1 and XTAL0 bits in Register 0x5C. See the XTAL1 and XTAL0 bits for further details including allowed alternate XTALI frequencies.

Each serial interface frame consists of a single 16-bit word sent into the AD1803 on the SDATA_OUT pin, and a single 16-bit word sent out of the AD1803 on the SDATA_IN pin. These words are simultaneously transferred during the first 16 clocks of the BIT_CLK pin after the start of a frame. The start of a frame is marked by one BIT_CLK long high pulse of the SYNC pin one BIT_CLK period before the first bit in the frame. Data is transmitted MSB first. Logic levels on all pins (SYNC, SDATA_IN, and SDATA_OUT) are updated on BIT_CLK rising edges, and should be sampled on BIT_CLK falling edges.

By default, all frames are designated as data frames for delivery of two's complement DAC and ADC samples to and from the AD1803 codec. To deliver control information into the part, the LSB of the word into the AD1803 is stolen, from what might otherwise have been DAC data, to serve as a control frame request bit.

While the AD1803 provides 16-bit ADC sample output, only 15-bit DAC sample input is possible because of this. If the LSB of the word into the AD1803 is set to 0, no control frame is requested and the next frame is another data frame. If the LSB of the word into the AD1803 is set to 1, a control frame is requested and the next frame is a control frame.

When a control frame is requested, an extra frame is inserted between data frames avoiding an interruption of codec sample data flow. The 16-bit control word into the AD1803 consists of (from MSB to LSB):

- A register read/write request bit (0 to request a write, 1 to request a read).
- The 6 MSBs of a 7-bit register address (where the LSB is removed to save space since it is always a 0).
- A byte select bit (0 to select the lower byte of the 16-bit control register addressed, 1 to select the upper byte of the 16-bit control register addressed).
- Eight bits of data that are written into the addressed register if a write is requested. Otherwise, these last eight bits are ignored.

While it seems peculiar to have a 7-bit register address with the LSB dropped when sent to the AD1803, it should be noted that AD1803 register addresses are defined by the AC '97 specification, whether configured in an AC '97 mode or in DSP mode. While the AC '97 Rev 2.1 specification reserves odd addresses for future feature expansion, there was no room in the DSP mode control word for this unused bit. The 16-bit control word out of the AD1803 consists of, from MSB to LSB, eight unused bits that are always set to 0, followed by eight bits of data that reflect the contents of the register addressed within the current frame, if a read was requested. Otherwise, they are all set to 0.

When serial interface frames first commence after $\overline{\text{RESET}}$ is deasserted, there are 512 bits per frame (8 kHz frame rate/ 4.096 MHz bit clock rate) where only the first 16 bits per frame are typically utilized. Bits out of the AD1803 after the first 16 are typically set to 0, and bits into the AD1803 after the first 16 are typically ignored. However, when a control frame is requested via the control frame request bit in a data frame, the control frame is inserted between data frames and placed 256 bits after the start of the data frame that requested the control frame. This control frame is marked by an additional 1-bit long clock pulse, high of the SYNC pin. Note that the spacing between data frames is never affected by the insertion of a control frame.

The frame rate at startup is 8 kHz and there are exactly 512 bits from the start of one data frame to the next; this changes as soon as the codec is enabled (the codec is powered down by default after power is first applied to the AD1803). Whenever the codec is enabled, the frame rate is switched from 8 kHz to the programmed codec sample rate, and whenever the codec is powered down again, the frame rate switches back to 8 kHz. With the bit clock always fixed at 4.096 MHz, this gives rise to a first cause of variation in the number of bits between starts of data frames. A second cause of a varying number of bits between starts of data frames is the presence of a subtle jitter in the assertion of frame sync when the codec is enabled. On average, there is an exact match between the programmed sample rate and the frame rate; the frame sync itself varies up to 4% of a sample period from the ideal assertion point in time.

When the serial interface is in DSP mode, it is possible to access only the upper or lower 8-bit byte of a 16-bit control register at a time. While this is sufficient for manipulating many of the AD1803 features, some features require more than eight control bits and span multiple 8-bit bytes and/or multiple 16-bit words.

To allow all bits of a feature to take effect simultaneously, writes to certain control bytes of certain registers are actually held in holding latches until a particular control byte of the feature is written. Note that a read of a control register always returns the contents of a holding latch (if present for that register), which does not necessarily reflect the control setting currently being used by the AD1803. The only feature that incorporates this complication is the codec sample rate, which writes to the lower byte of Register 0x40 and does not take effect until the upper byte of Register 0x40 is written.

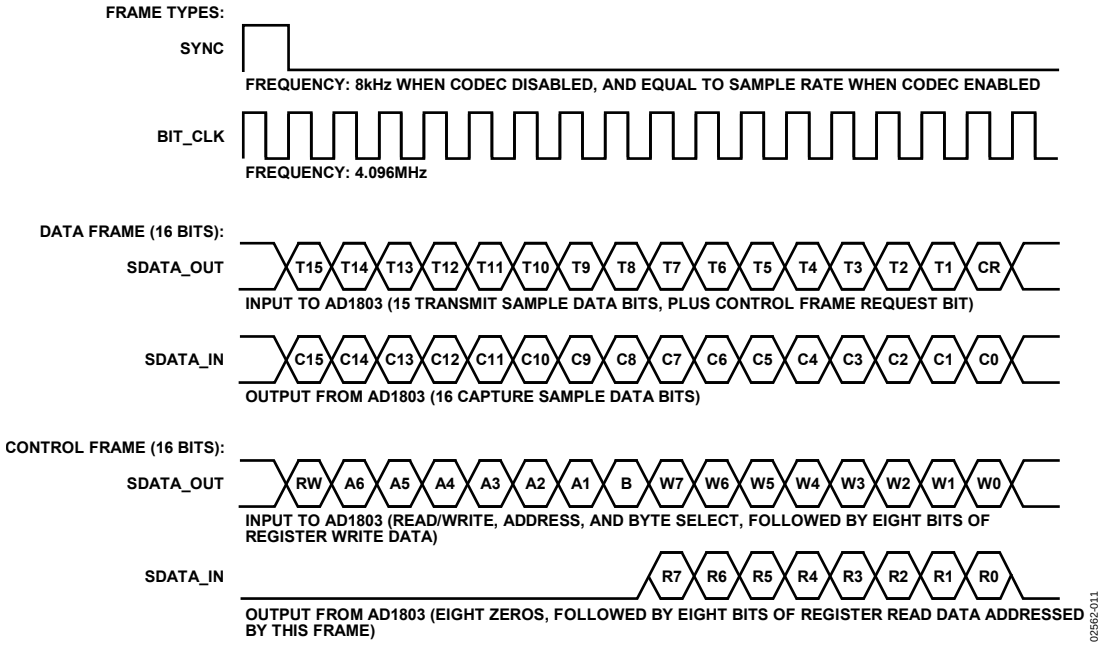

Figure 11. Frame Types

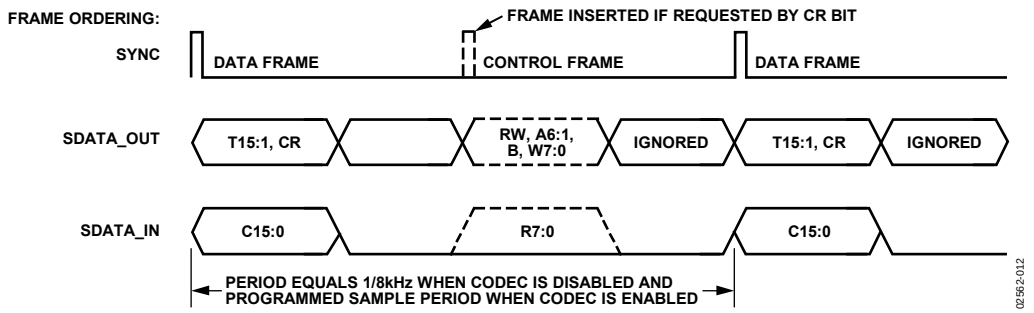

Figure 12. Frame Ordering

REGISTER BANKS

Register addresses are based on the Intel AC '97 specification. Because the AC '97 specification lacks sufficient vendor defined register space to control all extended features of the AD1803, some control registers must be accessed indirectly using register banks. See the BNK1 and BNK0 bits in Register 0x5C for details.

REGISTER ACCESS RESTRICTIONS

Nearly all control registers can be read from or written to at any time. Below is a list of restrictions that must be followed to ensure proper operation of the AD1803:

- The clock frequency delivered to the AD1803 on XTALI must be identified (via a write to the XTAL1 bit and XTAL0 bit in Register 0x5C) before the codec is enabled (via a write of 0 to Bits DPDN or APDN in Register 0x3E).
- During ADC calibration, codec sample rate (Register 0x40), and ADC source and gain level must not be changed. Calibration is initiated each time the AD1803's ADC is enabled (see Bit APDN in Register 0x3E) and whenever a 1 is written to Bit ADCAL in Register 0x5C. Completion of calibration is determined by polling the ADCAL bit.

GENERAL-PURPOSE I/O PIN OPERATION

Refer to Registers 0x4C through 0x54 and Register 0x60 for complete details (see Figure 13).

Table 8. Voice Features

Feature	AD1803
Power Supply	3 V to 5 V
Maximum Sampling Frequency	16 kHz
Differential Handset Output	No
Single-Ended Line Output	Yes, 600 Ω load
Output Full-Scale Range	2.2 V p-p
Output Attenuation Steps	+12 dB to −34.5 dB
Input Line/MIC Mux	Yes
Input Full-Scale Range	0.777 V rms, 2.2 V p-p
Input 0 dB/20 dB Gain Block	Yes
PGA, 0 dB to 22.5 dB Range	Yes
Single-Ended Input	Yes
Differential Input	No
Input Resistance	10 kΩ min varies with gain (see Table 9)

Table 9. Input Resistance vs. Gain Setting

PGA Gain (dB)	20 dB Gain Block	PGA Gain (dB)	R_{IN} (kΩ)
0.0 to 22.5	Disabled	0.0 to 22.5	100
0.0 to 22.5	Enabled	20.0 to 42.5	10

CONTROL REGISTER MAP

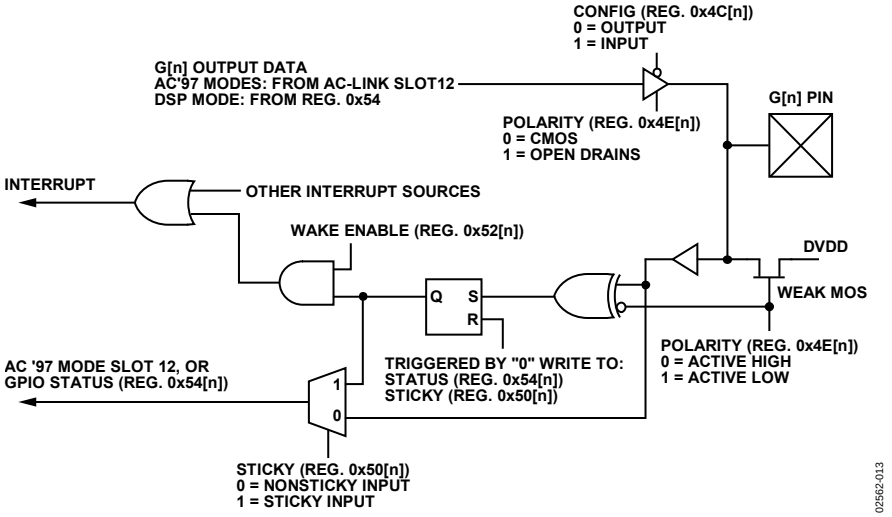

Figure 13. Conceptual Diagram of GPIO Pin Behavior

Table 10. Register Summary (Direct Mapped Registers)

Address	Register Name
0x3C	Extended Modem ID
0x3E	Extended AD1803 Status and Control
0x40	Line DAC/ADC Sample Rate Control
0x46	AD1803 DAC/ADC Level Control
0x4C	GPIO Pin Configuration
0x4E	GPIO Pin Polarity/Type
0x50	GPIO Pin Sticky
0x52	GPIO Pin Wake-Up Mask
0x54	GPIO Pin Status
0x56	Miscellaneous Modem AFE Status and Control
0x5C	Configuration 1
0x5E	Configuration 2
0x7A	Version ID
0x7C	Vendor ID1
0x7E	Vendor ID2

Table 11. Register Summary (Indirect Mapped Registers)

Address	Register Name
0x60	Bank 1—GPIO initial states
0x64	Bank 1—clock pad control
0x60	Bank 1—monitor output control

Table 12. Register Map

Adr/Bnk	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x3C	0xX00X	ID1	ID0	0	0	0	0	0	0	0	0	0	0	0	0	0	LIN1
0x3E	0xFF00	Res	Res	Res	Res	DPDN	APDN	VPDN	GPDN	0	0	0	0	DSTA	ASTA	VSTA	GSTA
0x40	0x3E80	SRG1	SRG0	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
0x46	0x8080	DAM	0	0	DAL4	DAL3	DAL2	DAL1	DAL0	ADM	0	ADS	ADG20	ADL3	ADL2	ADL1	ADL0
0x4C	0x00FF	0	0	0	0	0	0	0	0	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0
0x4E	0x00FF	0	0	0	0	0	0	0	0	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
0x50	0x0000	0	0	0	0	0	0	0	0	GS7	GS6	GS5	GS4	GS3	GS2	GS1	GS0
0x52	0x0000	0	0	0	0	0	0	0	0	GW7	GW6	GW5	GW4	GW3	GW2	GW1	GW0
0x54	0x00FF	0	0	0	0	0	0	0	0	GI7	GI6	GI5	GI4	GI3	GI2	GI1	GI0
0x56	0x0000	0	0	0	MLNK	0	0	0	0	0	0	0	0	0	L1B2	L1B1	L1B0
0x5C	0x18C0	Res	BNK1	BNK0	R34PM	XTAL1	XTAL0	ACSEL	ADCAL	CLKED	CLKEA	Res	Res	Res	Res	Res	Res
0x5E	0x0018	GPBAR	GPWAK	GPMON	GPMIC	SPCHN	SPGBP	SPDSS	SPISO	SPDL1	SPDL0	Res	Res	Res	Res	Res	Res
0x60/1	0x0000	0	0	0	0	0	0	0	0	GPIV7	GPIV6	GPIV5	GPIV4	GPIV3	GPIV2	GPIV1	GPIV0
0x64/1	0x0077	0	0	0	0	0	0	0	0	Res	Res	Res	Res	XTLP	COS2	COS1	COS0
0x60/2	0x4000	MMD1	MMD0	MDM	MDL4	MDL3	MDL2	MDL1	MDL0	Res	Res	MAM	MAL4	MAL3	MAL2	MAL1	MAL0
0x7A	0x0002	0	0	0	0	0	0	0	0	VER7	VER6	VER5	VER4	VER3	VER2	VER1	VER0
0x7C	0x4144	0	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0
0x7E	0x5380	0	1	0	1	0	0	1	1	1	0	0	0	0	0	0	0

CONTROL REGISTER DETAILS

EXTENDED MODEM ID REGISTER

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x3C	ID1	ID0	0	0	0	0	0	0	0	0	0	0	0	0	0	LIN1	0xX00X

A write to this register has no effect on the states of bits within this register, but does trigger Register 0x3E and Bank 2 Register 0x60 to be cleared to their default states, powering down the AD1803's codec resources.

Bit Name	Description
ID1, ID0	Interface Identification. These bits can be read to determine the AD1803's serial interface mode of operation. Serial interface mode is chosen by the states of Pin 13 and Pin 12 when $\overline{\text{RESET}}$ is deasserted ($\overline{\text{RESET}}$ pin driven from low to high) for the first time after power is applied to the AD1803. 00 = AC link primary (mode chosen if Pin 12 is high and Pin 13 is high on first deassertion of $\overline{\text{RESET}}$). 01 = AC link secondary (mode chosen if Pin 12 is high and Pin 13 is low on first deassertion of $\overline{\text{RESET}}$). 10 = AC link secondary (mode chosen if Pin 12 is low and Pin 13 is high on first deassertion of $\overline{\text{RESET}}$). 11 = DSP link (mode chosen if Pin 12 is low and Pin 13 is low on first deassertion of $\overline{\text{RESET}}$).
LIN1	Modem Line 1 Supported. For AC '97 compatibility, this bit returns a 1 when read to indicate that the AD1803 supports AC '97 modem line 1 features.

EXTENDED STATUS AND CONTROL REGISTER

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x3E	Res[1]	Res[1]	Res[1]	Res[1]	DPDN	APDN	VPDN	GPDN	0	0	0	0	DSTA	ASTA	VSTA	GSTA	0xFF00

[1] Res = reserved bit. To ensure future compatibility, reserved bits should be set to 0 when written and ignored when read.

This register is forced to its default when power is first applied to the AD1803, the $\overline{\text{RESET}}$ pin is driven low, or Register 0x3C is written with any value.

Bit Name	Description
DPDN	DAC Power-Down. When this bit is set to 1 (default), all DAC resources within the AD1803 are powered down, and all DAC data sent over the serial interface is ignored. When this bit is set to 0, the digital DAC resources are powered up. The analog DAC resources are powered up only if the voltage reference of the AD1803 is powered up (Bit VPDN in this register is set to 0), and the analog codec of the AD1803 is selected as the partner to the digital codec of the part (Bit ACSEL in Register 0x5C is set to 0). 0 = Enable digital DAC resources; conditionally enable analog DAC resources. 1 = Power-down all AD1803 DAC resources (default).
APDN	ADC Power-Down. When this bit is set to 1 (default), all ADC resources within the AD1803 are powered down, and all ADC data-words sent out of the AD1803 over the serial interface are midscale (zero) and tagged invalid if the serial interface is configured in an AC '97 mode. When this bit is set to 0, the digital ADC resources within the AD1803 are powered up. The analog ADC resources within the AD1803 are powered up only if both the voltage of the AD1803 reference is powered up (Bit VPDN in this register is set to 0), and the analog codec of the AD1803 is selected as the partner to the digital codec of the part (Bit ACSEL in Register 0x5C is set to 0). Each time the analog codec is powered up, an ADC dc offset calibration is automatically initiated. This calibration requires approximately 104 sample periods (defined by Register 0x40). It cannot be started until after the voltage reference is powered up (set Bit VPDN in this register to 0), which requires about 48 ms. Bit VSTA in this register can be polled first to determine if the voltage reference is powered up and then Bit ADCAL in Register 0x5C can be polled to determine if calibration is complete. During calibration, codec sample rate, ADC source, and ADC gain level must not be changed. 0 = Enable AD1803 digital ADC resources; conditionally enable AD1803 analog ADC resources. 1 = Power-down all AD1803 ADC resources (default).
VPDN	Voltage Reference Power-Down. Writes to this bit initiate codec voltage reference power-up and power-down sequences. Bit VSTA in this register can be polled to monitor current voltage reference status. Until the voltage reference is powered up, the analog ADC and DAC channels of the AD1803 ignore the settings of Bit APDN and Bit DPDN and the part remains powered down. 0 = Enable voltage reference. 1 = Power-down voltage reference (default).

Bit Name	Description
GPDN	GPIO Power-Down. Setting this bit affects the behavior of the AD1803 only when it is configured in an AC '97 mode (see Register 0x3C). This bit determines whether the logic levels received on the general-purpose input/output (GPIO) pins are reflected on the bits in Slot 12 of the AC '97 link, and whether or not the states of bits in Slot 12 determine the logic levels to drive out of GPIO pins that are configured as outputs. See Bit SPGBP in Register 0x5E for mapping. Contrary to the AC '97 specification, the setting of this bit does not actually control the power-up/power-down state of the GPIO pins. AD1803 GPIO pins are powered up and perform the functions they are assigned by programming Register 0x4C through Register 0x54 and Register 0x5E. 0 = Slot 12 output bits reflect logic levels received on GPIO pins. Slot 12 input bits determine logic bevels to drive out GPIO pins configured as outputs. 1 = Slot 12 output bits all 0 (default). Slot 12 input bits are ignored.
DSTA	DAC Status. This bit exists solely for AC '97 compatibility. Its purpose is to provide a handshake for DAC power-up/power-down status changes initiated by writes to Bit DPDN in this register. Because the AD1803 responds to a write of Bit DPDN before it is possible to read this bit in a following serial interface frame, there is no reason to poll this status bit. Writes to this bit have no effect on AD1803 behavior.
ASTA	ADC Status. This bit exists solely for AC '97 compatibility. Its purpose is to provide a handshake for ADC power-up/power-down status changes initiated by writes to Bit APDN in this register. Because the AD1803 responds to a write of Bit APDN prior to it being possible to read this bit in a following serial interface frame, there is no reason to poll this status bit. Writes to this bit have no effect on AD1803 behavior.
VSTA	Voltage Reference Status. This bit can be polled to monitor the status of the codec voltage reference of the AD1803. When read as a 0, the voltage reference is powered down or in the process of powering up. When read as a 1, the voltage reference is powered up or in the process of powering down. Approximately 48 ms after Bit VPDN in this register is set to a 0, this bit transitions from a 0 to a 1 indicating that the voltage reference is fully powered up. Approximately 0.8 ms after VPDN is set to a 1, this bit transitions from a 1 to a 0 indicating that the voltage reference is fully powered-down. If a clock is driven onto the XTALI pin (rather than generated by a crystal placed between the XTALI pin and XTALO pin), and it is desired to stop this clock for additional system power savings, stop the clock after this bit falls to 0. Writes to this bit have no effect on the behavior of the AD1803.
GSTA	GPIO Status. This bit exists solely for AC '97 compatibility. Its purpose is to provide a handshake for DAC power-up/power-down status changes initiated by writes to Bit GPDN in this register. However, since the AD1803 responds to a write of Bit GPDN prior to it being possible to read this bit in a following serial interface frame, there is no reason to poll this status bit. Writes to this bit have no effect on the behavior of the AD1803.

LINE DAC/ADC SAMPLE RATE CONTROL REGISTER

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x40	SRG1	SRG0	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	0x3E80

This register is forced to its default only when power is first applied to the AD1803. Do not write to this register while an ADC calibration is in progress (see Bit APDN in Register 0x3E and Bit ADCAL in Register 0x5C).

When the AD1803 serial interface is configured in DSP mode, writes to the lower byte of this register are temporarily placed in a holding register and do not actually take effect until the upper byte is written. This ensures that the 16-bit sample rate only takes effect as a whole. Reads of the lower byte of this register return the contents of this holding register that do not necessarily reflect the current sample rate.

Bit Name	Description
SRG1, SRG0	Sample Rate Granularity. These bits select the LSB weighting of the Bits SR[13:0] (Sample Rate Select). These bits select a fundamental LSB weighting of either 1 Hz, 8/7 Hz, or 10/7 Hz for Bits SR[13:0]. 00 = SR[13:0] LSB weight is 1 Hz. 01 = SR[13:0] LSB weight is 8/7 Hz. 10 = SR[13:0] LSB weight is 10/7 Hz. 11 = Reserved.
SR13 to SR0	Sample Rate Select. Bits SRG[1:0] (Sample Rate Granularity), these bits define the sample rate for both the ADC and DAC codec channels. Permitted settings of SR[13:0] range from 6400 to 16000 when SRG[1:0] = 00, 5600 to 14,000 when SRG[1:0] = 01, and 4480 to 11,200 when SRG[1:0] = 10. The default sample rate is 16,000 Hz.

DAC/ADC LEVEL CONTROL REGISTER

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x46	DAM	0	0	DAL4	DAL3	DAL2	DAL1	DAL0	ADM	0	ADS	ADG20	ADL3	ADL2	ADL1	ADL0	0x8080

This register is forced to its default only when power is first applied to the AD1803.

The states of Bit ADS, Bit ADG20, and Bit ADL3 to Bit ADL0 in this register must not be changed while an ADC calibration is in progress if the analog codec of the AD1803 is in use (see Bit APDN in Register 0x3E and Bit ADCAL in Register 0x5C).

Bit Name	Description
DAM	DAC Mute. 0 = DAC output enabled. 1 = DAC output muted (forced to midscale) (default).
DAL4 to DAL0	DAC Attenuation Level Select. Least significant bit represents −1.5 dB. This attenuation is valid when the AD1803's analog codec is used with the digital codec of the AD1803 (Bit ACSEL in Register 0x5C = 0). 00000 = +12.0 dB gain (default). 11111 = −34.5 dB attenuation.
ADM	ADC Mute. 0 = ADC samples passed. 1 = ADC samples substituted with midscale (0) data (default).
ADS	Analog ADC Input Select. The state of this bit has no effect on ADC behavior unless Bit ACSEL in Register 0x5C is set to 0 (default). This selects the analog codec of the AD1803 to partner with the digital codec of the part. If this bit is used to select the MIC input as the ADC input of the AD1803, Pin 15 must first be assigned to serve as this MIC input rather than its default role as a GPIO pin. This is done by setting Bit GPMIC in Register 0x5E to 1. 0 = Pin 16 (Rx input) selected as AD1803 ADC input source (default). 1 = Pin 15 (MIC input) selected as AD1803 ADC input source (requires GPMIC in Register 0x5E set to 1).
ADG20	AD1803 Analog ADC 20 dB Gain Enable. The state of this bit has no effect on ADC behavior unless Bit ACSEL in Register 0x5C is set to 0 (default). This selects the analog codec to partner with the digital codec. Total ADC gain is the summation due to this bit and Bit ADL3 to Bit ADL0. 0 = 0 dB gain (default). 1 = 20 dB gain.
ADL3 to ADL0	AD1803 ADC Gain Level Select. The state of these bits has no effect on ADC behavior unless Bit ACSEL in Register 0x5C is set to 0 (default). This selects the AD1803's analog codec to partner the AD1803's digital codec. 0000 = 0.0 dB gain (default). 1111 = 22.5 dB gain.

GPIO PIN CONFIGURATION REGISTER

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x4C	0	0	0	0	0	0	0	0	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	0x00FF

This register is forced to its default only when power is first applied to the AD1803.

Bit Name	Description
GC7 to GC2, GC0	General-Purpose I/O Pin Configuration. These bits define the directionality of GPIO pins with corresponding numbers. By default, all GPIO pins serve as inputs, but with weak (~100 µA with a 3.3 V supply, ~140 µA with a 5.0 V supply) pull-up devices internal to the AD1803 enabled. See Register 0x4E to disable these weak pull-up devices. Note that GPIO Pin 1 is always an input and cannot serve as an output. Also, note that bits in this register are ignored if the GPIO pin they control has been assigned to serve an alternate special purpose (see bits in Register by more than 0.3 V). GPIO Pin 1 is sourced by the analog supply (Pins AVDD and AGND). All other GPIO pins are sourced by the digital supply (Pin DVDD and Pin DGND). 0 = GPIO pin serves as an output. 1 = GPIO pin serves as an input (default).
GC1	GPIO Pin 1 is always an input (default=1) and cannot serve as an output. Any writes to this register will be ignored.

GPIO PIN POLARITY/TYPE REGISTER

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x4E	0	0	0	0	0	0	0	0	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0x00FF

This register is forced to its default only when power is first applied to the AD1803.

Bit Name	Description
GP7 to GP0	GPIO Input Polarity/Output Driver Type Select. These bits control GPIO pins with corresponding numbers. The effect they have is dependent on GPIO pin directionality (see Register 0x4C). When a GPIO pin serves as an input, these bits select the logic level necessary to set a sticky status bit which is used to trigger an interrupt (see Registers 0x50 and 0x52). When serving as an input, these bits determine whether a weak pull-up receives a low, the weak pull-up is disabled. If an input is set to active low, and therefore nominally receives a high, the weak pull-up is enabled. Meanwhile, when a GPIO pin serves as an output, these bits determine whether a CMOS or open drain with weak pull-up driver is activated. If a GPIO pin is defined as an input (corresponding GC bit in Register 0x4C is set to 1) 0 = Input is active high, weak pull-up disabled. 1 = Input is active low, weak pull-up enabled (default). If a GPIO pin is defined as an output (corresponding GC bit in Register 0x4C is set to 0). 0 = Output driver is CMOS. 1 = Output driver is open drain with weak pull-up enabled (default).

GPIO STICKY PIN REGISTER

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x50	0	0	0	0	0	0	0	0	GS7	GS6	GS5	GS4	GS3	GS2	GS1	GS0	0x0000

This register is forced to its default only when power is first applied to the AD1803.

Bit Name	Description
GS7 to GS0	GPIO Sticky Control. These bits control GPIO pins with corresponding numbers. They determine whether a read of Register 0x54 returns either the current logic level received on a GPIO pin, or a sticky status bit which indicates if a selected logic level (see Register 0x4E) has been received since this sticky status bit was last cleared. Sticky status bits are cleared by writes to their associated control bits in Register 0x54, and whenever the current GPIO pin received logic level is selected as the Register 0x54 return value. 0 = Reads of Register 0x54 return current state of GPIO pin, sticky status bit cleared (default). 1 = Reads of Register 0x54 return a sticky status bit set by GPIO pin level selected by Register 0x4E.

GPIO PIN WAKE-UP MASK

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x52	0	0	0	0	0	0	0	0	GW7	GW6	GW5	GW4	GW3	GW2	GW1	GW0	0x0000

This register is forced to its default only when power is first applied to the AD1803.

Bit Name	Description
GW7 to GW0	GPIO Wake-Up Mask Control. A GPIO pin triggers an interrupt providing that it is enabled to cause interrupts by the corresponding numbered bit in this register, and it has its associated sticky status bit set. For the associated sticky status bit to be set, the GPIO input must first be enabled to be sticky by the GS bit in Register 0x50, and then the logic level selected by a GP bit in Register 0x4E must be received on the associated GPIO pin. When an interrupt is triggered, Pin 12 is driven high providing Pin 12 is enabled to serve as an interrupt output (see GPWAK bit in Register 0x5E). If the AD1803's serial interface is configured in an AC '97 mode, interrupts are also reflected on Bit 0 of Slot 12 of each frame, even if Pin 12 is not enabled to respond to an interrupt. Also in AC '97 mode, if $\overline{\text{RESET}}$ is asserted when an interrupt is triggered, the SDATA_IN pin is driven from low (default during $\overline{\text{RESET}}$) to high to wake an AC '97 controller. Refer to the AC '97 specification for complete details. Activated GPIO pins can trigger interrupts. The source of the interrupt can be determined by reading Register 0x54. 0 = GPIO pin disabled from causing interrupts (default). 1 = GPIO pin enabled to cause interrupts (providing corresponding GS bit in Register 0x50 = 1).

GPIO PIN STATUS REGISTER

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x54	0	0	0	0	0	0	0	0	GI7	GI6	GI5	GI4	GI3	GI2	GI1	GI0	0x00FF

This register is forced to its default only when power is first applied to the AD1803.

Bit Name	Description
GI7 to GI0	GPIO Status. Each bit corresponds with a GPIO pin of the same number. When a bit is read, it reflects either the current logic level received on a GPIO pin or the state of the sticky status bit that is set if a selected logic level has been received on a GPIO pin since the last time the sticky status bit was cleared (see Register 0x4E, Register 0x50, and Register 0x52). When a bit is written with a 0, the associated sticky status bit is cleared. Note that it is not necessary to write a 1 to a bit after writing a 0 since it is the act of writing a 0 to a bit itself that clears the sticky status bit. When a bit is written with a 1, the associated sticky status bit is unaffected. If the AD1803's serial interface is configured in DSP mode (see Register 0x3C), writes to this register also control the logic level driven out on the GPIO pins provided that a GPIO pin is configured as an output (see Register 0x4C) and is serving as a GPIO pin (see Register 0x5E). If the AD1803's serial interface is configured in an AC '97 mode, GPIO output states are determined by the bits in ac link slot 12 rather than writes to this register (see Bit SPGBP in Register 0x5E and the AC '97 specification for further details).

MISCELLANEOUS MODEM AFE STATUS AND CONTROL REGISTER

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x56	0	0	0	MLNK	0	0	0	0	0	0	0	0	0	LIB2	LIB1	LIB0	0x0000

This register is forced to its default only when power is first applied to the AD1803.

Bit Name	Description
MLNK	AC Link Disable. This bit has no effect on the behavior of the AD1803 unless it is configured as an AC '97 primary device (see Register 0x3C). When this is the case, writing a 1 to this bit puts the AC '97 link interface into a sleep mode by causing the AD1803 to drive the BIT_CLK pin low within one BIT_CLK period after the completion of Slot 2 (the slot in which writes to control registers occur). While in this sleep mode, an AC '97 controller can wake the AD1803 interface either by pulsing the SYNC pin, or by asserting and then deasserting the $\overline{\text{RESET}}$ pin. Refer to the AC '97 specification for complete details. Note that the interface is put to sleep, regardless of interface mode, if the $\overline{\text{RESET}}$ pin is asserted.
LIB2 to LIB0	Loopback Modes. 000 = No loopback. Normal signal pathways engaged (default). 001 = Analog loopback. Analog ADC output to analog DAC input (at analog interface to digital codec). 010 = Local loopback. DAC output to ADC input (at analog pins). 011 = Digital loopback. Digital DAC output to digital ADC input (at digital interface to analog codec). 1xx = No loopback. Normal signal pathways engaged.

CONFIGURATION 1 REGISTER

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x5C	Res[1]	BNK1	BNK0	R34PM	XTAL1	XTAL0	ACSEL	ADCAL	CLKED	CLKEA	Res[1]	Res[1]	Res[1]	Res[1]	Res[1]	Res[1]	0x18C0

[1] Res = reserved bit. To ensure future compatibility, reserved bits should be set to 0 when written and ignored when read.

This register is forced to its default only when power is first applied to the AD1803.

Bit Name	Description
BNK1, BNK0	Register Bank Select. Since the AC '97 specification lacks sufficient vendor specified register space to control all extended features of the AD1803, some control registers must be accessed indirectly using register banks selected by these bits. 00 = Reserved. 01 = Bank 1: AD1803 I/O control registers. 10 = Bank 2: AD1803 codec control registers. 11 = Reserved.
R34PM	$\overline{\text{RESET}}$ Power Mode Select. When this bit is set to 0, the AD1803 is completely powered down whenever the $\overline{\text{RESET}}$ pin is asserted (driven low). This bit overrides the settings of all other power control bits. When this bit is set to 1, various features of the AD1803 remains powered up during $\overline{\text{RESET}}$ as individually enabled by their related control bits (see other bits in this register) 0 = During $\overline{\text{RESET}}$, power down the AD1803. 1 = During $\overline{\text{RESET}}$, allow enabled features to remain powered up (default).
XTAL1, XTAL0	Clock Identification. With the exception of the serial interface, which is always clocked by the BIT_CLK pin, these bits identify the clock source and frequency to be used by all other resources within the AD1803. The default setting of these bits is dependent on the chosen AD1803 serial interface configuration (see Register 0x3C). There are three reasons why it might be desirable to alter from the default setting: If the BIT_CLK is the default clock source, but the BIT_CLK has excessive edge noise that interferes with codec performance, than a crystal or other clean clock source could be taken from the XTALI pin instead. If the BIT_CLK is the default clock source, but the BIT_CLK is stopped during a period of time when AD1803 functionality is still necessary, such as ring validation and wake-up signaling during D3-Cold, then the clock source could be switched to the XTALI pin while the BIT_CLK is suspended. If the XTALI is the default clock source and the default crystal frequency is not the one actually used, the correct crystal frequency must be identified prior to the ADC, DAC, or barrier interface being enabled (see Register 0x3E). Also note that if the AD1803 is the master of BIT_CLK (serial interface in AC '97 primary mode or DSP mode), BIT_CLK cannot be at its proper frequency until the AD1803 is informed what clock frequency it is receiving. Until then, the BIT_CLK frequency is off by the ration of the actual to the default assumed frequency. As a final caution, if the clock frequency is chosen to be 32.768 MHz (setting 01 of these bits), and the AD1803 is chosen to be an AC '97 primary device, the AD1803 is incapable of producing the AC '97 specified 12.288 MHz BIT_CLK because there is no integer divisor between these frequencies. In this situation, the AD1803 violates the AC '97 specification and outputs a 16.384 MHz BIT_CLK. 00 = 12.288 MHz from BIT_CLK (default if in an AC '97 secondary mode). 01 = 32.768 MHz from XTALI. 10 = 24.576 MHz from XTALI (default if in either AC '97 primary mode or DSP mode). 11 = 12.288 MHz from XTALI.
ACSEL	Analog Codec Select. This bit selects the analog codec that is used in conjunction with the digital codec of the AD1803. 0 = AD1803 analog codec selected (default). 1 = Reserved.
ADCAL	ADC Calibration/Recalibration. Writing a 1 to this bit initiates a dc offset calibration of the codec's ADC channel, which requires approximately 104 sample periods (defined by Register 0x40). ADC calibration is automatic each time the analog ADC of the AD1803 is enabled. When this bit is read, a 1 is returned if calibration is in progress and a 0 is returned when calibration is completed or not in progress. During calibration, the ADC returns midscale (zero) samples. During calibration, codec sample rate, ADC source, and ADC gain must not be changed.
CLKED	CLK_OUT Enable While $\overline{\text{RESET}}$ Is Deasserted (Driven High). This bit controls the operation of the CLK_OUT pin while the $\overline{\text{RESET}}$ pin is deasserted. See Bit CLKEA for CLK_OUT operation while $\overline{\text{RESET}}$ is asserted. Each time $\overline{\text{RESET}}$ is deasserted (driven from low to high), this bit is automatically set to 1 to ensure that a clock is always available to hardware outside the AD1803 after a $\overline{\text{RESET}}$. If this clock is not needed, this bit should be set to 0 by software after each $\overline{\text{RESET}}$ for optimal power savings. 0 = When $\overline{\text{RESET}}$ is deasserted, CLK_OUT is driven low. 1 = When $\overline{\text{RESET}}$ is deasserted, CLK_OUT reflects clock on XTALI (default after deassertion of $\overline{\text{RESET}}$).

Bit Name	Description
CLKEA	CLK_OUT Enable While $\overline{\text{RESET}}$ Is Asserted (Driven Low). This bit controls the operation of the CLK_OUT pin while the $\overline{\text{RESET}}$ pin is asserted. See Bit CLKED for CLK_OUT operation while $\overline{\text{RESET}}$ is deasserted. If Bit R34PM is set to 0, this bit is ignored, and CLK_OUT is driven low while $\overline{\text{RESET}}$ is asserted. 0 = When $\overline{\text{RESET}}$ is asserted, CLK_OUT is driven low. 1 = When $\overline{\text{RESET}}$ is asserted, CLK_OUT reflects clock received on XTALI (providing R34PM set to 1) (default).

CONFIGURATION 2 REGISTER

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x5E	GPBAR	GPWAK	GPMON	GPMIC	SPCHN	SPGBP	SPDSS	SPISO	SPDL1	SPDL0	Res[1]	Res[1]	Res[1]	Res[1]	Res[1]	Res[1]	0x0018

[1] Res = reserved bit. To ensure future compatibility, reserved bits should be set to 0 when written and ignored when read.

This register is forced to its default only when power is first applied to the AD1803.

Bit Name	Description
GPBAR	GPIO Interface Select. 0 = Use AD1803 Pin 24, Pin 23, and Pin 22 as G[5], G[6], and G[7] respectively (default). 1 = Reserved.
GPWAK	G[3]/Wake Interrupt Signal Select. 0 = Use AD1803 Pin 12 as GPIO[3] (default). 1 = Use AD1803 Pin 12 as Wake Interrupt (see Register 0x52).
GPMON	GP[4]/Monitor Output Select. 0 = Use AD1803 Pin 11 as GPIO[4] (default). 1 = Use AD1803 Pin 11 as Σ-Δ monitor output (see Register 0x60 Bank 2).
GPMIC	GP[1]/MIC Input Select. 0 = Use AD1803 Pin 15 as G[1] (default). 1 = Use AD1803 Pin 15 as analog MIC input (see Bit ADS in Register 0x46).
SPCHN	Serial Port Chaining Mode Enabled. This bit is ignored unless the AD1803 is in an AC '97 serial interface mode (see Register 0x3C). This bit can be used to chain multiple AC '97 devices to a single 4-wire AC '97 link. Consult Analog Devices, Inc. for further details. 0 = ADI chaining mode disabled (default). 1 = ADI chaining mode enabled.
SPGBP	Serial Port GPIO Bit Placement Select. This bit is ignored unless the AD1803 is configured in an AC '97 serial interface mode (see Register 0x3C). Writes to this bit take effect on the current serial interface frame. 0 = State of AD1803 G[7] through G[0]0 reflected on Bits [1:4] of Slot 12 (default). 1 = State of AD1803 G[7] through G[0] reflected on Bits [19:12] of Slot 12
SPDSS	Serial Port Data Slot Size Select. This bit is ignored unless the AD1803 is configured in an AC '97 serial interface mode (see Register 0x3C). When set to 1, the four LSBs of all 20-bit data slots are dropped, allowing a simpler connection with a DSP. Writes to this bit take effect during the current frame, but can distort the current frames slot alignment. As a result, when the state of this bit is changed, all data slots sent to the AD1803 should be set to zero and all data slots received from the part should be ignored. 0 = Data slots are 20 bits (default). 1 = Data slots are 16 bits.
SPISO	Serial Port Isolate. When this bit is set to 1, the AD1803 serial interface is isolated from the outside system whenever $\overline{\text{RESET}}$ is asserted. This is achieved by ignoring the signals received on serial interface input pins and driving serial interface output pins weakly (less than 200 µA), rather than with nominal output drive strengths. This bit should be set to 1 prior to a controller on the other side of the part's serial interface losing power if the AD1803 continues to receive power. It can also be set to 1 to save power if the part's serial interface input pins continue to make transitions while $\overline{\text{RESET}}$ is asserted.
SPDL1, SPDL0	Serial Port Data Slot Location Select. These bits are ignored unless the AD1803 is configured in an AC '97 serial interface mode (see Register 0x3C). Writes to these bits take effect during the current frame, but data sent during the current frame can be distorted or dropped. For reliable operation, these bits should not be changed while the codec is enabled. 00 = AD1803 uses Slot 5 to send and receive sample data (default). 01 = AD1803 uses Slot 10 to send and receive sample data. 10 = AD1803 uses Slot 11 to send and receive sample data. 11 = Reserved.

BANK 1—GPIO INITIAL STATES REGISTER

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x60	0	0	0	0	0	0	0	0	GPIV7	GPIV6	GPIV5	GPIV4	GPIV3	GPIV2	GPIV1	GPIV0	0x0000

This register is forced to its default only when power is first applied to the AD1803.

Bit Name	Description
GPIV7 to GPIV0	GPIO Pin Initial Value. When $\overline{\text{RESET}}$ is deasserted for the first time after power is applied to the AD1803, the states of all GPIO pins are sampled and stored in this register. Writes to this register and subsequent logic level changes on GPIO pins have no effect on the values reported by reads of this register. While the sampled states of GPIO Pin 2 and Pin 3 are used by the AD1803 to determine serial interface mode (see Register 0x3C), all remaining GPIO pins are available for use, if beneficial, as identification bits to host software or hardware. Immediately after power is first applied to the AD1803, all GPIO pins by default serve as inputs, but with weak pull-up devices internal to the enabled AD1803. Since these pull-up devices have an effective resistance of about 30 kΩ, external resistors of less than 8 kΩ tied to digital ground (DGND pin) must be used for logic lows to be sampled.

BANK 1—CLOCK PAD CONTROL REGISTER

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x64	0	0	0	0	0	0	0	0	Res[1]	Res[1]	Res[1]	Res[1]	XTLP	COS2	COS1	COS0	0x0077

[1] Res = reserved bit. To ensure future compatibility, reserved bits should be set to 0 when written and ignored when read.

This register is forced to its default only when power is first applied to the AD1803.

Bit Name	Description
XTLP	Crystal Oscillator Low Power Mode Enable. Depending on board design and crystal used, this bit can be set to 1 to engage a crystal oscillator low power mode, which saves up to 0.7 mA. This mode reduces the amount of energy that an AD1803 provides to keep a crystal oscillating, but otherwise has no effect on AD1803 behavior. If a clock is driven onto the XTALI pin from an external source, rather than generated by a crystal connected between the XTALI pin and XTALO pin, the optimal setting for this bit is 1, although with only a slight power benefit. 0 = Normal power mode (default). 1 = Low power mode.
COS2 to COS0	CLK_OUT Pin Drive Strength Select. This bit can be used to reduce EM emissions, or three-state the CLK_OUT pin. 000 = 0% of full drive strength (pad three-stated). 001 = 13% of full drive strength. 010 = 25% of full drive strength. 011 = 38% of full drive strength. 100 = 63% of full drive strength. 101 = 75% of full drive strength. 110 = 88% of full drive strength. 111 = 100% of full drive strength (default).

BANK 2—MONITOR OUTPUT CONTROL REGISTER

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D2	D2	D1	D0	Default
0x62	MMD1	MMD0	MDM	MDL4	MDL3	MDL2	MDL1	MDL0	Res	Res	MAM	MAL4	MAL3	MAL2	MAL1	MAL0	0x4000

This register is forced to its default only when power is first applied to the AD1803.

Bit Name	Description
MMD1, MMD0	Monitor Output Mode. The monitor output of the AD1803 provides a programmable mix of the ADC and DAC signals passing through the codec of the part. Pin 11 serves as the monitor output, providing Bit GPMON in Register 0x5E is set to 1. Otherwise, Pin 11 serves its default role as a GPIO pin. When the monitor output is enabled (powered up) using Bits MDM[1:0], the monitor output is in the form of digital Σ-Δ modulator bit stream with a maximum edge rate (carrier) of 512 kHz. One of two different Σ-Δ modulator types can be activated: Either a first order that generates 6 dB more signal swing than the other choice but has more inband noise and idle tones or a third order that has half the signal swing but significantly superior inband noise and negligible idle tones. To extract the signal from the Σ-Δ modulator noise, it is recommended that the monitor output be filtered by connecting Pin 11 to a 1 kΩ resistor in series with a parallel 4.7 kΩ resistor and 100 nF capacitor combination which is then tied to digital ground (DVDD pin). This filter, with the output taken from the middle node, has a 1500 Hz corner to filter out high frequency Σ-Δ noise. It generates an approximate 1 V p-p output when using a 5 V digital supply with the monitor output configured as a first order (MMD1 and MMD0 set to 10) if the filter output load is greater than or equal to 20 kΩ. Other filter networks can also be used, perhaps to save power or increase effective output signal swing, but for long term reliability, care must be taken to ensure that the monitor output never sources more than 5 mA. The recommended filter dissipates approximately 1 mA. 00 = Reserved. 01 = Monitor output powered down and driven low (default). 10 = Monitor enabled, first-order Σ-Δ output, signal swing: 0% to 100% ones (best signal amplitude). 11 = Monitor enabled, third-order Σ-Δ output, signal swing: 25% to 75% ones (best signal SNR post filter).
MDM	Monitor Output DAC Mix Mute. If both ADC and DAC mix are muted, the monitor output should be powered down (MDM[1:0] set to 10) to achieve a quieter mute. 0 = DAC mix level determined by bits MDL4 to MDL0 (default). 1 = DAC mix is muted.
MDL4 to MDL0	Monitor Output DAC Mix Level. Unless muted by the MDM bit in this register, these bits control the amount of DAC signal that is mixed into the monitor output. Representation is two's complement with an LSB weighting of 3 dB and a permissible range of +45 dB to −18 dB. If the analog codec of the AD1803 is in use (ACSEL set to 0), the DAC signal mixed is taken before this attenuation is applied. In either case, the DAC signal mixed is always taken before the mute bit DAM in Register 0x46 is applied. 01111 = +45 dB. 00000 = 0 dB (default). 11010 = −18 dB.
MAM	Monitor Output ADC Mix Mute. If both ADC and DAC mix are muted, the monitor output should probably be powered down (MAM[1:0] set to 10) to achieve a quieter mute. 0 = ADC mix level determined by bits MAL[4:0] (default). 1 = ADC mix is muted.
MAL4 to MAL0	Monitor Output ADC Mix Level. Unless muted by the MAM bit in this register, these bits control the amount of ADC signal that is mixed into the monitor output. Representation is two's complement with an LSB weighting of 3 dB and a permissible range of +45 dB to −18 dB. The ADC signal mixed is always taken after the gain specified by Bit DAL4 to Bit DAL0 in Register 0x46 is applied, but before the mute bit ADM in Register 0x46 is applied. 01111 = +45 dB. 00000 = 0 dB (default). 11010 = −18 dB.

VERSION ID REGISTER

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x7A	0	0	0	0	0	0	0	0	VER7	VER6	VER5	VER4	VER3	VER2	VER1	VER0	0x0002

Bit Name	Description
VER7 to VER0	AD1803 Version. Writes to this register have no effect. The latest version of the AD1803 is 0x0002.

VENDOR ID1 REGISTER

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x7C	0	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0x4144

Writes to Register 0x7C and Register 0x7E have no effect. When read, Address 0x7C and Address 0x7E return 0x4144 and 0x5380, respectively, which, taken together, map to ADS in ASCII followed by Address 0x80. ADS is registered in the AC '97 specification to identify Analog Devices as the vendor, and the final byte of Address 0x80 is used to identify the AD1803 (vendor selected value).

VENDOR ID2 REGISTER

Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x7E	0	1	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0x5380

APPLICATIONS

APPLICATION CIRCUITS

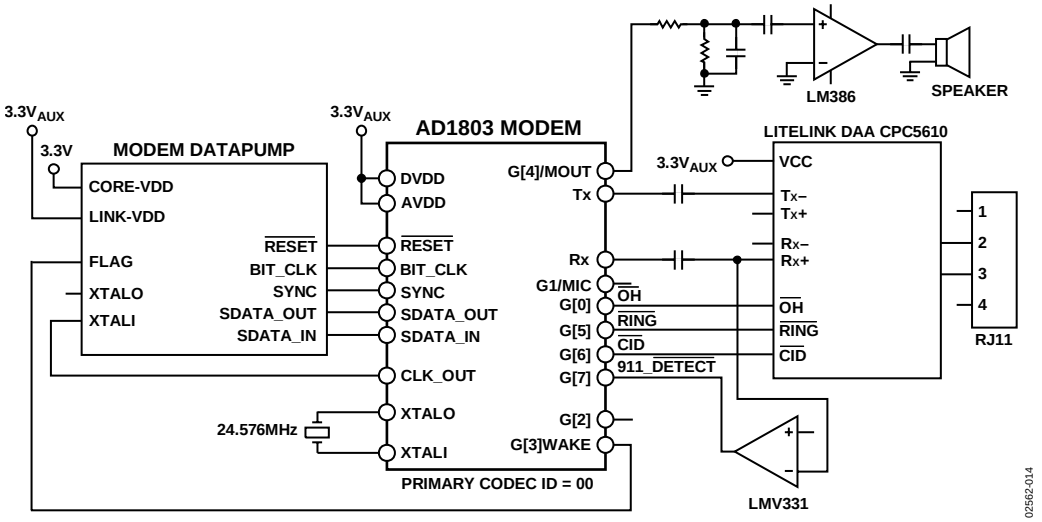

Figure 14. PC/Embedded Modem

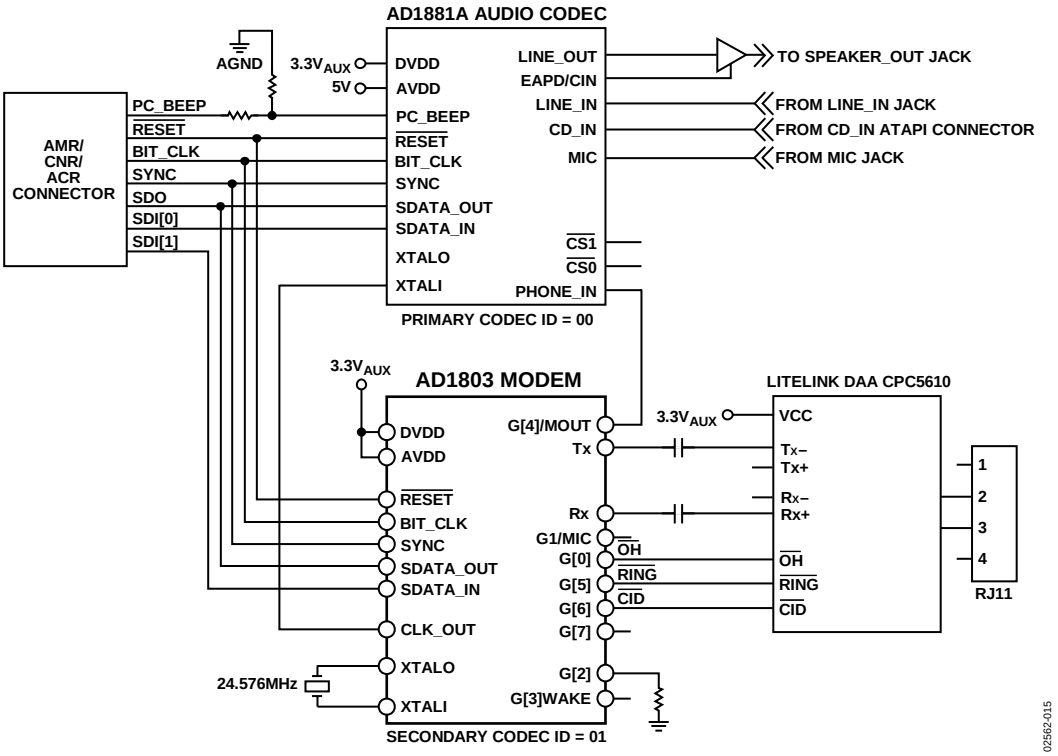

Figure 15. Audio Modem Riser

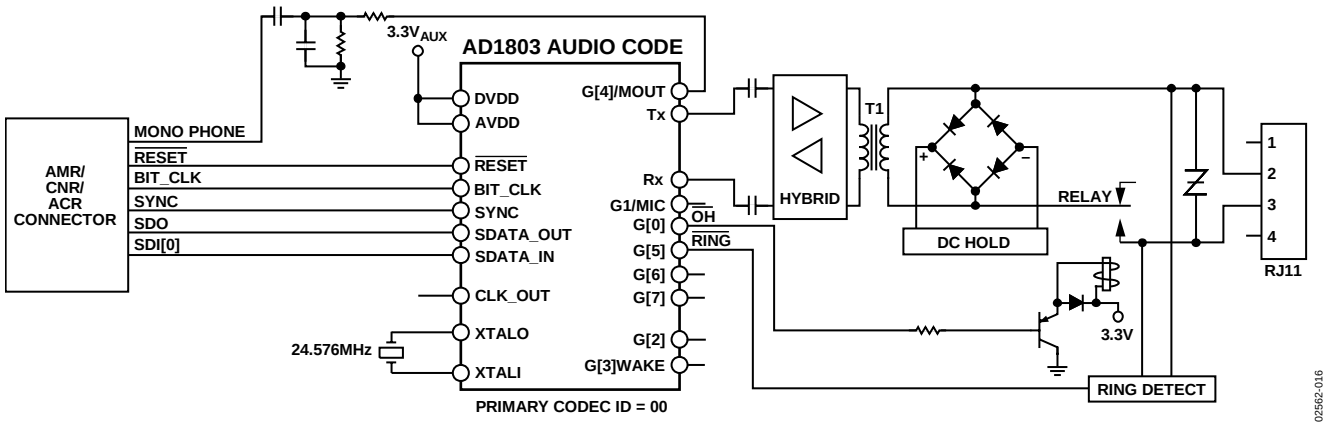

Figure 16. Modem Riser with Discrete DAA

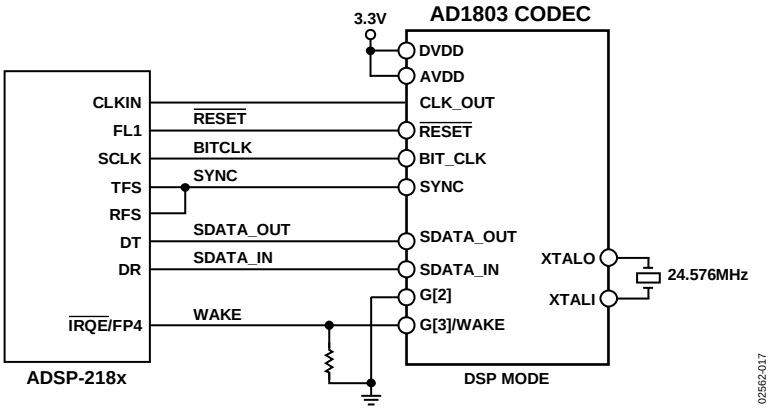

Figure 17. Interfacing AD1803 to ADSP-218x DSP

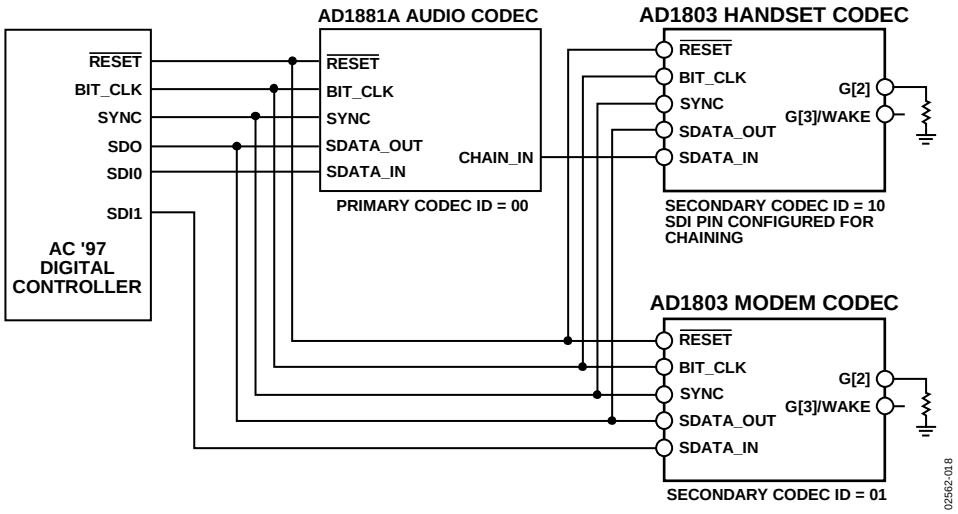

Figure 18. Codec Chaining Allows Several Analog Devices AC '97 Codecs to be Connected to One AC Link Controller Port

TYPICAL INITIALIZATION SEQUENCE IMMEDIATELY AFTER FIRST $\overline{\text{RESET}}$

Step 1: Write to Register 0x5C (Configuration 1 Register).

Bits[14:13]—BNK1, BNK0 (register bank select). These bits should be set to 01 in preparation for Step 2.

Bit[12]—R34PM ($\overline{\text{RESET}}$ power mode select). If it is desired to have the AD1803 drive a clock out on the CLK_OUT pin while $\overline{\text{RESET}}$ is asserted, this bit must be changed from its default setting of 0 to 1, otherwise, the AD1803 is completely powered down whenever $\overline{\text{RESET}}$ is asserted ($\overline{\text{RESET}}$ pin driven low).

Bits[11:10]—XTAL1, XTAL0 (clock identification): If the clock presented on pin XTALI is not 24.576 MHz, the default setting of these bits must be changed to identify the actual XTALI frequency provided.

Bit[9]—ACSEL (analog codec select). While this bit can be updated at any time, and even while the codec is enabled, it is recommended to set this bit prior to enabling the codec. This bit selects an analog codec used in conjunction with the digital codec within the AD1803. When set to 0, which is the default, the analog codec within the AD1803 is used.

Bit[8]—ADCAL (ADC calibration recalibration). Until the codec is enabled, writes to this bit have little purpose.

Bit[7]—CLKED (CLK_OUT enable while $\overline{\text{RESET}}$ is deasserted). Immediately after $\overline{\text{RESET}}$ is deasserted ($\overline{\text{RESET}}$ pin driven high) this bit is always $\overline{\text{RESET}}$ to a 1. This enables the CLK_OUT pin to provide a buffered version of the clock received on the XTALI pin following every deassertion of $\overline{\text{RESET}}$. Therefore, to stop this clock low and save power, this bit must be set to 0 after every deassertion of $\overline{\text{RESET}}$. Stopping CLK_OUT saves about 1.5 mA plus any addition current saved by not driving the board load that might be present. Note that CLK_OUT can also be permanently three-stated using bits COS2 to COS0 in Register 0x64 Bank 1.

Bit[6]—CLKEA (CLK_OUT enable while $\overline{\text{RESET}}$ is asserted). This bit must be changed from its default of 0 to 1 if it is desired to have the CLK_OUT pin provide a clock output while the AD1803 is $\overline{\text{RESET}}$ ($\overline{\text{RESET}}$ pin driven low). Note that Bit R34PM can override the behavior selected by the state of this bit.

Step 2: Write to Register 0x64 (Bank 1—Clock Pad Control Register).

Bit[3]—XTLP (crystal oscillator low power mode enable). Depending on board design and crystal used, this bit can be set to 1 to engage a crystal oscillator low power mode, which saves up to 0.7 mA. This mode reduces the amount of energy that an AD1803 provides to keep a crystal oscillating, but otherwise has no effect on AD1803 behavior. If a clock is driven onto the XTALI pin from an external source rather than generated by a crystal connected between the XTALI and XTALO pins, the optimal setting for this bit is 1, although with only a slight power benefit.

Bits[2:0]—COS2 to COS0 (CLK_OUT pin drive strength select). These bits should be set to select the optimal output driver strength for the CLK_OUT pin to soften edges and reduce EMI emissions.

Step 3: Write to Register 0x5E (Configuration 2 Register).

Bit[14]—GPWAK (G[3]/Wake interrupt signal select). If an interrupt/wake output signal is desired, this bit must be changed from its default setting of 0 to 1. This enables Pin 12 to serve this role rather than a default role as a general-purpose I/O pin. When serving as an interrupt/wake flag, Pin 12 is driven high whenever a qualifying event has occurred.

Bit[13]—GPMON (G[4]/Monitor output select): If the monitor output feature is used, this bit must be changed from its default setting of 0 to 1. This enables Pin 11 to serve this role rather than a default role as a general-purpose I/O pin. When serving as a monitor output, Pin 11 outputs a Σ-Δ bit stream consisting of a selectable mix of the signals present on the ADC and DAC channels.

Bit[12]—GPMIC (GPI[1]/MIC input select). If a second selectable ADC input source is desired, the setting of this bit must be changed from its default of 0 to 1. This switches the role of Pin 15 from a general-purpose input flag to an analog MIC input.

Bit[11], Bit[10], Bit[9], Bit[7], and Bit[6]—SPCHN, SPGBP, SPDSS, SPDL1, and SPDL0. These bits affect the operation of the AD1803 only if in an AC '97 serial interface mode.

Bit[8]—SPISO (serial port isolate). See the Typical Codec Power-Down Sequence section for further details.

Step 4: Read Register 0x60 (Bank 1—GPIO Initial States Register).

As $\overline{\text{RESET}}$ is deasserted ($\overline{\text{RESET}}$ pin driven high), the first time after power is applied to the AD1803, the states of all general-purpose I/O pins are sampled and stored in this register. While the sampled states of GPIO Pin 2 and Pin 3 are used by the AD1803 to determine serial interface mode, all remaining GPIO pins are available for use, if beneficial, as identification bits to a host software.

Step 5: Write to Register 0x4C through Register 0x54 (GPIO control registers).

These registers determine the behavior of the GPIO pins of the AD1803. After power is first applied to the AD1803, all GPIO pins default as inputs, but with weak (~100 µA) pull-up devices within the part enabled to pull any floated GPIO pins high. As needed, these pins can be reconfigured to serve as interrupt sources, active high or low, sticky or unsticky, or general-purpose outputs with open-drain or CMOS drivers. The weak pull-up device can also be disabled to save power. The settings of these registers, like most registers within the AD1803, are unaffected by a $\overline{\text{RESET}}$ and are set to their defaults only when power is first applied to the AD1803. The most practical order is 0x4E, 0x4C, 0x50, 0x54, and finally 0x52.

Step 6: Write to Register 0x40 (Line DAC/ADC Sample Rate Control Register) and Register 0x46 (DAC/ADC Level Control Register).

These registers determine the codec sample rate and channel attenuation levels. While these register can be updated at any time, including while the codec is enabled, establishing desired settings prior to enabling the codec is recommended.

TYPICAL CODEC POWER-UP SEQUENCE

Step 7: Write to Register 0x3E (Extended Status and Control Register).

Bit[11]—DPDN (DAC power-down). This bit must be set to 0 for the DAC codec channel of the AD1803 to be enabled. While this bit is set to 1 (default), all DAC resources within the part are powered down and all data words sent to the AD1803 over the serial interface are ignored. When this bit is set to 0, the digital DAC resources within the part are powered up. The analog DAC resources within the part are powered up only if the voltage reference of the AD1803 is powered up (Bit VPDN in this register is set to 0), and the analog codec of the AD1803 is selected as the partner to the digital codec of the part (Bit ACSEL in register 0x5C is set to 0).

Bit[10]—APDN (ADC power-down): This bit should be set to 0 for the ADC codec channel of the part to be enabled. While this bit is set to 1 (default), all ADC resources within the AD1803 are powered down, and all data words sent out of the part over the serial interface are set to midscale (zero). When this bit is set to 0, the digital ADC resources within the AD1803 are powered up. The analog ADC resources within the part are powered up only if the voltage reference of the AD1803 is powered up (Bit VPDN in this register is set to 0), and the analog codec of the AD1803 is selected as the partner to the digital codec of the part (Bit ACSEL in Register 0x5C is set to 0).

Each time the analog codec of the AD1803 is powered up, an ADC calibration is automatically initiated. This calibration requires approximately 104 sample periods (defined by Register 0x40), but can't be started until after the voltage reference of the part is powered up (by setting Bit VPDN to 0). The voltage reference requires about 48 ms to start up. Bit VSTA in this register can be polled first to determine if the voltage reference is powered up, and then Bit ADCAL in register 0x5C can be polled to determine if calibration is completed. During calibration, the codec sample rate (Register 0x40) and ADC source and gain levels (Bit ADS, Bit ADG20, and Bit ADL[3:0] in Register 0x46) must not be changed.

Bit[9]—VPDN (voltage reference power-down). If the analog codec of the AD1803 is used, this bit must be set to 0 to power up the part's voltage reference. Until the voltage reference is powered up, the analog codec channels of the AD1803 ignore the setting of Bit APDN and Bit DPDN and remain powered down. Once this bit is set to 0, approximately 48 ms are necessary to power up the voltage reference. Bit VSTA in this register can be polled to monitor the status of the voltage reference.

Bit[8]—GPDN (GPIO power-down). Contrary to this bit's name, its setting has no effect on the operation of the AD1803 when configured in DSP mode. When the AD1803 is configured in an AC '97 mode, this bit must be set to 0 for Slot 12 to access GPIO pins.

Bit[3]—DSTA (DAC status). This bit exists solely for AC '97 compatibility. Its purpose is to provide a handshake for DAC power-up/power-down status changes initiated by writes to Bit DPDN. However, because the AD1803 responds to a write of Bit DPDN prior to it being possible to read this bit in a following serial interface frame, there is no reason to poll this status bit.

Bit[2]—ASTA (ADC status). This bit exists solely for AC '97 compatibility. Its purpose is to provide a handshake for ADC power-up/power-down status changes initiated by writes to Bit APDN. Because the AD1803 responds to a write of Bit APDN prior to it being possible to read this bit in a following serial interface frame, there is no reason to poll this status bit.

Bit[1]—VSTA (voltage reference status). This bit can be polled to monitor the status of the voltage reference. When read as a 0, the voltage reference is either powered down or in the process of powering up. When read as a 1, the voltage reference is either powered up or in the process of powering down. Approximately 48 ms after VPDN is set to a 0, this bit transitions from a 0 to a 1 indicating that the voltage reference is powered up.

Bit[0]—GSTA (GPIO status). This bit exists solely for AC '97 compatibility. Its purpose is to provide a handshake for power-up/power-down status changes initiated by writes to Bit GPDN. Because the AD1803 responds to a write of Bit GPDN prior to it being possible to read this bit in a following serial interface frame, there is no reason to poll this status bit.

Step 8: Write to Register 0x5C (Configuration 1 Register).

The purpose of this write is to change the register bank selection in preparation for Step 9. The value written to Register 0x5C at this time should be identical to the value from Step 1, except with Bits[14:13] (BNK1, BNK0) set to 10.

Step 9: Write to Register 0x62 Bank 2 (Monitor Output Control Register).

Writes to this register have no purpose unless a pin has been assigned to serve as a monitor output (see Step 3 in the Typical Initialization Sequence Immediately After First section). This register can be written to power up and power down the monitor channel, select the mix of ADC and DAC channels delivered to the monitor output, and select the order of the Σ-Δ monitor output bit stream.

TYPICAL CODEC POWER-DOWN SEQUENCE

There are two ways to power down the codec. The first way is to simply assert RESET (drive RESET pin low). This clears register 0x3E to its initial power-up default, powering down the ADC, DAC, and voltage reference of the AD1803. A second method is outlined below.

Step 1: Write to Register 0x3E (Extended Status and Control Register).

Bit[11]—DPDN (DAC power-down). This bit must be set to 1 to power down the DAC channel of the AD18103.

Bit[10]—APDN (ADC power-down). This bit must be set to 1 to power down the ADC channel of the AD18103.

Bit[9]—VPDN (voltage reference power-down). This bit can be set to 1 to power down the voltage reference of the AD1803 and save approximately 200 μA, but it can be desirable to leave the voltage reference powered up. Leaving it powered up saves about 48 ms from a future codec power-up sequence, and avoids potential clicks caused by the DAC output tracking the voltage reference as it falls to 0 volts when powered down, and rises to ~1.25 V when powered back up.

Bit[8]—GPDN (GPIO power-down). This bit can be set to any value because it has no effect on AD1803 operation when in DSP mode.

Bit[1]—VSTA (voltage reference status). This bit can be polled to determine the status of the part's voltage reference. When read as a 0, the voltage reference is either powered down or in the process of powering up. When read as a 1, the voltage reference is either powered up or in the process of powering down. Within 0.8 ms after VPDN is set to 0, this bit transitions from 1 to 0, indicating that the voltage reference is completely powered down. If a clock is driven onto the XTALI pin, and it is desired to stop this clock for additional system power savings, this clock must not be stopped until after this bit falls to a 0.

TYPICAL CHIP POWER-DOWN SEQUENCE

Once the codec is powered down to the level desired, no additional power can be saved unless the AD1803 receives a RESET, ignoring power potentially saved by stopping the clock on the CLK_OUT pin or disabling GPIO pin drivers, which have resistive loads. When a RESET is received by the AD1803, the serial interface automatically powers down, leaving the internal clock generation and distribution circuitry of the part as the final significant power consumer to be addressed. If Bit R34PM in Register 0x5C is set to a 0 before RESET is asserted, this clock circuitry is powered down as well when RESET is asserted, with the consequence that wake-up on ring and ability to source a clock on the CLK_OUT pin during RESET is lost. This leaves silicon leakage current, typically less than 100 μA, plus inadvertent serial interface loading as the final power drains. Inadvertent serial interface loading can be due to either the AD1803 receiving intermediate or switching logic levels on its BIT_CLK, SYNC, or SDATA_OUT input pins, or the presence of resistive loads to a potential other than DGND (AD1803 digital ground) on the SDATA_IN or BIT_CLK output pins. This inadvertent serial interface loading can be eliminated if Bit SPISO (Serial Port Isolate) in Register 0x5E is set to 1 before the part receives a RESETwith the consequence that output BIT_CLK is driven low weakly (<200 μA drive current) whenever RESET is asserted.

OUTLINE DIMENSIONS

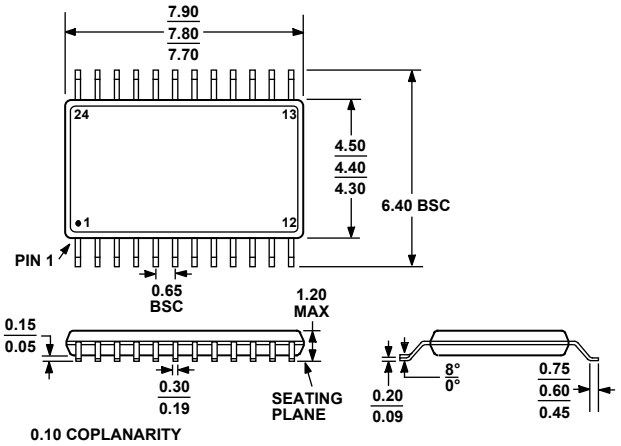

Figure 19. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1803JRU-REEL	0°C to +70°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD1803JRUZ-REEL[1]	0°C to +70°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24

[1] Z = Pb-free part.

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