Am29DL800B

Data Sheet *(Retired Product)*

This product has been retired and is not recommended for designs. For new and current designs please contact your Spansion representative for alternates. Availability of this document is retained for reference and historical purposes only.

The following document contains information on Spansion memory products.

Continuity of Specifications

There is no change to this data sheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal data sheet improvement and are noted in the document revision summary.

For More Information

Please contact your local sales office for additional information about Spansion memory solutions.

Publication Number 21519 **Revision** C **Amendment** 5 **Issue Date** March 17, 2009

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DATA SHEET

Am29DL800B

8 Megabit (1 M x 8-Bit/512 K x 16-Bit) CMOS 3.0 Volt-only, Simultaneous Operation Flash Memory

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DISTINCTIVE CHARACTERISTICS

- **Simultaneous Read/Write operations**
  - Host system can program or erase in one bank, then immediately and simultaneously read from the other bank
  - Zero latency between read and write operations
  - Read-while-erase
  - Read-while-program
- **Single power supply operation**
  - Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
- **Manufactured on 0.35 µm process technology**
  - Compatible with 0.5 µm Am29DL800 device
- **High performance**
  - Access times as fast as 70 ns
- **Low current consumption (typical values at 5 MHz)**
  - 7 mA active read current
  - 21 mA active read-while-program or read-while-erase current
  - 17 mA active program-while-erase-suspended current
  - 200 nA in standby mode
  - 200 nA in automatic sleep mode
  - Standard t_{CE} chip enable access time applies to transition from automatic sleep mode to active mode
- **Flexible sector architecture**
  - Two 16 Kword, two 8 Kword, four 4 Kword, and fourteen 32 Kword sectors in word mode
  - Two 32 Kbyte, two 16 Kbyte, four 8 Kbyte, and fourteen 64 Kbyte sectors in byte mode
  - Any combination of sectors can be erased
  - Supports full chip erase
- **Unlock Bypass Program Command**
  - Reduces overall programming time when issuing multiple program command sequences
- **Sector protection**
  - Hardware method of locking a sector to prevent any program or erase operation within that sector
  - Sectors can be locked in-system or via programming equipment
  - Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - Embedded Erase algorithm automatically pre-programs and erases sectors or entire chip
  - Embedded Program algorithm automatically programs and verifies data at specified address
- **Minimum 1,000,000 program/erase cycles guaranteed per sector**
- **Package options**
  - 44-pin SO
  - 48-pin TSOP
  - 48-ball FBGA
- **Compatible with JEDEC standards**
  - Pinout and software compatible with single-power-supply flash standard
  - Superior inadvertent write protection
- **Data# Polling and Toggle Bits**
  - Provides a software method of detecting program or erase cycle completion
- **Ready/Busy# output (RY/BY#)**
  - Hardware method for detecting program or erase cycle completion
- **Erase Suspend/Erase Resume**
  - Suspends or resumes erasing sectors to allow reading and programming in other sectors
  - No need to suspend if sector is in the other bank
- **Hardware reset pin (RESET#)**
  - Hardware method of resetting the device to reading array data

Publication# **21519** Rev: **C** Amendment: **5**
Issue Date: **March 17, 2009**

GENERAL DESCRIPTION

The Am29DL800B is an 8 Mbit, 3.0 volt-only flash memory device, organized as 524,288 words or 1,048,576 bytes. The device is offered in 44-pin SO, 48-pin TSOP, and 48-ball FBGA packages. The word-wide (x16) data appears on DQ0–DQ15; the byte-wide (x8) data appears on DQ0–DQ7. This device requires only a single 3.0 volt V_{CC} supply to perform read, program, and erase operations. A standard EPROM programmer can also be used to program and erase the device.

This device is manufactured using AMD's 0.35 µm process technology, and offers all the features and benefits of the Am29DL800, which was manufactured using a 0.5 µm technology.

The standard device offers access times of 70, 90, and 120 ns, allowing high-speed microprocessors to operate without wait states. Standard control pins—chip enable (CE#), write enable (WE#), and output enable (OE#)—control read and write operations, and avoid bus contention issues.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

Simultaneous Read/Write Operations with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into two banks. Bank 1 contains eight boot/parameter sectors, and Bank 2 consists of fourteen larger, code sectors of uniform size. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from the other bank, with **zero latency**. This releases the system from waiting for the completion of program or erase operations.

Am29DL800B Features

The device offers complete compatibility with the **JEDEC single-power-supply Flash command set standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low VCC detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector within that bank that is not selected for erasure. True background erase can thus be achieved. There is no need to suspend the erase operation if the read data is in the other bank.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device to reading array data, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability, and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed one byte or word at a time using hot electron injection.

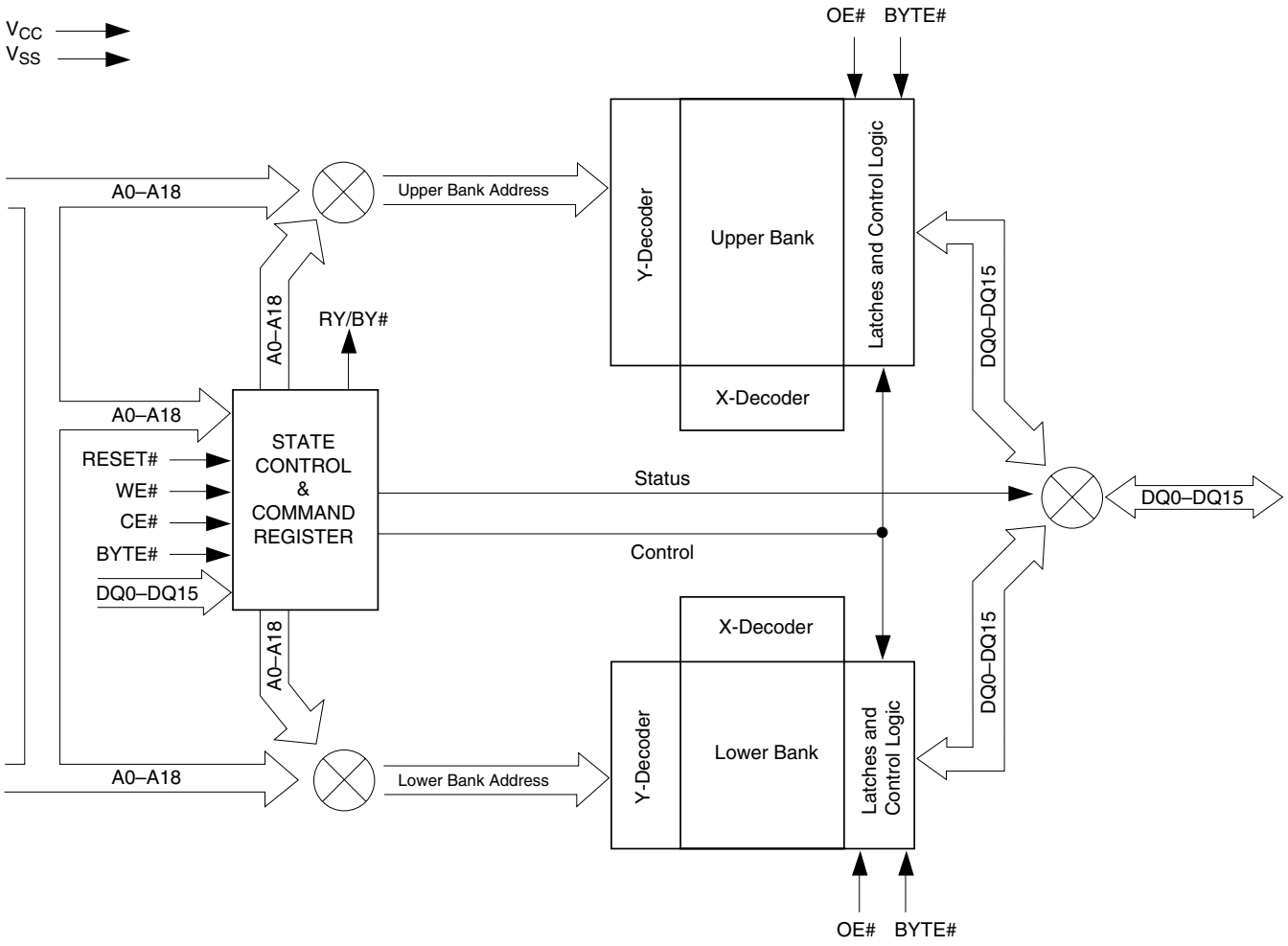
TABLE OF CONTENTS

PRODUCT SELECTOR GUIDE

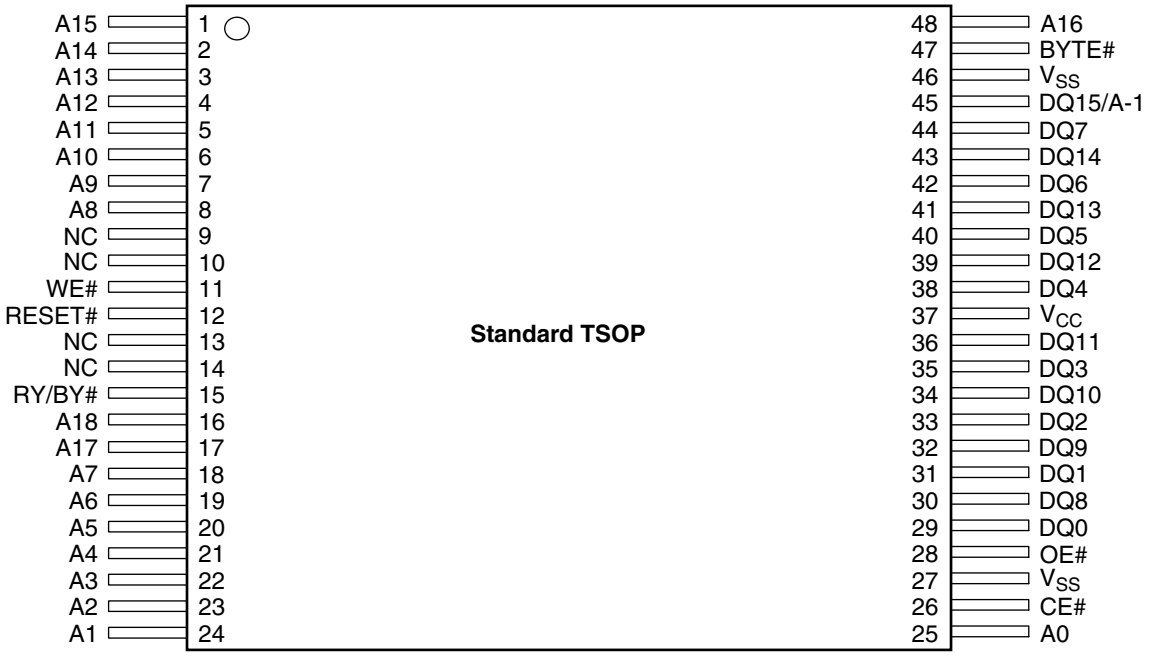
Family Part Number		Am29DL800B		
Speed Option	Full Voltage Range: V_{CC} = 2.7 – 3.6 V	**70**	**90**	**120**
Max Access Time (ns)		70	90	120
CE# Access (ns)		70	90	120
OE# Access (ns)		30	35	50

Note: *See "AC Characteristics" for full specifications.*

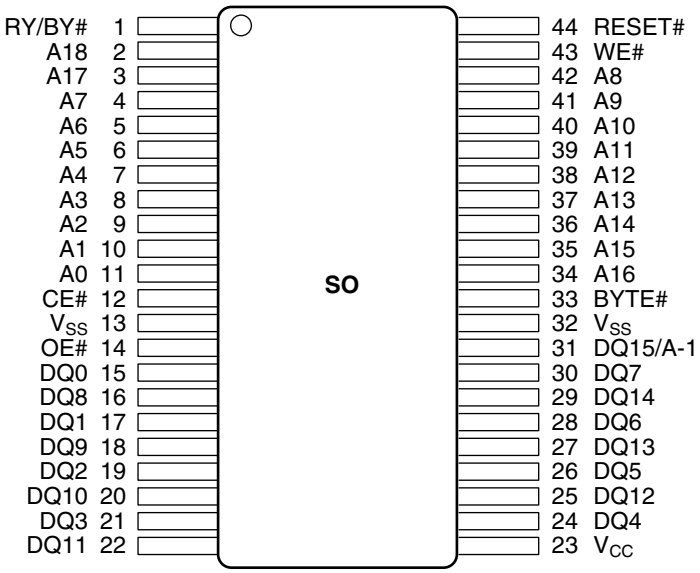
BLOCK DIAGRAM



CONNECTION DIAGRAMS



CONNECTION DIAGRAMS



48-Ball FBGA
Top View, Balls Facing Down

A6 A13	B6 A12	C6 A14	D6 A15	E6 A16	F6 BYTE#	G6 DQ15/A-1	H6 V_{SS}
A5 A9	B5 A8	C5 A10	D5 A11	E5 DQ7	F5 DQ14	G5 DQ13	H5 DQ6
A4 WE#	B4 RESET#	C4 NC	D4 NC	E4 DQ5	F4 DQ12	G4 V_{CC}	H4 DQ4
A3 RY/BY#	B3 NC	C3 A18	D3 NC	E3 DQ2	F3 DQ10	G3 DQ11	H3 DQ3
A2 A7	B2 A17	C2 A6	D2 A5	E2 DQ0	F2 DQ8	G2 DQ9	H2 DQ1
A1 A3	B1 A4	C1 A2	D1 A1	E1 A0	F1 CE#	G1 OE#	H1 V_{SS}

Special Handling Instructions for FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN DESCRIPTION

A0-A18 = 19 Addresses

DQ0-DQ14 = 15 Data Inputs/Outputs

DQ15/A-1 = DQ15 (Data Input/Output, word mode), A-1 (LSB Address Input, byte mode)

CE# = Chip Enable

OE# = Output Enable

WE# = Write Enable

BYTE# = Selects 8-bit or 16-bit mode

RESET# = Hardware Reset Pin, Active Low

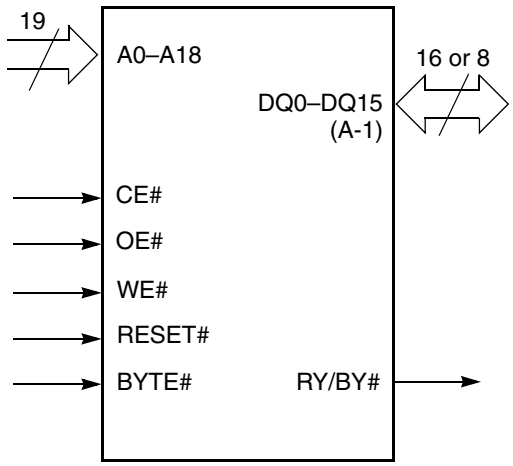
RY/BY# = Ready/Busy Output

V_{CC} = 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)

V_{SS} = Device Ground

NC = Pin Not Connected Internally

LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:

Am29DL800B T 70 E I

TEMPERATURE RANGE

C	=	Commercial (0°C to +70°C)
D	=	Commercial (0°C to +70°C) with Pb-Free package
I	=	Industrial (–40°C to +85°C)
F	=	Industrial (–40°C to +85°C) with Pb-Free package
E	=	Extended (–55°C to +125°C)
K	=	Extended (–55°C to +125°C) with Pb-Free package

PACKAGE TYPE

E	=	48-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 048)
S	=	44-Pin Small Outline Package (SO 044)
WB	=	48-Ball Fine-Pitch Ball Grid Array (FBGA) 0.80 mm pitch, 6 x 9 mm package (FBB048)

SPEED OPTION

See Product Selector Guide and Valid Combinations

BOOT CODE SECTOR ARCHITECTURE

T	=	Top sector
B	=	Bottom sector

DEVICE NUMBER/DESCRIPTION

Am29DL800B
8 Megabit (1 M x 8-Bit/512 K x 16-Bit) CMOS Flash Memory
3.0 Volt-only Read, Program, and Erase

Valid Combinations for TSOP and SO Packages	
AM29DL800BT70, AM29DL800BB70	EC, EI, ED, EF SC, SI, SD, SF
AM29DL800BT90, AM29DL800BB90	EC, EI, EE, ED, EF, EK SC, SI, SE, SD, SF, SK
AM29DL800BT120, AM29DL800BB120	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Valid Combinations for FBGA Packages			
Order Number		**Package Marking**	
AM29DL800BT70, AM29DL800BB70	WBC, WBI, WBD, WBF	D800BT70V, D800BB70V	C, I, D, F
AM29DL800BT90, AM29DL800BB90	WBC, WBI, WBE, WBD, WBF, WBK	D800BT90V, D800BB90V	C, I, E, D, F, K
AM29DL800BT120, AM29DL800BB120		D800BT12V, D800BB12V	

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Am29DL800B Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	Addresses (Note 1)	DQ0–DQ7	DQ8–DQ15	
							BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Write	L	H	L	H	A_{IN}	D_{IN}	D_{IN}	
Standby	$V_{CC} \pm 0.3$ V	X	X	$V_{CC} \pm 0.3$ V	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	High-Z	High-Z	High-Z
Sector Protect (Note 2)	L	H	L	V_{ID}	Sector Address, A6 = L, A1 = H, A0 = L	D_{IN}	X	X
Sector Unprotect (Note 2)	L	H	L	V_{ID}	Sector Address, A6 = H, A1 = H, A0 = L	D_{IN}	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	A_{IN}	D_{IN}	D_{IN}	High-Z

Legend:
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes:
1. *Addresses are A18:A0 in word mode (BYTE# = V_{IH}), A18:A-1 in byte mode (BYTE# = V_{IL}).*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector Protection/Unprotection" section.*

Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ0-15 are active and controlled by CE# and OE# .

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read-Only Operations table for timing specifications and to Figure 13 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing

sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. Refer to “Word/Byte Configuration” for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The “Byte/Word Program Command Sequence” section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Tables 2 and 3 indicate the address space that each sector occupies. The device address space is divided into two banks: Bank 1 contains the boot/parameter sectors, and Bank 2 contains the larger, code sectors of uniform size. A “bank address” is the address bits required to uniquely select a bank. Similarly, a “sector address” is the address bits required to uniquely select a sector.

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence sections for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in the other bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 19 shows how read and write cycles may be initiated for simultaneous operation with zero latency. I_{CC6} and I_{CC7} in the DC Characteristics table represent the current specifications for read-while-program and read-while-erase, respectively.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within $V_{CC} \pm 0.3$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics table represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device **immediately terminates** any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 14 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Am29DL800BT Top Boot Sector Architecture

Bank	Sector	Sector Address							Sector Size (Kbytes/ Kwords)	(x8) Address Range	(x16) Address Range
		Bank Address									
		A18	A17	A16	A15	A14	A13	A12			
Bank 2	SA0	0	0	0	0	X	X	X	64/32	00000h–0FFFFh	00000h–07FFFh
	SA1	0	0	0	1	X	X	X	64/32	10000h–1FFFFh	08000h–0FFFFh
	SA2	0	0	1	0	X	X	X	64/32	20000h–2FFFFh	10000h–17FFFh
	SA3	0	0	1	1	X	X	X	64/32	30000h–3FFFFh	18000h–1FFFFh
	SA4	0	1	0	0	X	X	X	64/32	40000h–4FFFFh	20000h–27FFFh
	SA5	0	1	0	1	X	X	X	64/32	50000h–5FFFFh	28000h–2FFFFh
	SA6	0	1	1	0	X	X	X	64/32	60000h–6FFFFh	30000h–37FFFh
	SA7	0	1	1	1	X	X	X	64/32	70000h–7FFFFh	38000h–3FFFFh
	SA8	1	0	0	0	X	X	X	64/32	80000h–8FFFFh	40000h–47FFFh
	SA9	1	0	0	1	X	X	X	64/32	90000h–9FFFFh	48000h–4FFFFh
	SA10	1	0	1	0	X	X	X	64/32	A0000h–AFFFFh	50000h–57FFFh
	SA11	1	0	1	1	X	X	X	64/32	B0000h–BFFFFh	58000h–5FFFFh
	SA12	1	1	0	0	X	X	X	64/32	C0000h–CFFFFh	60000h–67FFFh
	SA13	1	1	0	1	X	X	X	64/32	D0000h–DFFFFh	68000h–6FFFFh
Bank 1	SA14	1	1	1	0	0	0	X	16/8	E0000h–E3FFFh	70000h–71FFFh
	SA15	1	1	1	0	0	1	X	32/16	E4000h–E7FFFh, E8000h–EBFFFh	72000h–73FFFh 74000h–75FFFh
						1	0	X			
	SA16	1	1	1	0	1	1	0	8/4	EC000h–EDFFFh	76000h–76FFFh
	SA17	1	1	1	0	1	1	1	8/4	EE000h–EFFFFh	77000h–77FFFh
	SA18	1	1	1	1	0	0	0	8/4	F0000h–F1FFFh	78000h–78FFFh
	SA19	1	1	1	1	0	0	1	8/4	F2000h–F3FFFh	79000h–79FFFh
	SA20	1	1	1	1	0	1	X	32/16	F4000h–F7FFFh, F8000h–FBFFFh	7A000h–7BFFFh 7C000h–7DFFFh
						1	0	X			
	SA21	1	1	1	1	1	1	X	16/8	FC000h–FFFFFh	7E000h–7FFFFh

Note: *The address range is A18:A-1 if in byte mode (BYTE# = V_{IL}). The address range is A18:A0 if in word mode (BYTE# = V_{IH}).*

Table 3. Am29DL800BB Bottom Boot Sector Architecture

Bank	Sector	Sector Address: Bank Address A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	(x8) Address Range	(x16) Address Range
Bank 2	SA21	1	1	1	1	X	X	X	64/32	F0000h–FFFFFh	78000h–7FFFFh
	SA20	1	1	1	0	X	X	X	64/32	E0000h–EFFFFh	70000h–77FFFh
	SA19	1	1	0	1	X	X	X	64/32	D0000h–DFFFFh	68000h–6FFFFh
	SA18	1	1	0	0	X	X	X	64/32	C0000h–CFFFFh	60000h–67FFFh
	SA17	1	0	1	1	X	X	X	64/32	B0000h–BFFFFh	58000h–5FFFFh
	SA16	1	0	1	0	X	X	X	64/32	A0000h–AFFFFh	50000h–57FFFh
	SA15	1	0	0	1	X	X	X	64/32	90000h–9FFFFh	48000h–4FFFFh
	SA14	1	0	0	0	X	X	X	64/32	80000h–8FFFFh	40000h–47FFFh
	SA13	0	1	1	1	X	X	X	64/32	70000h–7FFFFh	38000h–3FFFFh
	SA12	0	1	1	0	X	X	X	64/32	60000h–6FFFFh	30000h–37FFFh
	SA11	0	1	0	1	X	X	X	64/32	50000h–5FFFFh	28000h–2FFFFh
	SA10	0	1	0	0	X	X	X	64/32	40000h–4FFFFh	20000h–27FFFh
	SA9	0	0	1	1	X	X	X	64/32	30000h–3FFFFh	18000h–1FFFFh
	SA8	0	0	1	0	X	X	X	64/32	20000h–2FFFFh	10000h–17FFFh
Bank 1	SA7	0	0	0	1	1	1	X	16/8	1C000h–1FFFFh	0E000h–0FFFFh
	SA6	0	0	0	1	1	0	X	32/16	18000h–1BFFFh 14000h–17FFFh	0C000h–0DFFFh 0A000h–0BFFFh
						0	1	X			
	SA5	0	0	0	1	0	0	1	8/4	12000h–13FFFh	09000h–09FFFh
	SA4	0	0	0	1	0	0	0	8/4	10000h–11FFFh	08000h–08FFFh
	SA3	0	0	0	0	1	1	1	8/4	0E000h–0FFFFh	07000h–07FFFh
	SA2	0	0	0	0	1	1	0	8/4	0C000h–0DFFFh	06000h–06FFFh
	SA1	0	0	0	0	1	0	X	32/16	08000h–0BFFFh, 04000h–07FFFh	04000h–05FFFh, 02000h–03FFFh,
						0	1	X			
	SA0	0	0	0	0	0	0	X	16/8	00000h–03FFFh	00000h–01FFFh

Note: *The address range is A18:A-1 if in byte mode (BYTE# = V_{IL}). The address range is A18:A0 if in word mode (BYTE# = V_{IH}).*

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 4. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Tables 2 and 3). Table 4 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 5. This method does not require V_{ID}. Refer to the Autoselect Command Sequence section for more information.

Table 4. Am29DL800B Autoselect Codes (High Voltage Method)

Description	Mode	CE#	OE#	WE#	A18 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID: AMD		L	L	H	BA	X	V_{ID}	X	L	X	L	L	X	01h
Device ID: Am29DL800B (Top Boot Block)	Word	L	L	H	BA	X	V_{ID}	X	L	X	L	H	22h	4Ah
	Byte	L	L	H									X	4Ah
Device ID: Am29DL800B (Bottom Boot Block)	Word	L	L	H	BA	X	V_{ID}	X	L	X	L	H	22h	CBh
	Byte	L	L	H									X	CBh
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	H	L	X	01h (protected)
													X	00h (unprotected)

Note: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, BA = Bank Address, SA = Sector Address, X = Don't care.*

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection/unprotection can be implemented via two methods.

The primary method requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 2 shows the algorithms and Figure 24 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

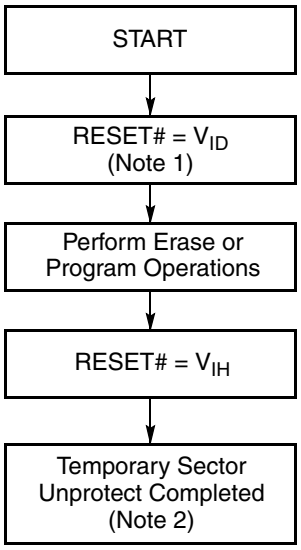
The alternate method intended only for programming equipment requires V_{ID} on address pin A9 and OE#. This method is compatible with programmer routines written for earlier 3.0 volt-only AMD flash devices. Publication number 21467 contains further details; contact an AMD representative to request a copy.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See the Autoselect Mode section for details.

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID} (11.5 V – 12.5 V). During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 1 shows the algorithm, and Figure 23 shows the timing diagrams, for this feature.



Notes:
1. *All protected sectors unprotected.*
2. *All previously protected sectors are protected once again.*

Figure 1. Temporary Sector Unprotect Operation

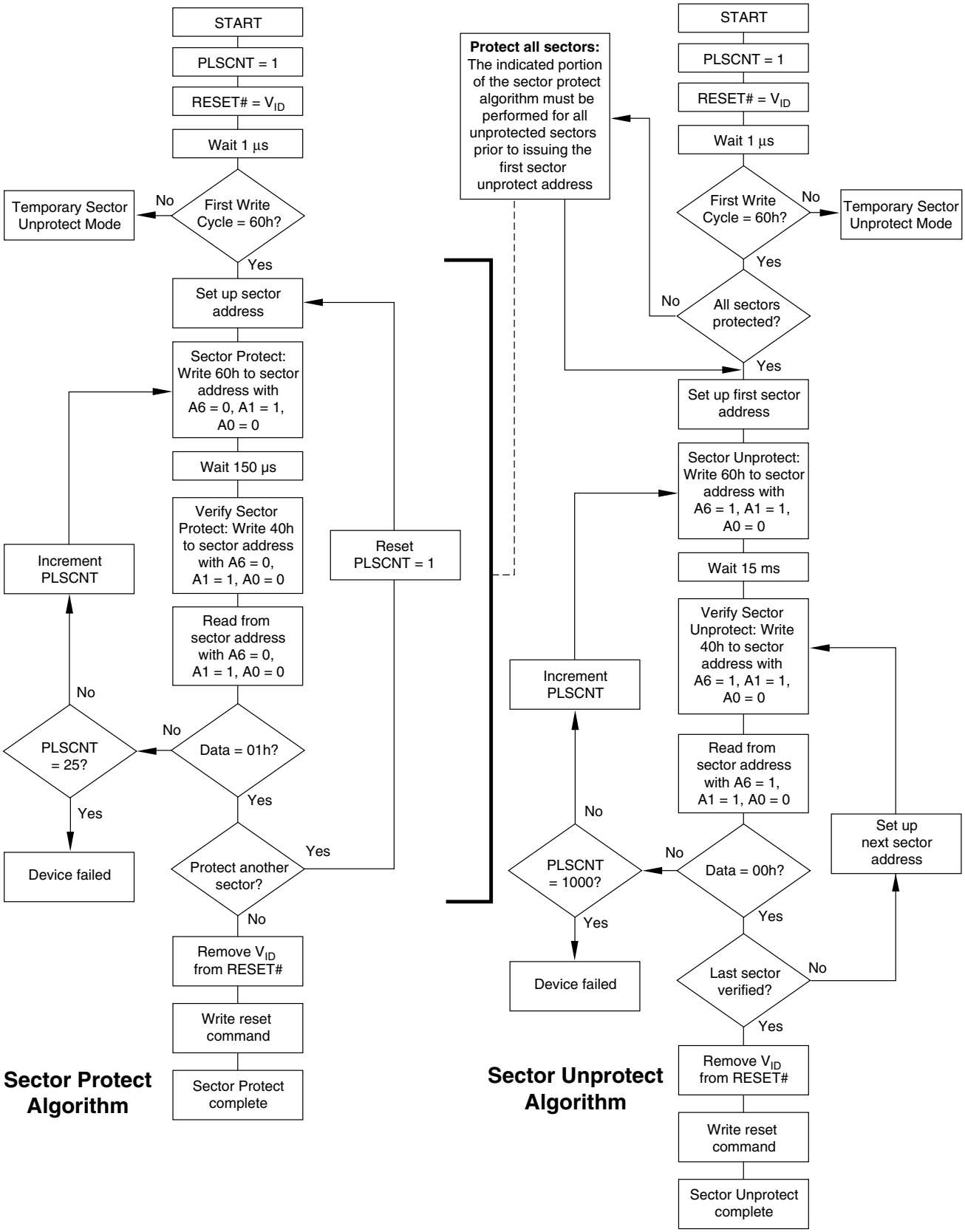


Figure 2. In-System Sector Protect/Unprotect Algorithms

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 5 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 5 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in the AC Characteristics section.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the Device Bus Operations section for more information. The Read-Only Operations table provides the read parameters, and Figure 13 shows the timing diagram.

Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the reading array data. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to reading array data (or erase-suspend-read mode if that bank was in Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes,

and determine whether or not a sector is protected. Table 5 shows the address and data requirements. This method is an alternative to that shown in Table 4, which is intended for PROM programmers and requires V_{ID} on address pin A9. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The addressed bank then enters the autoselect mode. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence:

- A read cycle at address (BA)XX00h (where BA is the bank address) returns the manufacturer code.
- A read cycle at address (BA)XX01h in word mode (or (BA)XX02h in byte mode) returns the device code.
- A read cycle to an address containing a sector address (SA) within the same bank, and the address 02h on A7–A0 in word mode (or the address 04h on A6–A-1 in byte mode) returns 01h if the sector is protected, or 00h if it is unprotected. Refer to Tables 2 and 3 for valid sector addresses.

The system may continue to read array data from the other bank while a bank is in the autoselect mode. To exit the autoselect mode, the system must write the reset command to return both banks to reading array data. If a bank enters the autoselect mode while erase suspended, a reset command returns that bank to the erase-suspend-read mode. A subsequent Erase Resume command returns the bank to the erase operation.

Byte/Word Program Command Sequence

The system may program the device by word or byte, depending on the state of the BYTE# pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 5 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, that bank then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Note that while the Embedded Program operation is in progress, the system can read data from the non-programming bank. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

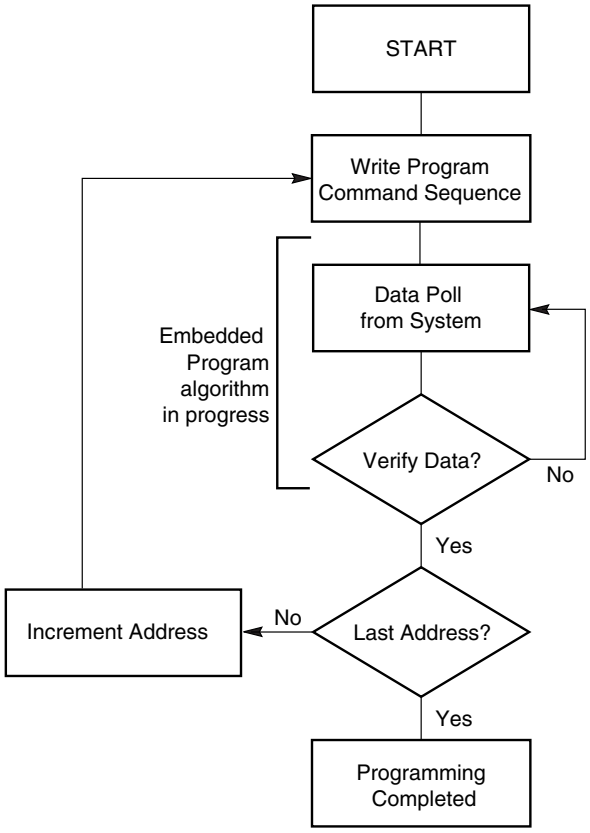
Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from “0” back to a “1.”** Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still “0.” Only erase operations can convert a “0” to a “1.”

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 5 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the bank address and the data 90h. The second cycle need only contain the data 00h. The bank then returns to reading array data.

Figure 3 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 17 for timing diagrams.



Note: *See Table 5 for program command sequence.*

Figure 3. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 5 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 18 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 5 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands within the bank may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command may not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to reading array data.** The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 (in the erasing bank) to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading DQ7, DQ6, DQ2, or RY/BY# in the erasing bank. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** im-

mediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 18 section for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

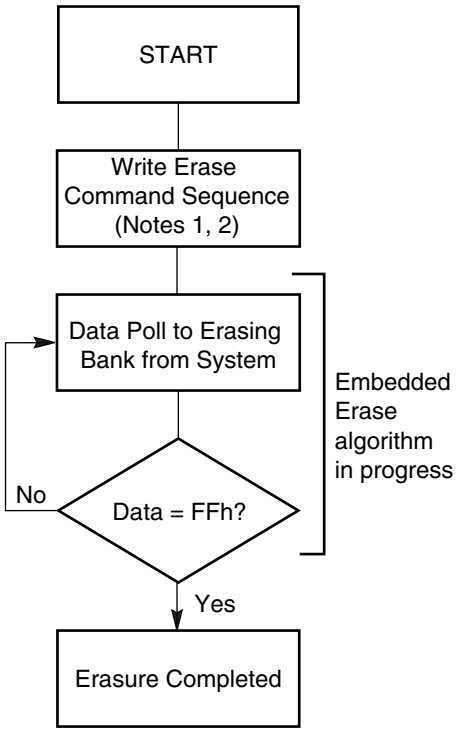
When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard Byte Program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the Autoselect Mode and Autoselect Command Sequence sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.



Notes:

1. *See Table 5 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 4. Erase Operation

Command Definitions

Table 5. Am29DL800B Command Definitions

Command Sequence (Note 1)			Cycles	Bus Cycles (Notes 2–5)											
				First		Second		Third		Fourth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)			1	RA	RD										
Reset (Note 7)			1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	Word	4	555	AA	2AA	55	(BA)555	90	(BA)X00	01				
		Byte		AAA		555		(BA)AAA							
	Device ID, Top Boot Block	Word	4	555	AA	2AA	55	(BA)555	90	(BA)X01	224A				
		Byte		AAA		555		(BA)AAA		(BA)X02	4A				
	Device ID, Bottom Boot Block	Word	4	555	AA	2AA	55	(BA)555	90	(BA)X01	22CB				
		Byte		AAA		555		(BA)AAA		(BA)X02	CB				
	Sector Protect Verify (Note 9)	Word	4	555	AA	2AA	55	(BA)555	90	(SA) X02	XX00				
											XX01				
		Byte		AAA		555		(BA)AAA		(SA) X04	00				
											01				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Unlock Bypass		Word	3	555	AA	2AA	55	555	20						
		Byte		AAA		555		AAA							
Unlock Bypass Program (Note 10)			2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 11)			2	BA	90	XXX	00								
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Erase Suspend (Note 12)			1	BA	B0										
Erase Resume (Note 13)			1	BA	30										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A18–A12 uniquely select any sector.

BA = Address of the bank that is being switched to autoselect mode, is in bypass mode, or is being erased. Address bits A18–A16 select a bank.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except when reading array or autoselect data, all bus cycles are write operations.*
4. *Data bits DQ15–DQ8 are don't cares for unlock and command cycles.*
5. *Address bits A18–A11 are don't cares for unlock and command cycles, unless bank address (BA) is required.*
6. *No unlock or command cycles required when bank is in read mode.*
7. *The Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 is goes high (while the bank is providing status information).*
8. *The fourth cycle of the autoselect command sequence is a read cycle. The system must provide the bank address to obtain the manufacturer or device ID information.*
9. *The data is 00h for an unprotected sector and 01h for a protected sector. See the Autoselect Command Sequence section for more information.*
10. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
11. *The Unlock Bypass Reset command is required to return to reading array data when the bank is in the unlock bypass mode.*
12. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and requires the bank address.*
13. *The Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation in the bank where a program or erase operation is in progress: DQ2, DQ3, DQ5, DQ6, DQ7, and RY/BY#. Table 6 and the following subsections describe the function of these bits. DQ7, RY/BY#, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

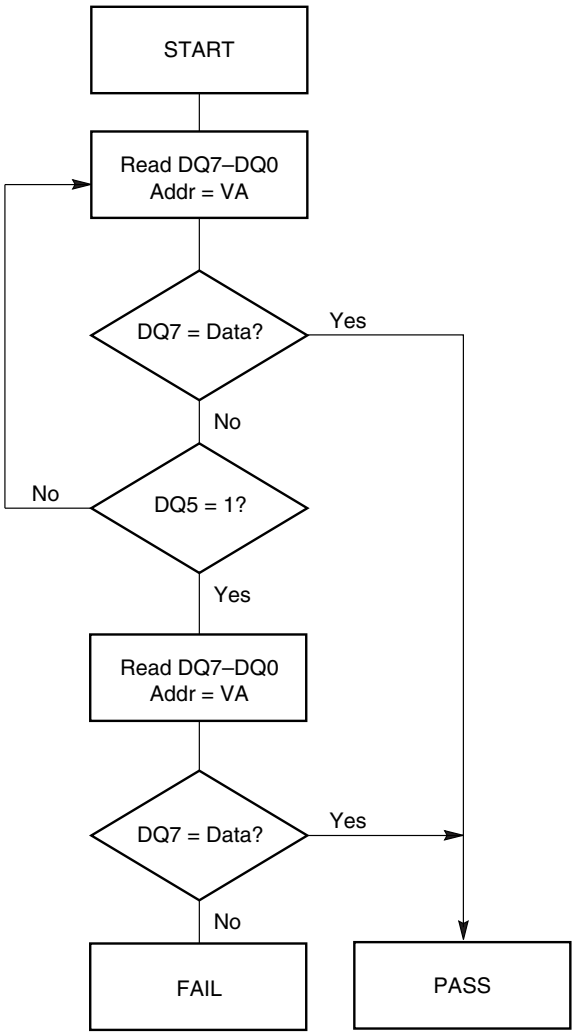
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the bank returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0–DQ6 may be still invalid. Valid data on DQ0–DQ7 will appear on successive read cycles.

Table 6 shows the outputs for Data# Polling on DQ7. Figure 5 shows the Data# Polling algorithm. Figure 20 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.*

Figure 5. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data, is in the standby mode, or one of the banks is in the erase-suspend-read mode.

Table 6 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address within the programming or erasing bank, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address within the programming or erasing bank cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When a bank is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When that bank enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 6 shows the outputs for Toggle Bit I on DQ6. Figure 6 shows the toggle bit algorithm. Figure 21 in the "AC Characteristics" section shows the toggle bit timing diagrams. Figure 22 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 6 to compare outputs for DQ2 and DQ6.

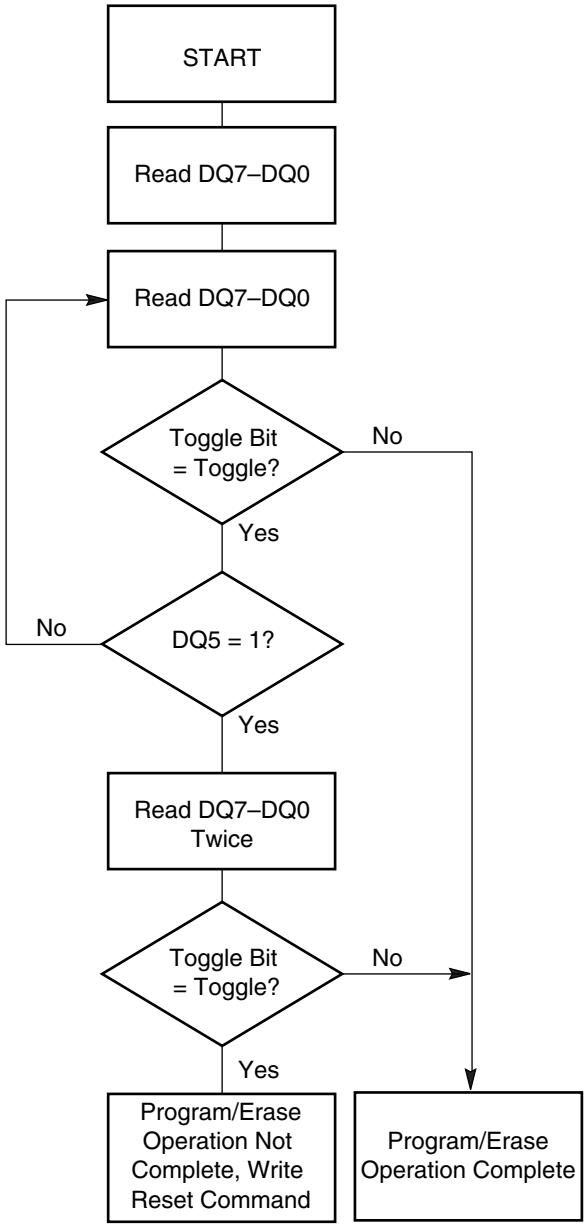
Figure 6 shows the toggle bit algorithm in flowchart form, and the section "DQ2: Toggle Bit II" explains the algorithm. See also the DQ6: Toggle Bit I subsection. Figure 21 shows the toggle bit timing diagram. Figure 22 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6).



Note: *The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.*

Figure 6. Toggle Bit Algorithm

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1".

Under both these conditions, the system must write the reset command to return to reading array data (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1". If the system can guarantee the time between additional sector erase commands to be less than 50 µs, it need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1", the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 6 shows the status of DQ3 relative to the other status bits.

Table 6. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V

A9, OE#,
and RESET# (Note 2). . . . . –0.5 V to +12.5 V

All other pins
(Note 1). . . . . –0.5 V to V_{CC}+0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. See Figure 7. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 8.*
2. *Minimum DC input voltage on pins A9, OE#, and RESET# is –0.5 V. During voltage transitions, A9, OE#, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

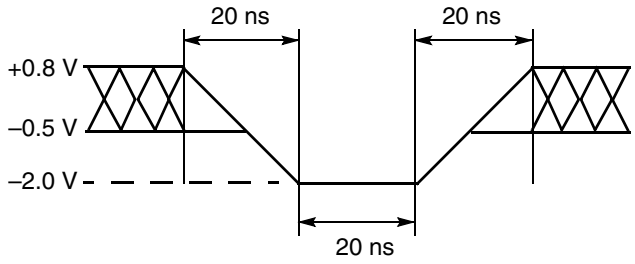


Figure 7. Maximum Negative Overshoot Waveform

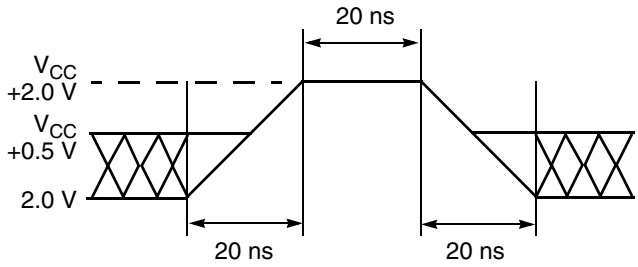


Figure 8. Maximum Positive Overshoot Waveform

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A) . . . . . –55°C to +125°C

V_{CC} Supply Voltages

V_{CC} for all devices . . . . . 2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

CMOS Compatible

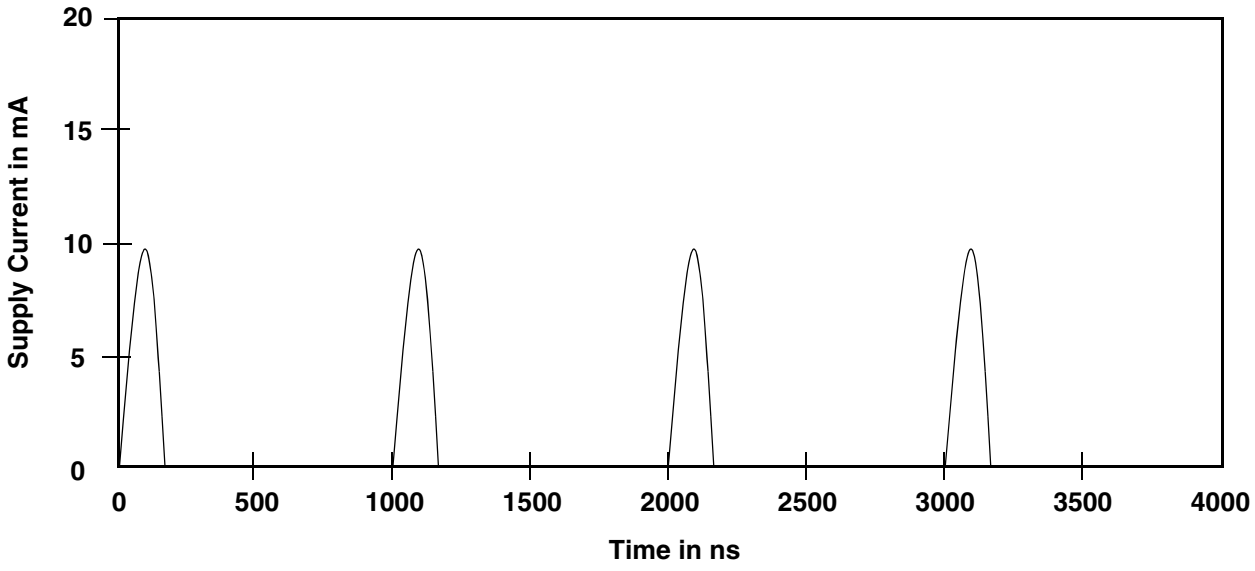
Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}, Byte Mode	5 MHz		7	12	mA
			1 MHz		2	4	
		CE# = V_{IL}, OE# = V_{IH}, Word Mode	5 MHz		7	12	
			1 MHz		2	4	
I_{CC2}	V_{CC} Active Write Current (Notes 2, 3)	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IL}			15	30	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	OE# = V_{IL}; CE#, RESET# = V_{CC} ± 0.3 V			0.2	5	µA
I_{CC4}	V_{CC} Reset Current (Note 2)	RESET# = V_{SS} ± 0.3 V			0.2	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 2, 4)	$V_{IH} = V_{CC}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V			0.2	5	µA
I_{CC6}	V_{CC} Active Read-While-Program Current (Notes 1, 2, 5)	CE# = V_{IL}, OE# = V_{IH}	Byte		21	45	mA
			Word		21	45	
I_{CC7}	V_{CC} Active Read-While-Erase Current (Notes 1, 2, 5)	CE# = V_{IL}, OE# = V_{IH}	Byte		21	45	mA
			Word		21	45	
I_{CC8}	V_{CC} Active Program-While-Erase-Suspended Current (Notes 2, 5)	CE# = V_{IL}, OE# = V_{IH}			17	35	mA
V_{IL}	Input Low Voltage			–0.5		0.8	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.0 V ± 10%		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min}$		0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{CC}–0.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 5)			2.3		2.5	V

Notes:

1. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
2. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 200 nA.*
5. *Not 100% tested.*

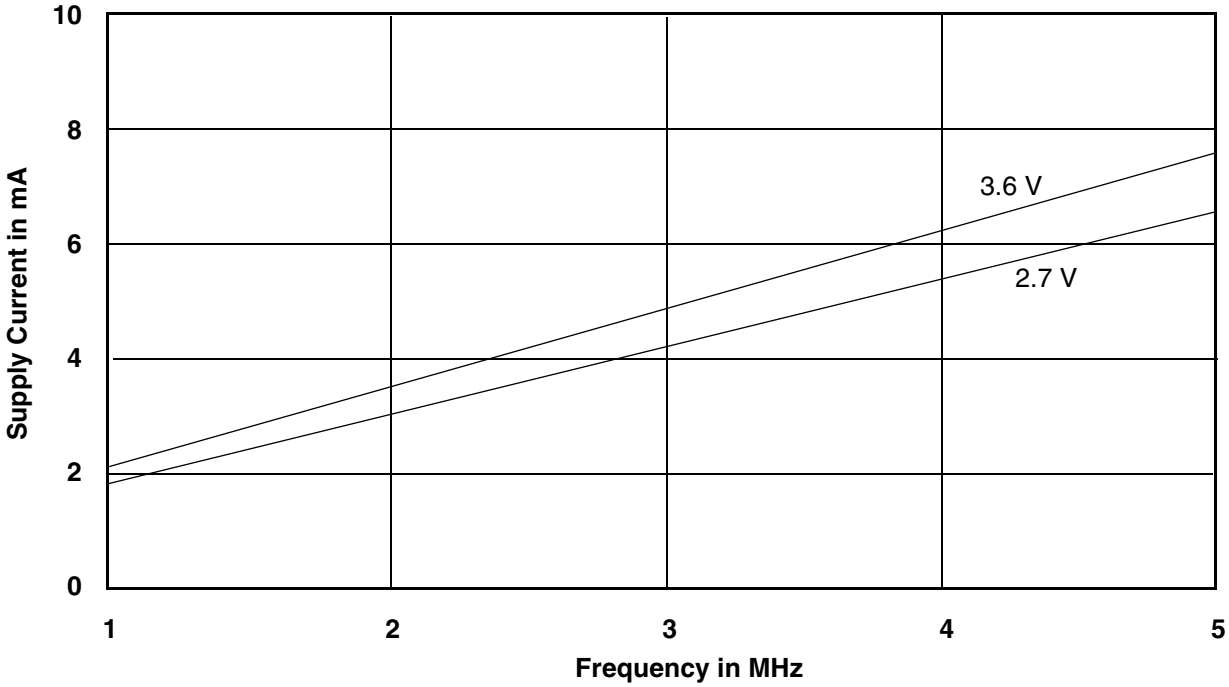
DC CHARACTERISTICS

Zero-Power Flash



Note: *Addresses are switching at 1 MHz*

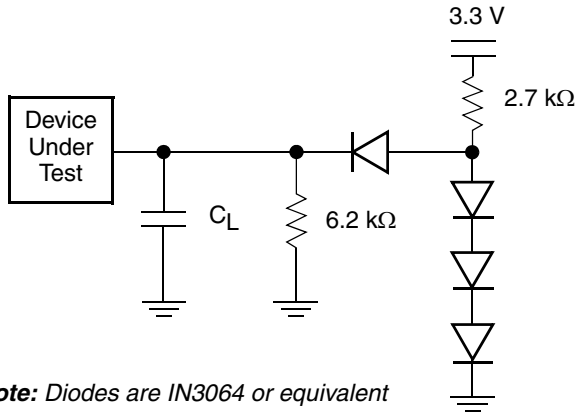
Figure 9. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: *T = 25 °C*

Figure 10. Typical I_{CC1} vs. Frequency

TEST CONDITIONS



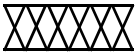
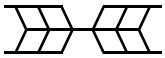
Note: *Diodes are IN3064 or equivalent*

Figure 11. Test Setup

Table 7. Test Specifications

Test Condition	70	90, 120	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0–3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

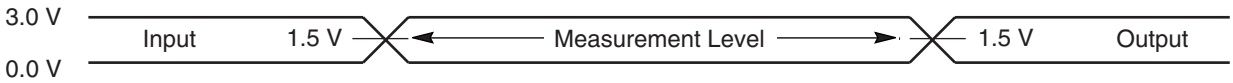


Figure 12. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Read-Only Operations

Parameter		Description		Test Setup		Speed Options			Unit
JEDEC	Std					70	90	120	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	70	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE#, OE# = V_{IL}	Max	70	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	70	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	25	30	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	25	30	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0			ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0			ns
			Toggle and Data# Polling		Min	10			ns

Notes:

1. *Not 100% tested.*
2. *See Figure 11 and Table 7 for test specifications.*

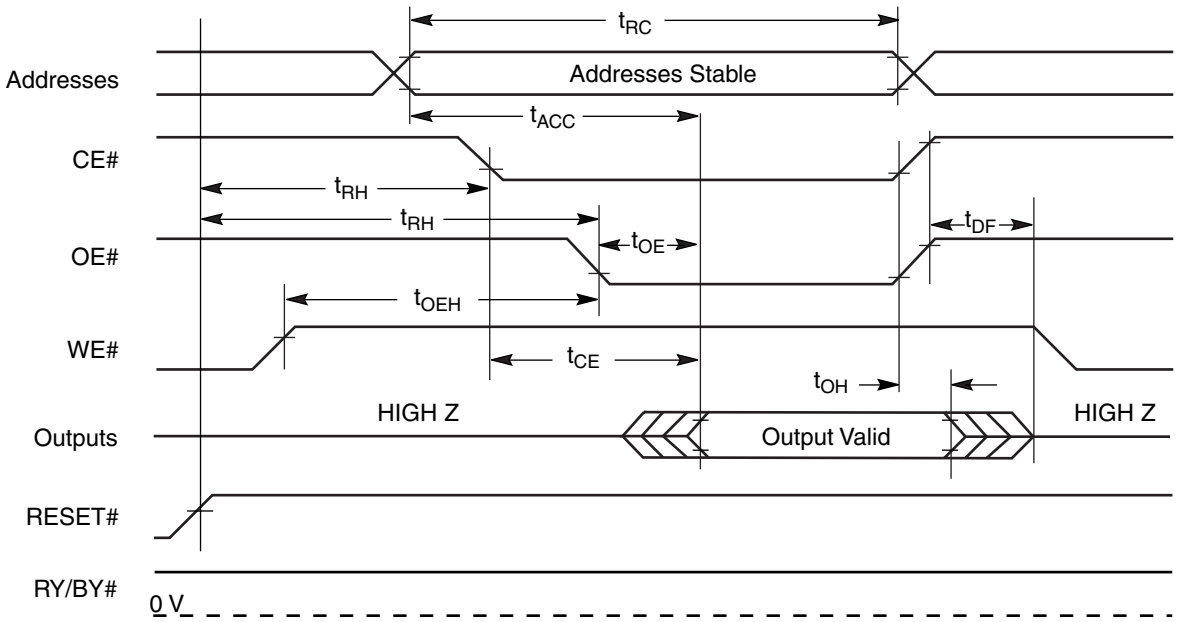


Figure 13. Read Operation Timings

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note: *Not 100% tested.*

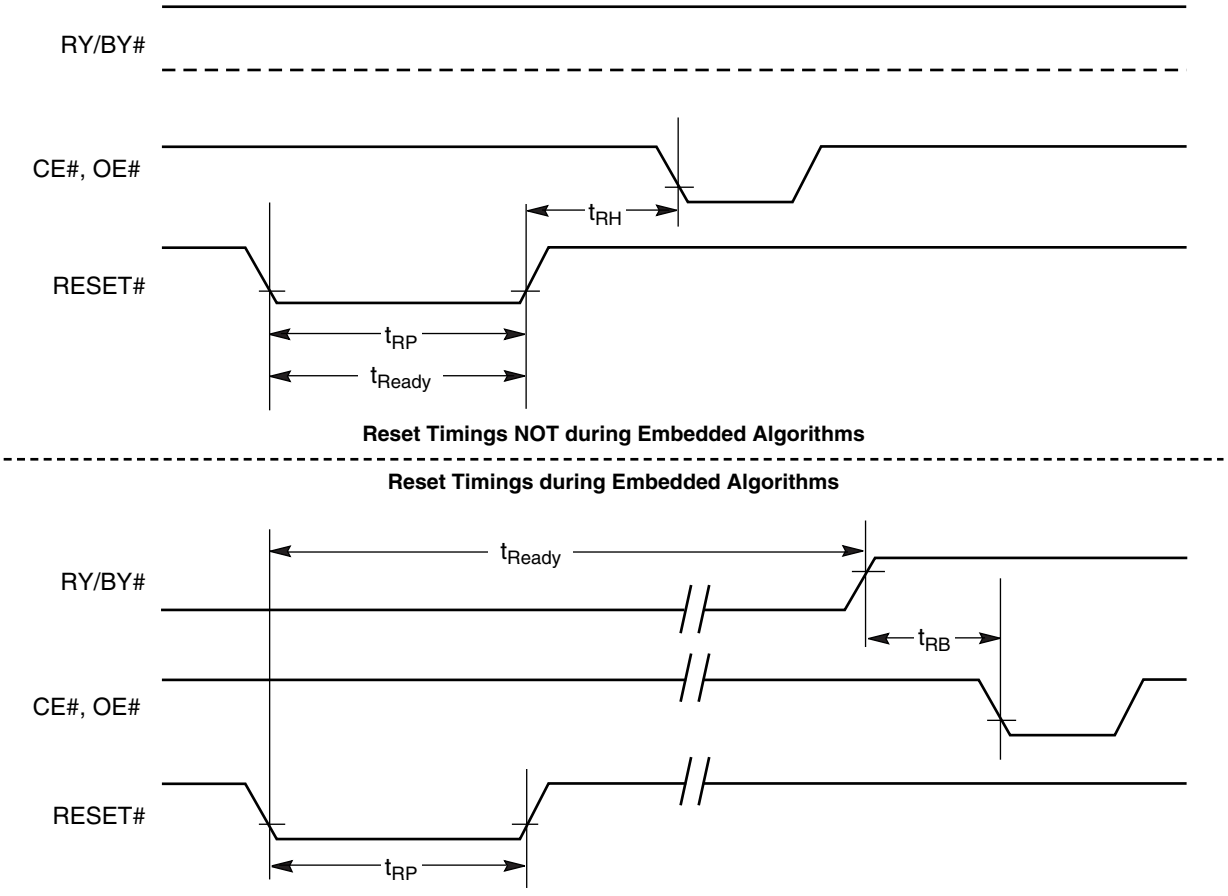


Figure 14. Reset Timings

AC CHARACTERISTICS

Word/Byte Configuration (BYTE#)

Parameter							
JEDEC	Std	Description		70	90	120	Unit
	t_{ELFL}/t_{ELFH}	CE# to BYTE# Switching Low or High	Max		5		ns
	t_{FLQZ}	BYTE# Switching Low to Output HIGH Z	Max	25	30	30	ns
	t_{FHQV}	BYTE# Switching High to Output Active	Min	70	90	120	ns

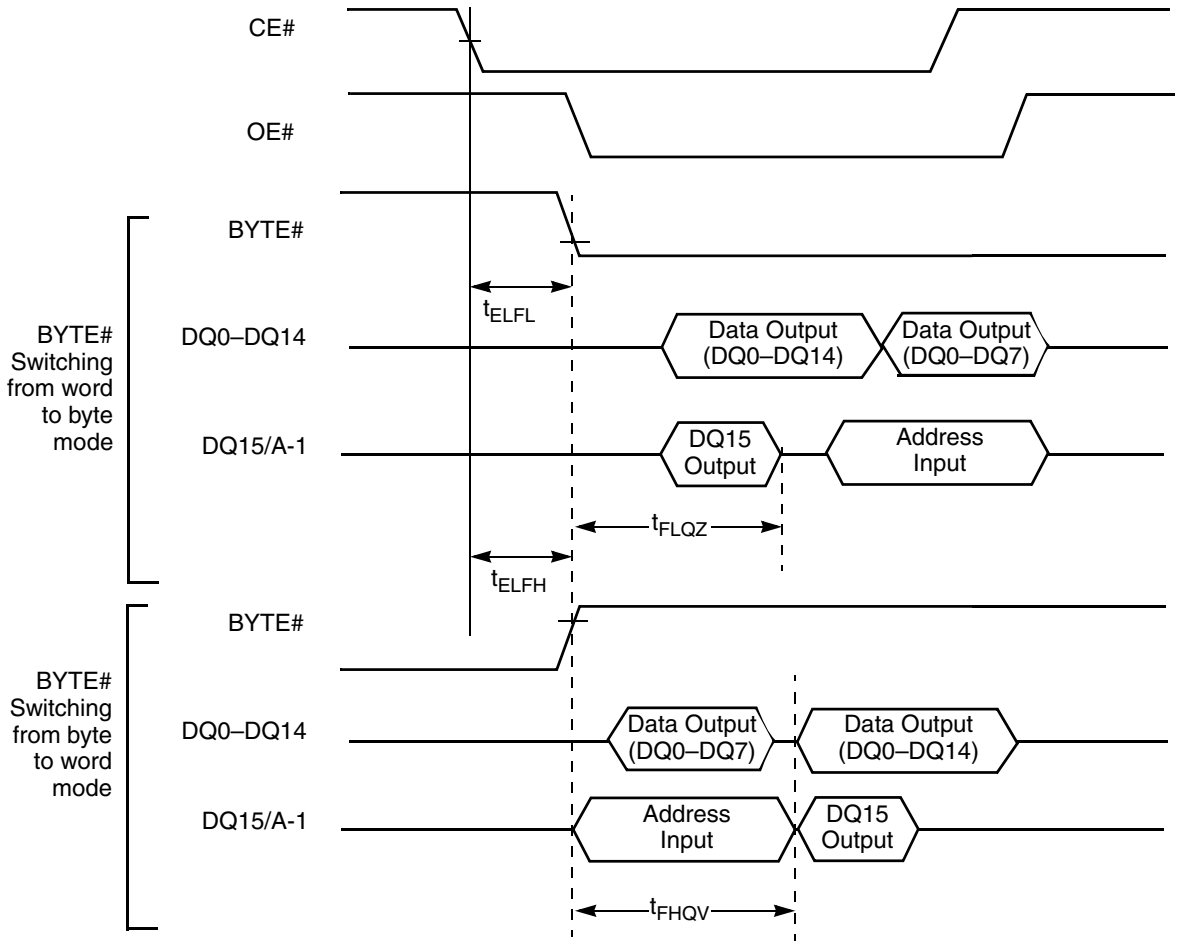
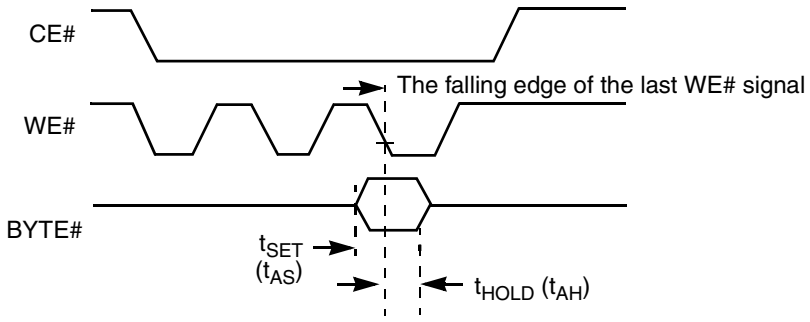


Figure 15. BYTE# Timings for Read Operations



Note: *Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.*

Figure 16. BYTE# Timings for Write Operations

AC CHARACTERISTICS

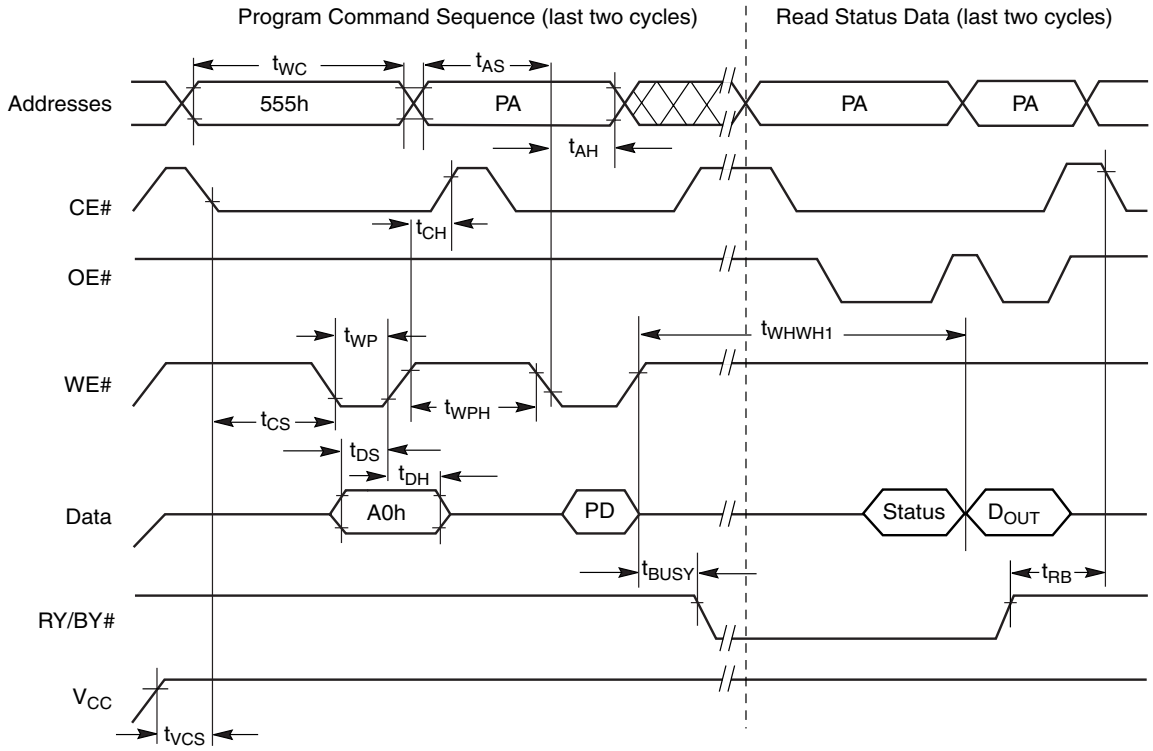
Erase and Program Operations

Parameter							
JEDEC	Std	Description			70	90	120	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0			ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	45	45	50	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	45	50	ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0			ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	35	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0			ns
	t_{OEPH}	Output Enable High during toggle bit polling		Min	20	20	25	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0			ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0			ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0			ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	35	50	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	30			ns
	$t_{SR/W}$	Zero Latency Between Read and Write Operations		Min	0			ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	9			µs
			Word	Typ	11			
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.7			sec
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50			µs
	t_{RB}	Write Recovery Time from RY/BY#		Min	0			ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay		Max	90			ns

Notes:

1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*

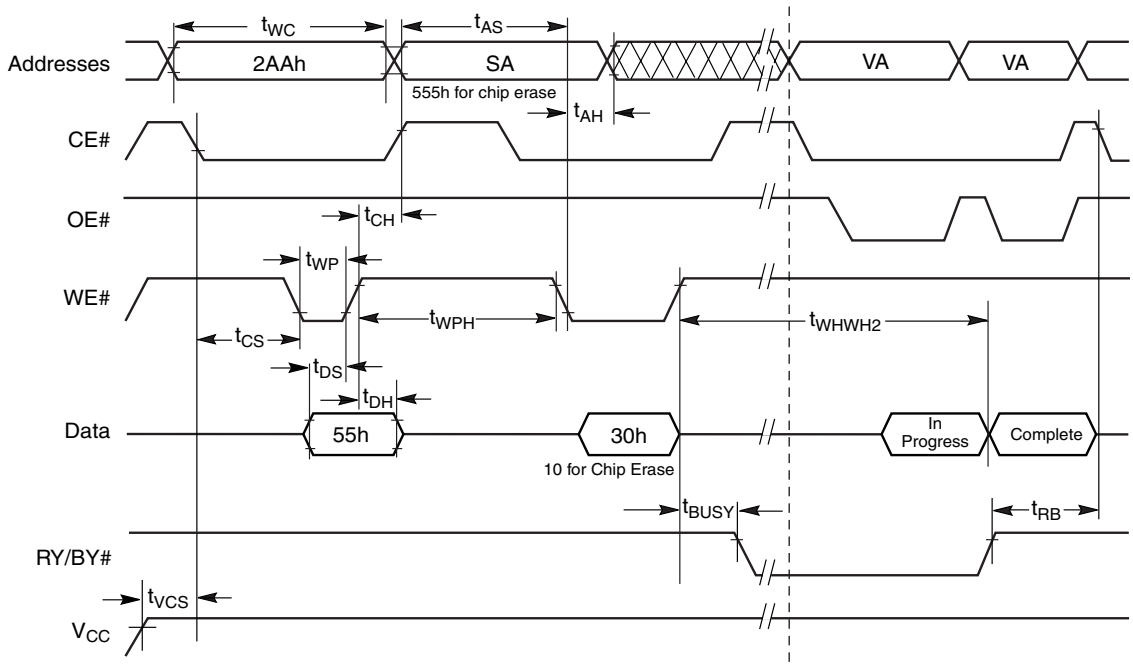
AC CHARACTERISTICS



Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode*

Figure 17. Program Operation Timings



Notes:

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data(see "Write Operation Status").*
2. *Illustration shows device in word mode.*

Figure 18. Chip/Sector Erase Operation Timings

AC CHARACTERISTICS

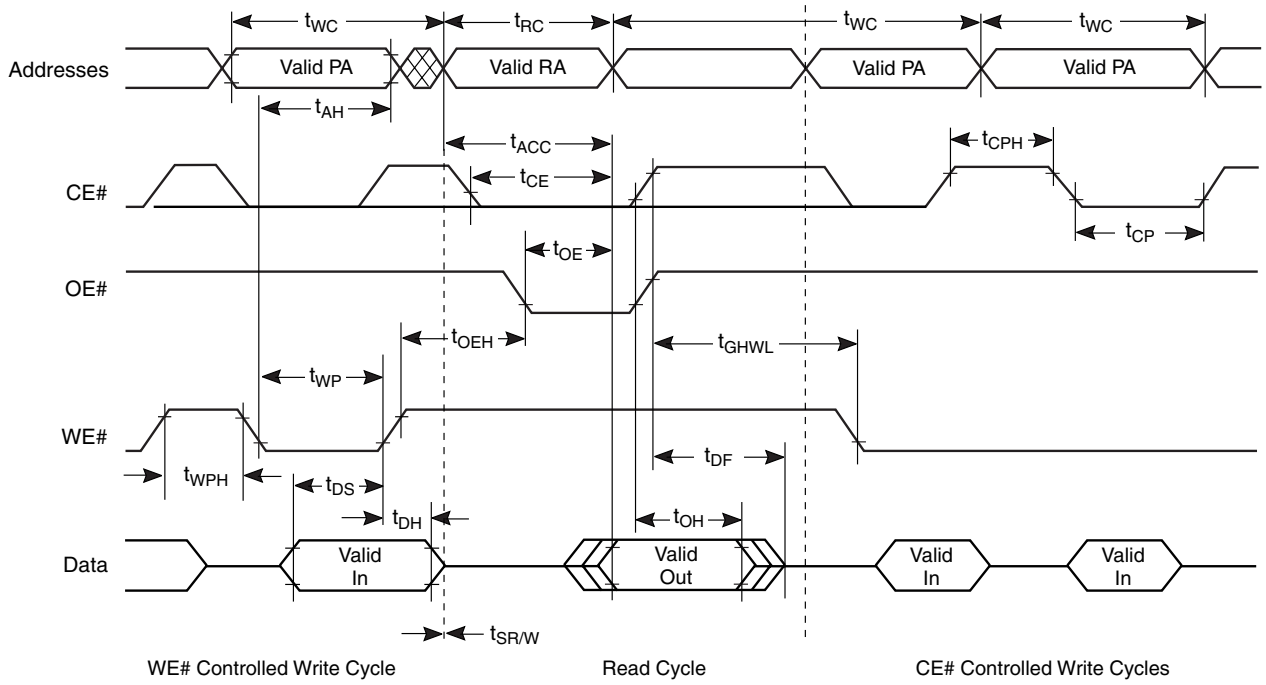
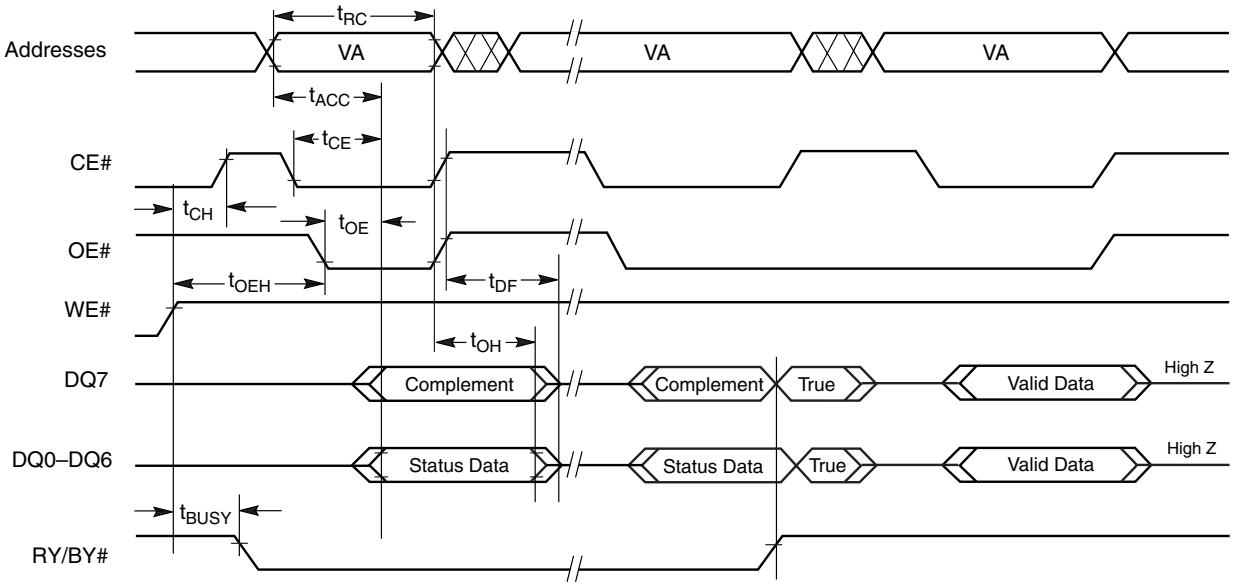


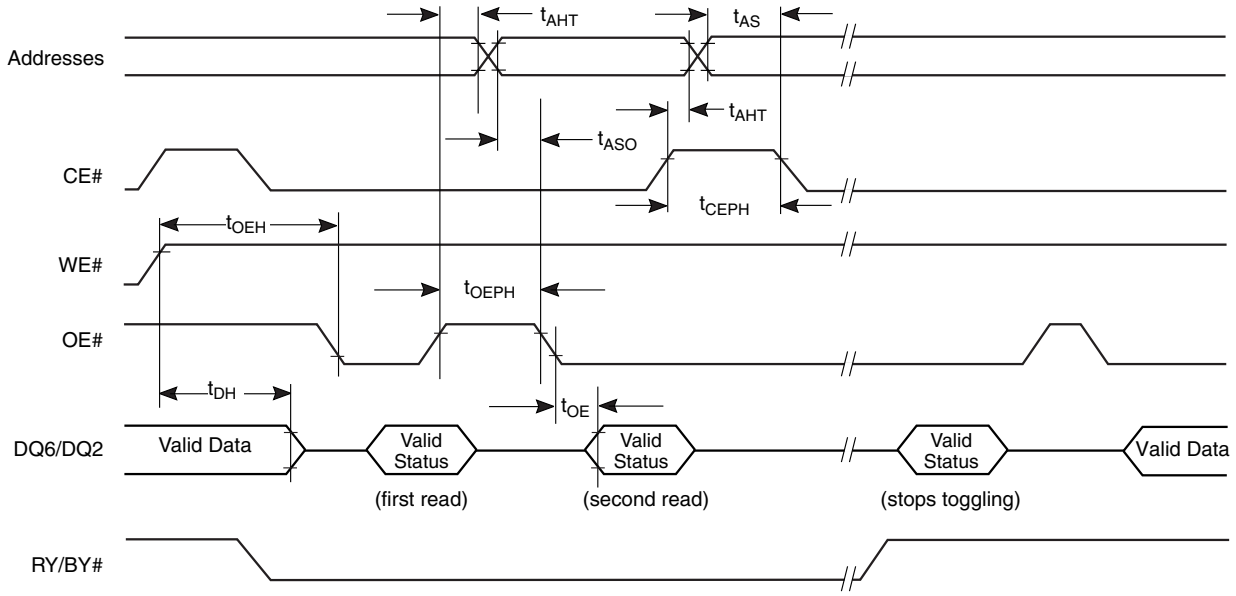
Figure 19. Back-to-Back Read/Write Cycle Timings



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

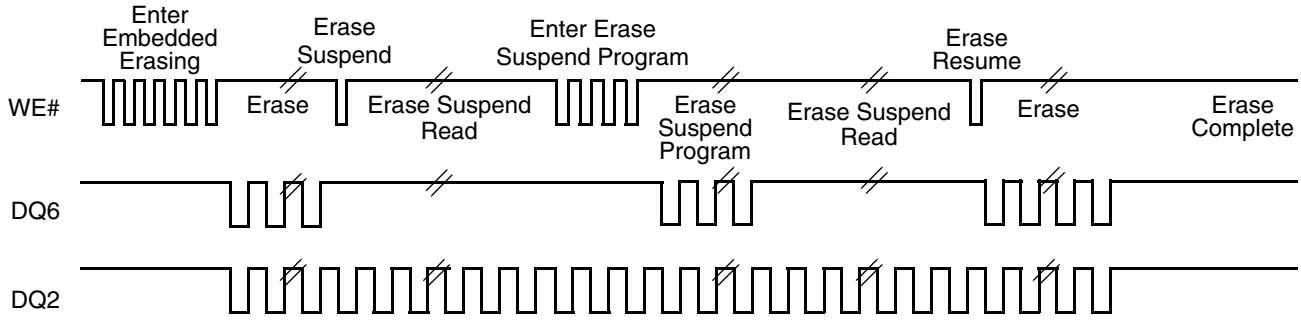
Figure 20. Data# Polling Timings (During Embedded Algorithms)

AC CHARACTERISTICS



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle*

Figure 21. Toggle Bit Timings (During Embedded Algorithms)



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

Figure 22. DQ2 vs. DQ6

AC CHARACTERISTICS

Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs
	t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect	Min	4	µs

Note: *Not 100% tested.*

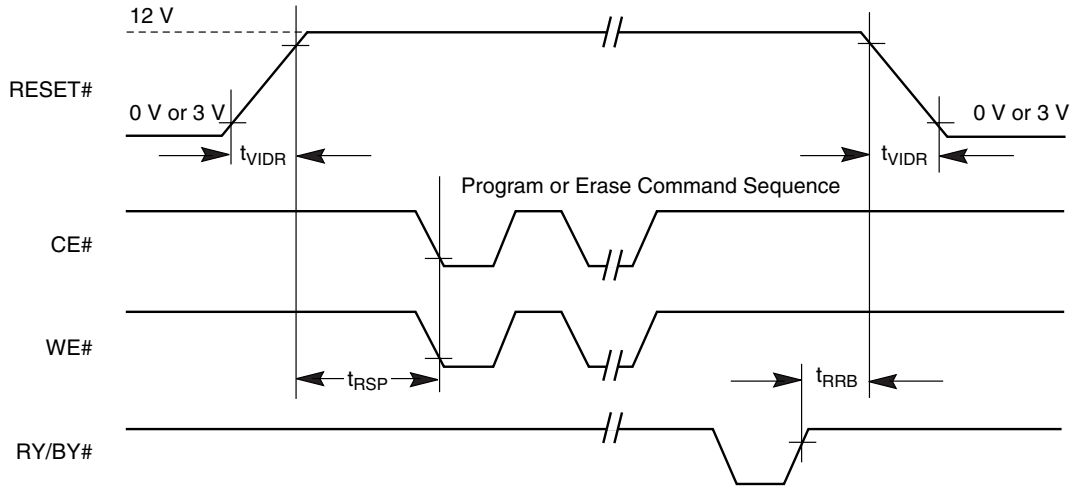
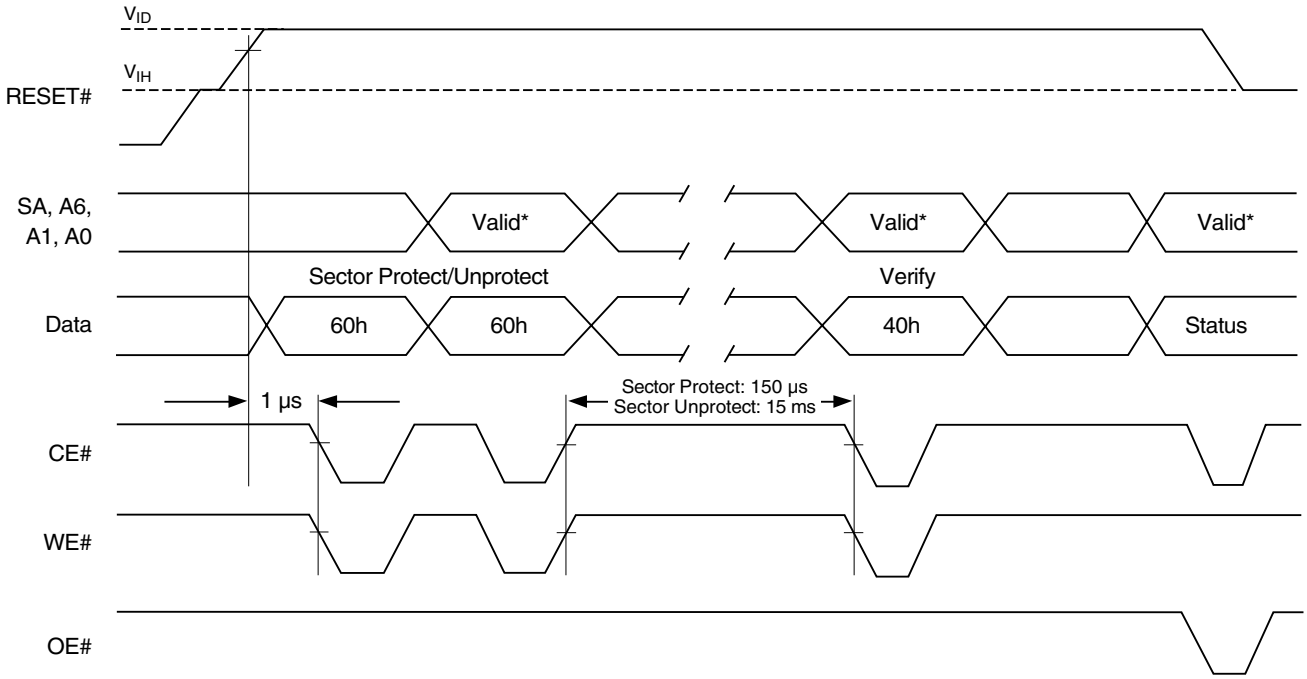


Figure 23. Temporary Sector Unprotect Timing Diagram



* *For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.*

Figure 24. Sector Protect/Unprotect Timing Diagram

AC CHARACTERISTICS

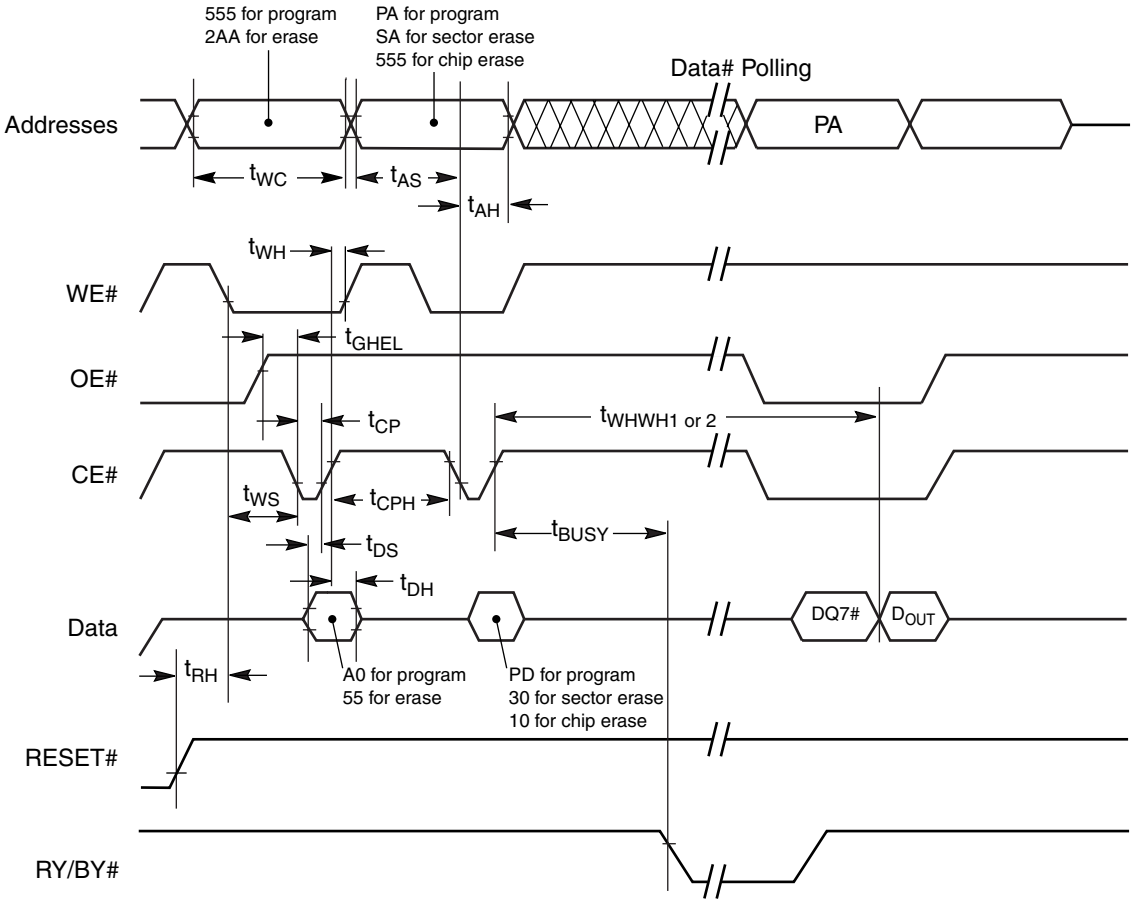
Alternate CE# Controlled Erase/Program Operations

Parameter								
JEDEC	Std	Description			70	90	120	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0			ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	35	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0			ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0			ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0			ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0			ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	35	35	50	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30			ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	9			µs
			Word	Typ	11			
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.7			sec

Notes:

1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*

AC CHARACTERISTICS



Notes:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data, DQ7# = complement of the data written to the device, D_{OUT} = data written to the device.*
3. *Waveforms are for the word mode.*

Figure 25. Alternate CE# Controlled Erase/Program Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.7	15	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time		14		sec	
Byte Program Time		9	300	µs	Excludes system level overhead (Note 5)
Word Program Time		11	360	µs	
Chip Program Time (Note 3)	Byte Mode	9	27	sec	
	Word Mode	5.8	17		

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 2.7 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 5 for further information on command definitions.*
6. *The device has a guaranteed minimum erase and program cycle endurance of 1,000,000 cycles.*

LATCHUP CHARACTERISTICS

	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.

TSOP AND SO PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

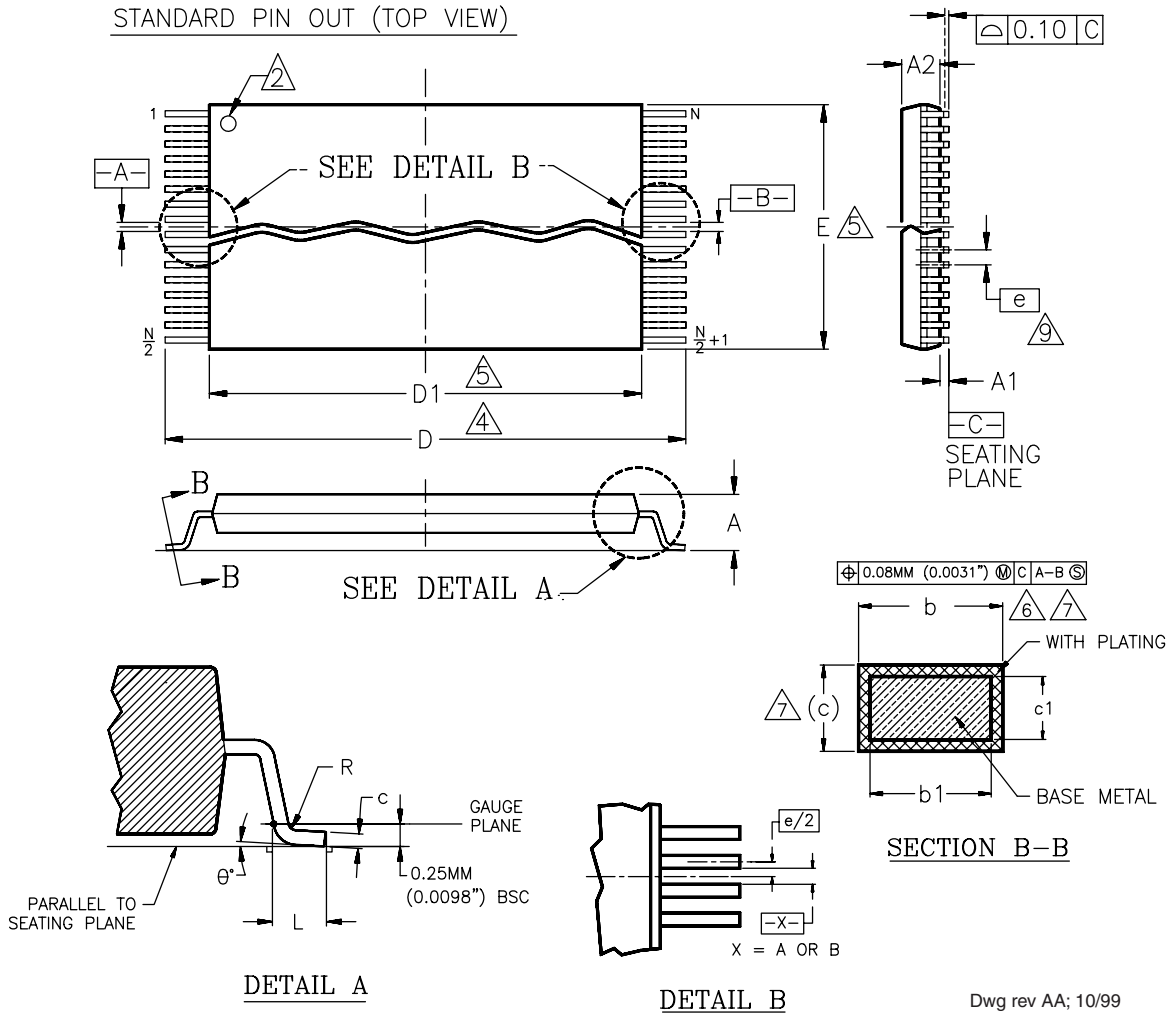
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

PHYSICAL DIMENSIONS

TS 048—48-Pin Standard TSOP



Package	TS 48		
Jedec	MO-142 (B) DD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	48		

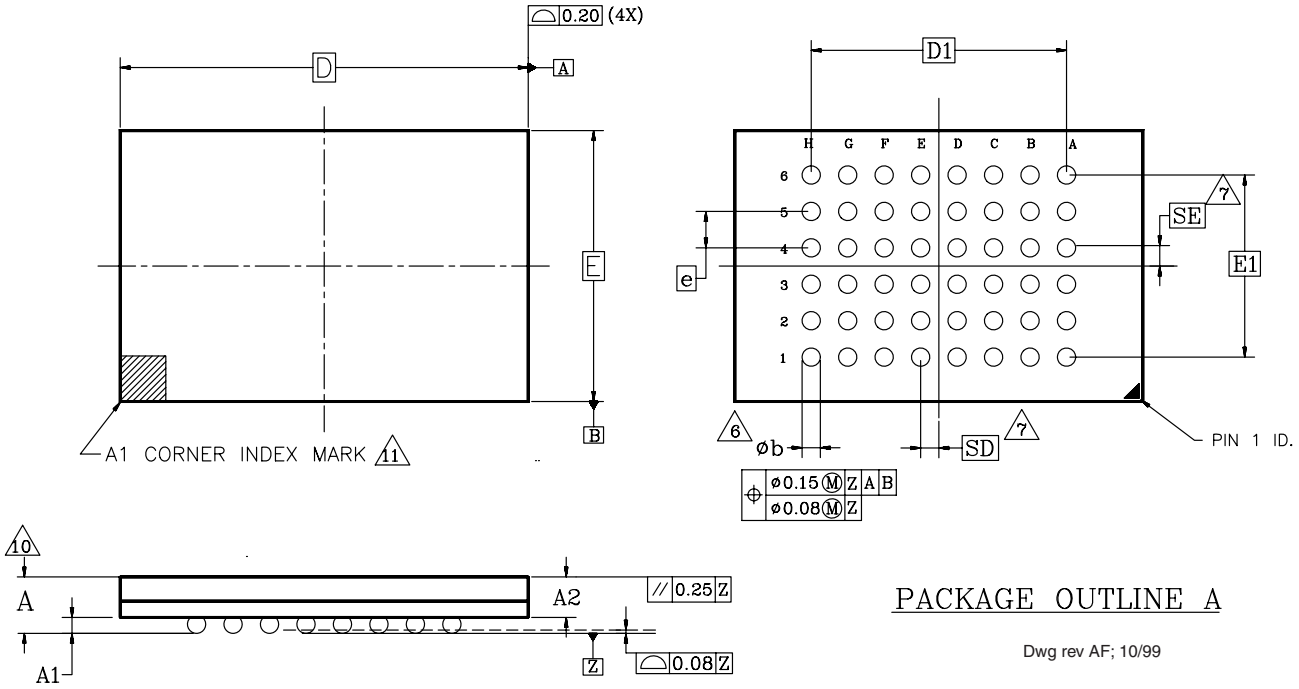
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

** For reference only. BSC is an ANSI standard for Basic Space Centering*

PHYSICAL DIMENSIONS (continued)

FBB048 —48-Ball Fine-Pitch Ball Grid Array (FBGA), 6 x 9 mm package



PACKAGE OUTLINE A

Dwg rev AF; 10/99

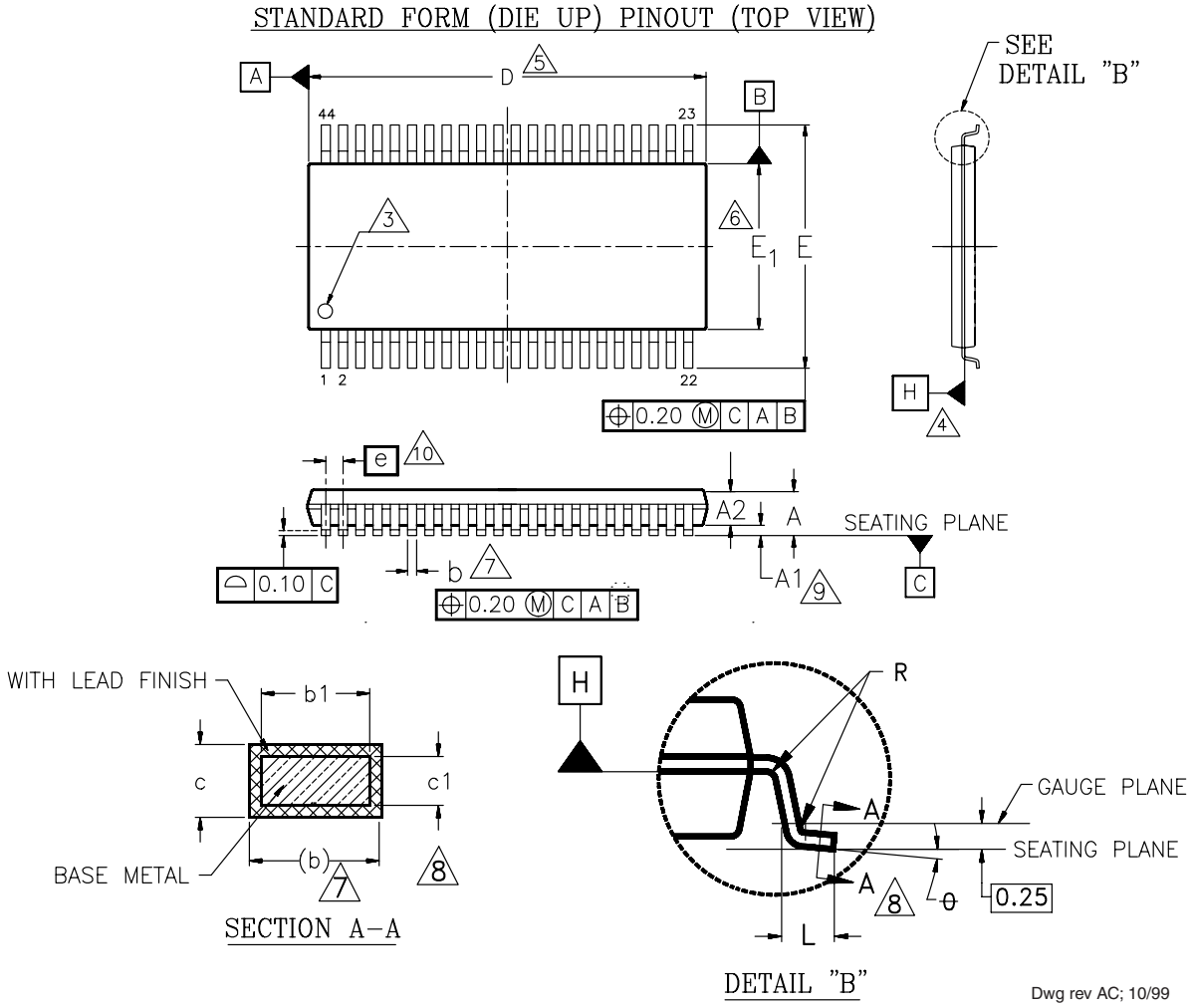
PACKAGE	xFBB 048			
JEDEC	N/A			
	6.00mmx9.00mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	OVERALL THICKNESS
A1	0.20	—	—	BALL HEIGHT
A2	0.84	—	0.94	BODY THICKNESS
D	9.00 BSC			BODY SIZE
E	6.00 BSC			BODY SIZE
D1	5.60 BSC			BALL FOOTPRINT
E1	4.00 BSC			BALL FOOTPRINT
MD	8			ROW MATRIX SIZE D DIRECTION
ME	6			ROW MATRIX SIZE E DIRECTION
N	48			TOTAL BALL COUNT
b	0.25	0.30	0.35	BALL DIAMETER
e	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC			SOLDER BALL PLACEMENT

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION. N IS THE MAXIMUM NUMBER OF SOLDER BALLS FOR MATRIX SIZE MD x ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM Z.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000 WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
9. "+" IN THE PACKAGE DRAWING INDICATE THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. FOR PACKAGE THICKNESS A IS THE CONTROLING DIMENSION.
11. A1 CORNER TO BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKINGS INDENTION OR OTHER MEANS.

PHYSICAL DIMENSIONS (continued)

SO 044—44-Pin Small Outline



PACKAGE	SO 044		
JEDEC	MO–180 (A) AA		
SYMBOL	MIN	NOM	MAX
A	—	—	2.80
A1	0.15	0.23	0.35
A2	2.17	2.30	2.45
b	0.35	—	0.50
b1	0.35	0.40	0.45
c	0.10	—	0.21
c1	0.10	0.15	0.18
D	28.00	28.20	28.40
E	15.70	16.00	16.30
E1	13.10	13.30	13.50
e	1.27 BSC		
L	0.60	0.80	1.00
R	0.09	—	—
θ	0°	4°	8°

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm).
2. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994.
3. PIN 1 IDENTIFIER FOR STANDARD FORM (DIE UP) OR REVERSE FORM (DIE DOWN) PINOUTS.
4. DATUMS A AND B AND DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTUSIONS OR GATE BURRS. MOLD FLASH. PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END.
6. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT EXCEED 0.15 mm PER SIDE. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.07 mm AT LEAST MATERIAL CONDITION.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIPS.
9. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE.
10. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
11. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THER SEATING PLANE.

REVISION SUMMARY

Revision A (January 1998)

Initial release.

Revision A+1 (January 1998)

Reset Command

Deleted last paragraph in section, which applied to RESET#, not the reset command.

Revision A+2 (Febrauary 1998)

Hardware Reset (RESET#)

Added note to table, fixed references to note.

Revision A+3 (April 1998)

Global

Removed references to the 80 ns speed option.

Changed the 70R ns (V_{CC} ± 5%) speed option to the 70 ns (V_{CC} ± 10%) speed option.

Figure 2, In-System Sector Protect/Unprotect Algorithms

In the sector protect algorithm, added a "Reset PLSCNT=1" box in the path from "Protect another sector?" back to setting up the next sector address.

DQ6: Toggle Bit I

In the first and second paragraphs, clarified that the toggle bit may be read "at any address within the programming or erasing bank," not "at any address." In the fourth paragraph, clarified "device" to "bank."

DC Characteristics

Added reference to Note 4 on I_{CC6} and I_{CC7} specifications.

AC Characteristics

Erase/Program Operations; Alternate CE# Controlled Erase/Program Operations: Corrected the notes reference for t_{WHWH1} and t_{WHWH2}. These parameters are 100% tested. Corrected the note reference for t_{VCS}. This parameter is not 100% tested.

Temporary Sector Unprotect Table

Added note reference for t_{VIDR}. This parameter is not 100% tested.

Figure 24, Sector Protect/Unprotect Timing Diagram

A valid address is not required for the first write cycle; only the data 60h.

Erase and Programming Performance

In Note 2, the worst case endurance is now 1 million cycles.

Revision A+4 (August 1998)

Ordering Information

Corrected description for E and F package type designators to 48-pin TSOP.

AC Characteristics

Read Operations: Corrected t_{RC}, t_{ACC}, t_{CE} for 90 ns speed option.

Figure 24, Sector Protection/Unprotection Timing Diagram

Changed timing parameters to match those in Figure 2.

Revision B (January 1999)

Connection Diagrams

Changed FBGA drawing to top view.

Ordering Information

Changed FBGA package reference to FBB048. Added FBGA package markings to valid combinations table.

Revision B+1 (February 1999)

Physical Dimensions

Corrected ball grid layout on FBB048.

Revision B+2 (July 2, 1999)

Test Conditions

Test Specifications table: Corrected to indicate that the 70 ns speed is tested at 30 pF loading.

Revision C (December 7, 1999)

AC Characteristics—Figure 17. Program Operations Timing and Figure 18. Chip/Sector Erase Operations

Deleted t_{GHWL} and changed OE# waveform to start at high.

Physical Dimensions

Replaced figures with more detailed illustrations.

Revision C+1 (November 21, 2000)

Global

Added table of contents.

Ordering Information

Deleted burn-in option.

Revision C+2 (June 7, 2000)

Ordering Information

Added Pb-Free OPNs.

Revision C+3 (January 5, 2006)

Global

Removed TSR048 48-pin Reverse TSOP option.

Revision C4 (December 4, 2006)

Erase and Program Operations table

Changed t_{BUSY} to a maximum specification.

Revision C5 (February 26, 2009)

Global

Added obsolescence information.

Colophon

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