16-Bit, 1 MSPS PulSAR ADC in MSOP

Enhanced Product

AD7980-EP

FEATURES

- 16-bit resolution with no missing codes
- Throughput: 1 MSPS
- Low power dissipation
  - 4 mW at 1 MSPS (VDD only)
  - 7 mW at 1 MSPS (total)
  - 70 µW at 10 kSPS
- INL: ±0.6 LSB typical, ±1.5 LSB maximum
- SINAD: 91 dB @ 10 kHz
- THD: −114 dB @ 10 kHz
- Pseudo differential analog input range
  - 0 V to V_{REF} with V_{REF} between 2.5 V to 5.5 V
- No pipeline delay
- Single-supply 2.5 V operation with 1.8 V/2.5 V/3 V/5 V logic interface
- Proprietary serial interface
  - SPI/QSPI/MICROWIRE™/DSP compatible
- Daisy-chain multiple ADCs and busy indicator
- Supports defense and aerospace applications (AQEC)
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request
- 10-lead MSOP
- Military temperature range: −55°C to +125°C

APPLICATIONS

- Battery-powered equipment
- Communications
- ATE
- Data acquisitions
- Medical instruments

APPLICATION DIAGRAM EXAMPLE

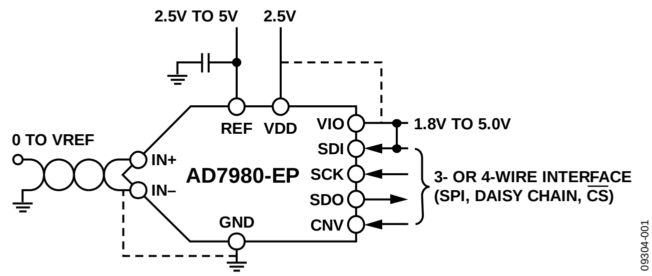

Figure 1.

GENERAL DESCRIPTION

The AD7980-EP[1] is a 16-bit, successive approximation, analog-to-digital converter (ADC) that operates from a single power supply, VDD. It contains a low power, high speed, 16-bit sampling ADC and a versatile serial interface port. On the CNV rising edge, it samples an analog input IN+ between 0 V to REF with respect to a ground sense IN−. The reference voltage, REF, is applied externally and can be set independent of the supply voltage, VDD. Its power scales linearly with throughput.

The SPI-compatible serial interface also features the ability, using the SDI input, to daisy-chain several ADCs on a single, 3-wire bus and provides an optional busy indicator. It is compatible with 1.8 V, 2.5 V, 3 V, or 5 V logic, using the separate supply VIO.

The AD7980-EP is housed in a 10-lead MSOP with operation specified from −55°C to +125°C.

[1] Protected by U.S. Patent 6,703,961.

Table 1. MSOP, LFCSP 14-/16-/18-Bit PulSAR® ADC

Type	100 kSPS	250 kSPS	400 kSPS to 500 kSPS	≥1000 kSPS
18-Bit	AD7989-1[1]	AD7691[1]	AD7690[1]	AD7982[1]
			AD7989-5[1]	AD7984[1]
16-Bit	AD7680	AD7685[1]	AD7686[1]	AD7980[1]
	AD7683	AD7687[1]	AD7688[1]	AD7983[1]
	AD7684	AD7694	AD7693[1]	
	AD7988-1[1]		AD7988-5[1]	
14-Bit	AD7940	AD7942[1]	AD7946[1]	

[1] Pin-for-pin compatible.

Rev. A Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

7/15—Rev. 0 to Rev. A

Changes to Product Title, Features Section, and Table 1 ... 1
Added Patent Note, Note 1 ... 1
Changes to Table 2 ... 3
Changes to Table 3 ... 4
Changes to Table 6 ... 7
Changes to Figure 11, Figure 12, Figure 14, Figure 15 ... 9
Changes to Figure 17, Figure 20, Figure 21 ... 10
Changes to Ordering Guide ... 12

9/10—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.5 V, VIO = 2.3 V to 5.5 V, V_{REF} = 5 V, T_A = −55°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	IN+ − IN−	0		V_{REF}	V
Absolute Input Voltage	IN+	−0.1		V_{REF} + 0.1	V
	IN−	−0.1		+0.1	V
Analog Input CMRR	f_{IN} = 100 kHz		60		dB
Leakage Current @ 25°C	Acquisition phase		1		nA
ACCURACY					
No Missing Codes		16			Bits
Differential Linearity Error	REF = 5 V	−0.9	±0.4	+0.9	LSB[1]
	REF = 2.5 V		±0.55		LSB[1]
Integral Linearity Error	REF = 5 V	−1.5	±0.6	+1.5	LSB[1]
	REF = 2.5 V		±0.65		LSB[1]
Transition Noise	REF = 5 V		0.6		LSB[1]
	REF = 2.5 V		1.0		LSB[1]
Gain Error, T_{MIN} to T_{MAX}[2]			±2		LSB[1]
Gain Error Temperature Drift			±0.35		ppm/°C
Zero Error, T_{MIN} to T_{MAX}[2]		−0.62	±0.08	+0.62	mV
Zero Temperature Drift			0.54		ppm/°C
Power Supply Sensitivity	VDD = 2.5 V ± 5%		±0.1		LSB[1]
THROUGHPUT					
Conversion Rate	VIO ≥ 2.3 V up to 85°C, VIO ≥ 3.3 V above 85°C up to 125°C	0		1	MSPS
Transient Response	Full-scale step			290	ns
AC ACCURACY					
Dynamic Range	V_{REF} = 5 V		92		dB[3]
	V_{REF} = 2.5 V		87		dB[3]
Oversampled Dynamic Range	f_O = 10 kSPS		111		dB[3]
Signal-to-Noise Ratio, SNR	f_{IN} = 10 kHz, V_{REF} = 5 V		91.5		dB[3]
	f_{IN} = 10 kHz, V_{REF} = 2.5 V		87		dB[3]
Spurious-Free Dynamic Range, SFDR	f_{IN} = 10 kHz		−110		dB[3]
Total Harmonic Distortion, THD	f_{IN} = 10 kHz		−114		dB[3]
Signal-to-(Noise + Distortion), SINAD	f_{IN} = 10 kHz, V_{REF} = 5 V		91		dB[3]
	f_{IN} = 10 kHz, V_{REF} = 2.5 V		86.5		dB[3]

[1] LSB means least significant bit. With the 5 V input range, 1 LSB is 76.3 µV.
[2] These specifications include full temperature range variation, but not the error contribution from the external reference.
[3] All specifications in dB are referred to a full-scale input FSR. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

VDD = 2.5 V, VIO = 2.3 V to 5.5 V, V_{REF} = 5 V, T_A = −55°C to +125°C, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
REFERENCE					
Voltage Range		2.4		5.1	V
Load Current	1 MSPS, REF = 5 V		330		µA
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			10		MHz
Aperture Delay	VDD = 2.5 V		2.0		ns
DIGITAL INPUTS					
Logic Levels					
V_{IL}	VIO > 3V	−0.3		0.3 × VIO	V
V_{IH}	VIO > 3V	0.7 × VIO		VIO + 0.3	V
V_{IL}	VIO ≤ 3V	−0.3		0.1 × VIO	
V_{IH}	VIO ≤ 3V	0.9 × VIO		VIO + 0.3	µA
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format		Serial 16 bits straight binary			
Pipeline Delay		Conversion results available immediately after completed conversion			
V_{OL}	I_{SINK} = 500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD		2.375	2.5	2.625	V
VIO	Specified performance	2.3		5.5	V
VIO Range		1.8		5.5	V
Standby Current[1, 2]	VDD and VIO = 2.5 V, 25°C		0.35		µA
Power Dissipation	VDD = 2.625 V, V_{REF} = 5 V, VIO = 3 V				
Total	10 kSPS throughput		70		µW
	1 MSPS throughput		7.0	10	mW
VDD Only			4		mW
REF Only			1.7		mW
VIO Only			1.3		mW
Energy per Conversion			7.0		nJ/sample
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−55		+125	°C

[1] With all digital inputs forced to VIO or GND as required.
[2] During the acquisition phase.

TIMING SPECIFICATIONS

−55°C to +125°C, VDD = 2.37 V to 2.63 V, VIO = 3.3 V to 5.5 V, unless otherwise stated. See Figure 2 and Figure 3 for load conditions.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	500		710	ns
Acquisition Time	t_{ACQ}	290			ns
Time Between Conversions	t_{CYC}	1000			ns
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	10			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}				ns
VIO Above 4.5 V		10.5			ns
VIO Above 3 V		12			ns
VIO Above 2.7 V		13			ns
VIO Above 2.3 V		15			ns
SCK Period (Chain Mode)	t_{SCK}				ns
VIO Above 4.5 V		11.5			ns
VIO Above 3 V		13			ns
VIO Above 2.7 V		14			ns
VIO Above 2.3 V		16			ns
SCK Low Time	t_{SCKL}	4.5			ns
SCK High Time	t_{SCKH}	4.5			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	3			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 4.5 V				9.5	ns
VIO Above 3 V				11	ns
VIO Above 2.7 V				12	ns
VIO Above 2.3 V				14	ns
CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}				
VIO Above 3 V				10	ns
VIO Above 2.3 V				15	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			20	ns
SDI Valid Setup Time from CNV Rising Edge	$t_{SSDICNV}$	5			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	2			ns
SDI Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	5			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	2			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	3			ns
SDI High to SDO High (Chain Mode with Busy Indicator)	$t_{DSDOSDI}$			15	ns

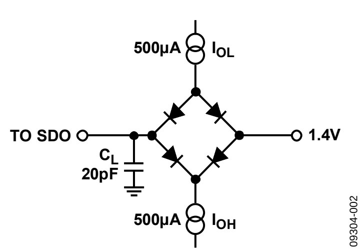

Figure 2. Load Circuit for Digital Interface Timing

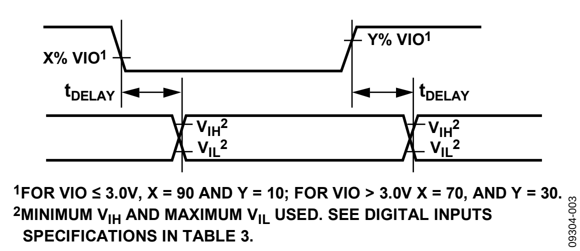

Figure 3. Voltage Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Inputs	
IN+, IN− to GND	−0.3 V to V_{REF} + 0.3 V or ±130 mA
Supply Voltage	
REF, VIO to GND	−0.3 V to +6 V
VDD to GND	−0.3 V to +3 V
VDD to VIO	+3 V to −6 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (10-Lead MSOP)	200°C/W
θ_{JC} Thermal Impedance (10-Lead MSOP)	44°C/W
Lead Temperature	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

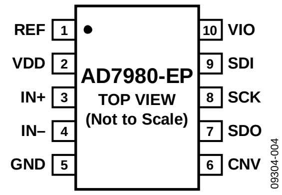

Figure 4. 10-Lead MSOP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	REF	AI	Reference Input Voltage. The REF range is from 2.4 V to 5.1 V. It is referred to the GND pin. This pin should be decoupled closely to the pin with a 10 μF capacitor.
2	VDD	P	Power Supply.
3	IN+	AI	Analog Input. It is referred to IN−. The voltage range, for example, the difference between IN+ and IN−, is 0 V to V_{REF}.
4	IN−	AI	Analog Input Ground Sense. To be connected to the analog ground plane or to a remote sense ground.
5	GND	P	Power Supply Ground.
6	CNV	DI	Convert Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode of the part, chain, or $\overline{CS}$ mode. In $\overline{CS}$ mode, it enables the SDO pin when low. In chain mode, the data should be read when CNV is high.
7	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
8	SCK	DI	Serial Data Clock Input. When the part is selected, the conversion result is shifted out by this clock.
9	SDI	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows. Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low; if SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled.
10	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).

[1]AI = analog input, DI = digital input, DO = digital output, and P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 2.5 V, V_{REF} = 5.0 V, VIO = 3.3 V, unless otherwise noted.

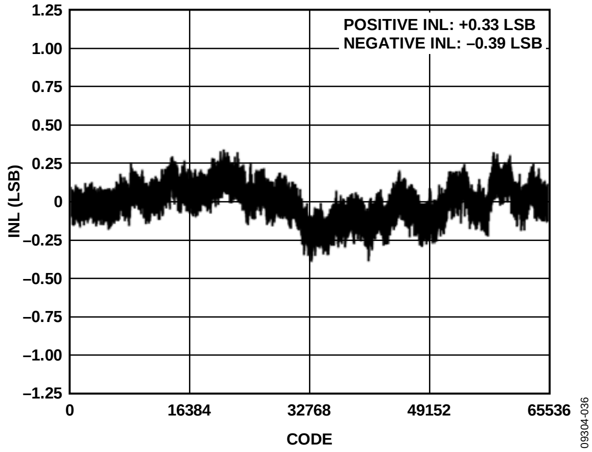

Figure 5. Integral Nonlinearity vs. Code, REF = 5 V

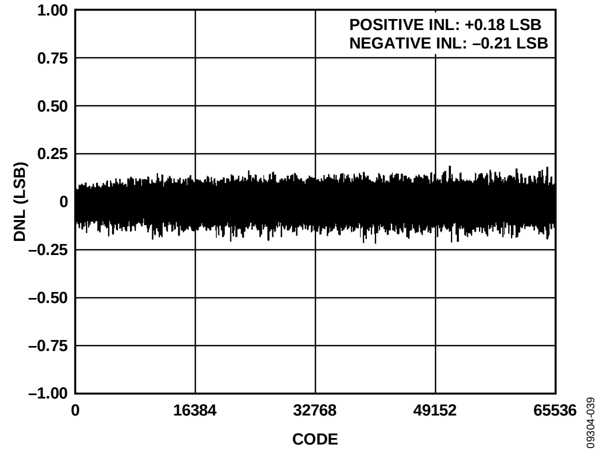

Figure 8. Differential Nonlinearity vs. Code, REF = 5 V

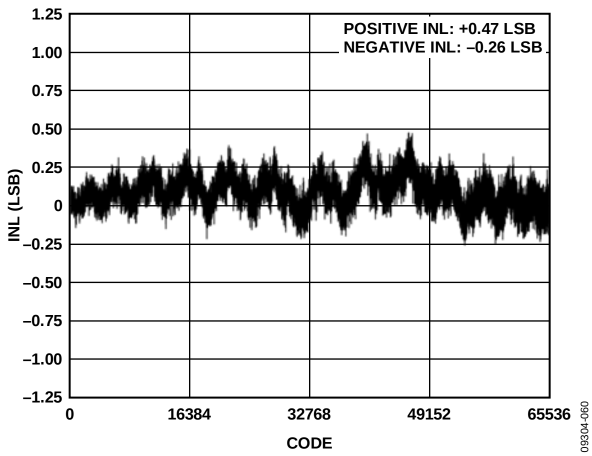

Figure 6. Integral Nonlinearity vs. Code, REF = 2.5 V

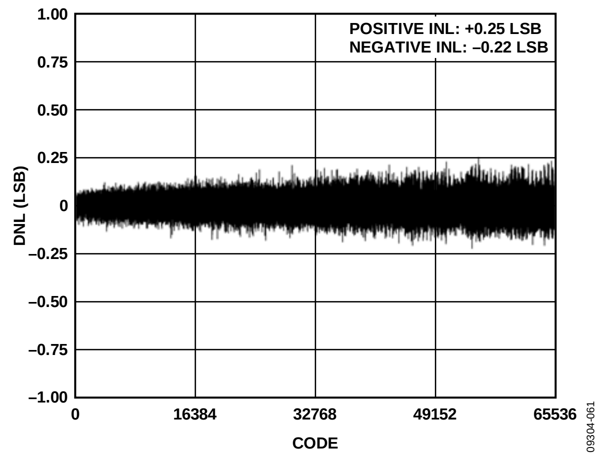

Figure 9. Differential Nonlinearity vs. Code, REF = 2.5 V

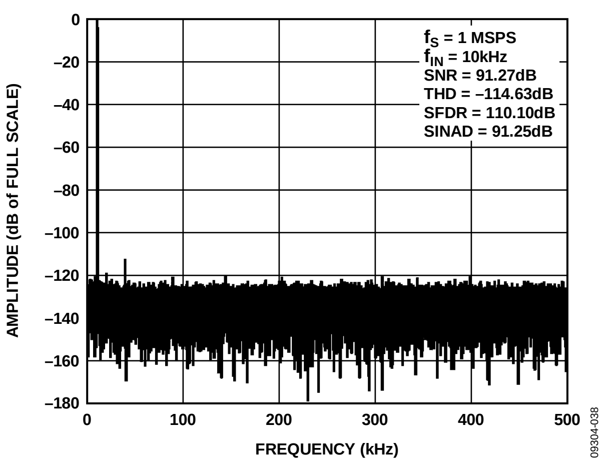

Figure 7. FFT Plot, REF = 5 V

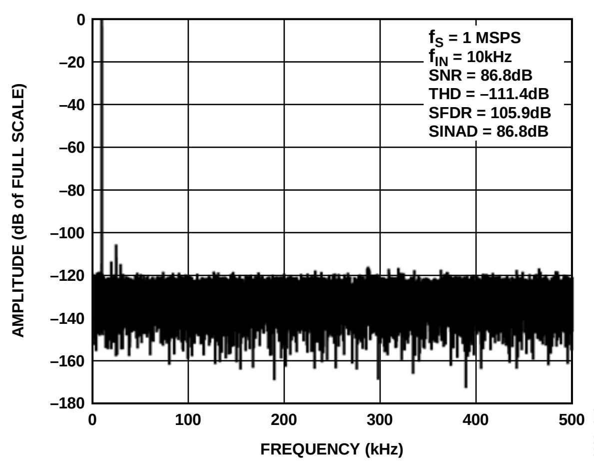

Figure 10. FFT Plot, REF = 2.5 V

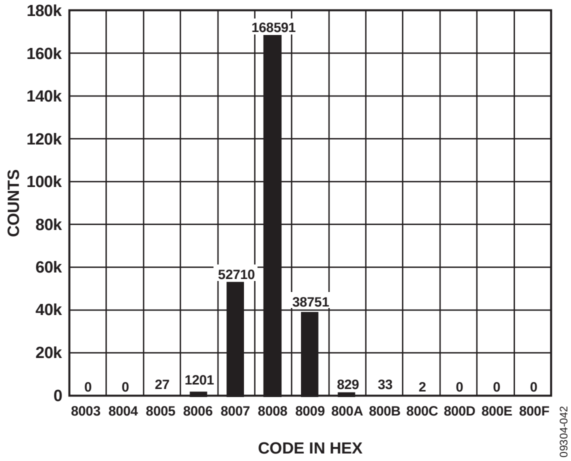

Figure 11. Histogram of a DC Input at the Code Center, REF = 5 V

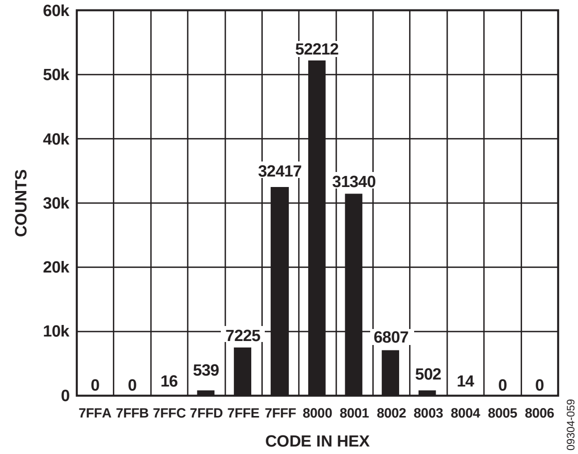

Figure 14. Histogram of a DC Input at the Code Center, REF = 2.5 V

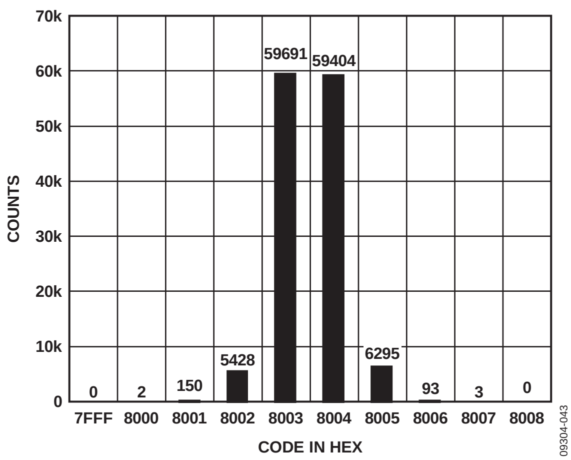

Figure 12. Histogram of a DC Input at the Code Transition, REF = 5 V

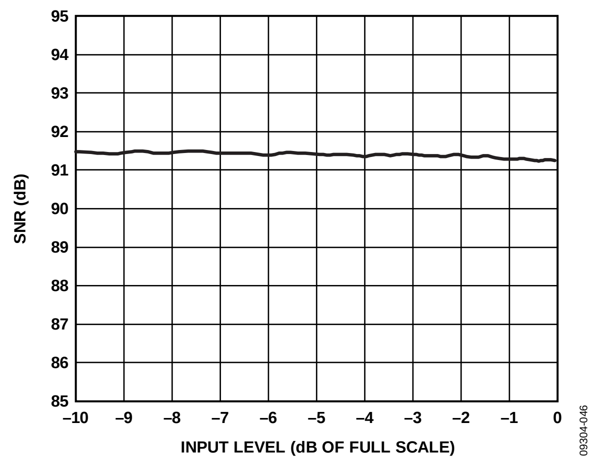

Figure 15. SNR vs. Input Level

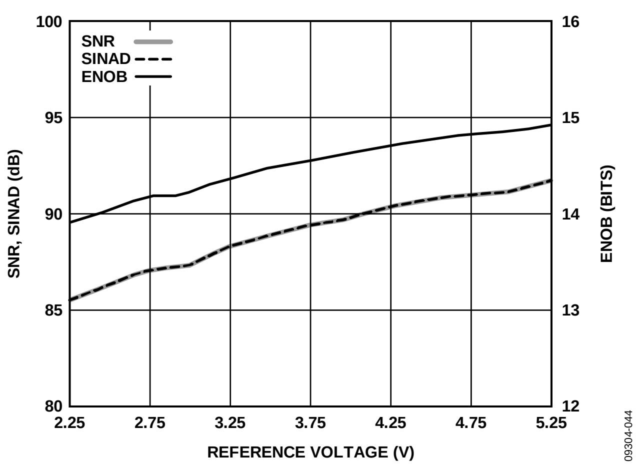

Figure 13. SNR, SINAD, and ENOB vs. Reference Voltage

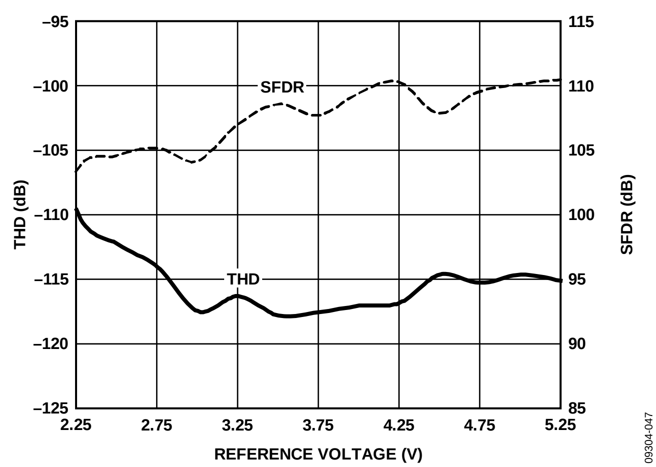

Figure 16. THD, SFDR vs. Reference Voltage

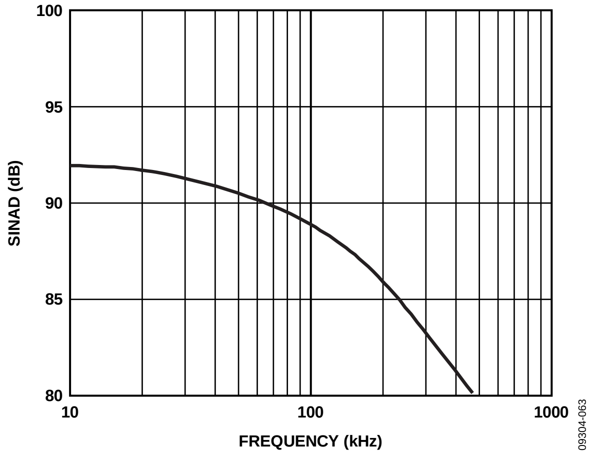

Figure 17. SINAD vs. Frequency

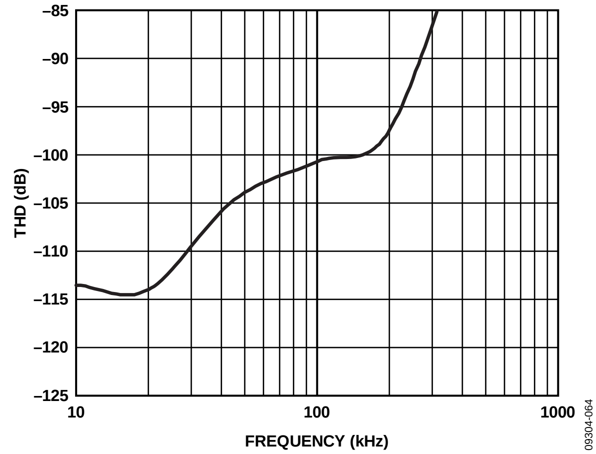

Figure 20. THD vs. Frequency

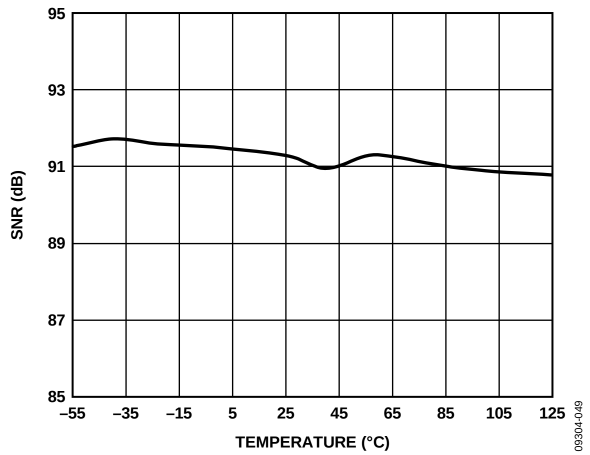

Figure 18. SNR vs. Temperature

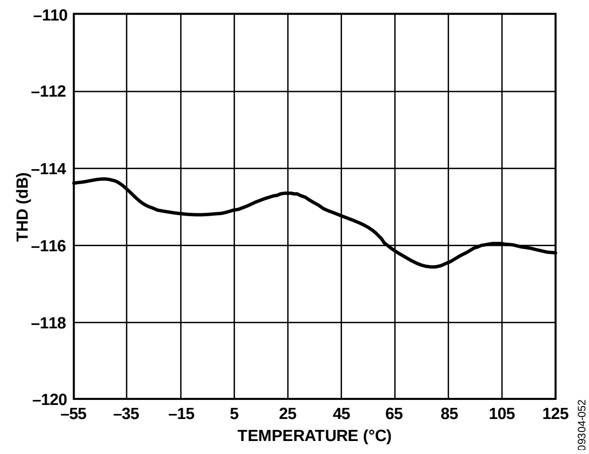

Figure 21. THD vs. Temperature

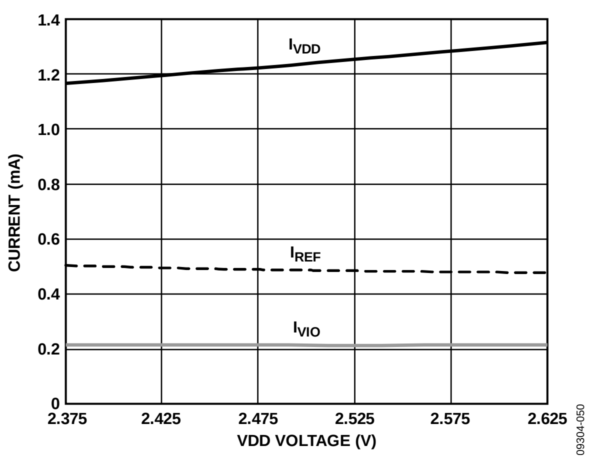

Figure 19. Operating Currents vs. Supply

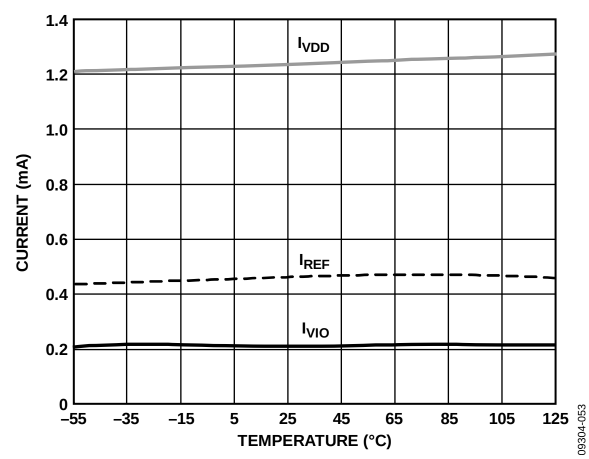

Figure 22. Operating Currents vs. Temperature

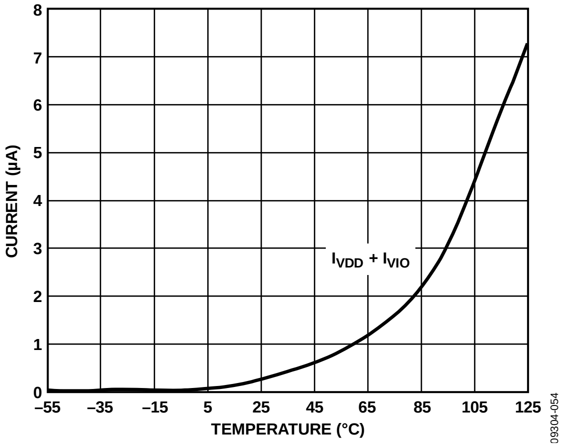

Figure 23. Power-Down Currents vs. Temperature

OUTLINE DIMENSIONS

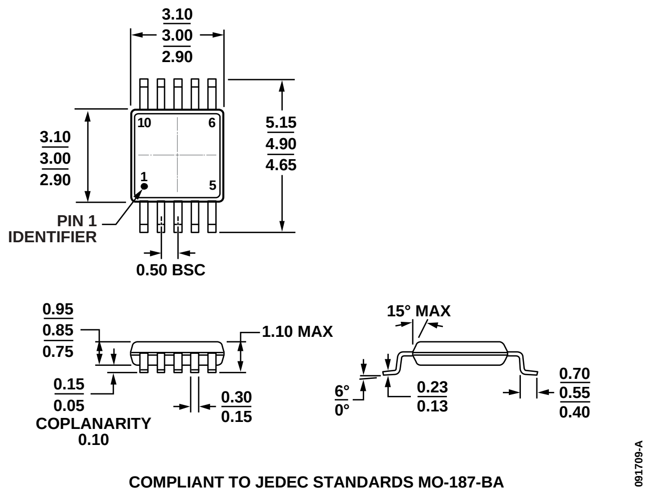

Figure 24.10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Integral Nonlinearity	Temperature Range	Ordering Quantity	Package Description	Package Option	Branding
AD7980SRMZ-EP-RL7	±1.5 LSB max	−55°C to +125°C	Reel, 1,000	10-Lead MSOP	RM-10	C78
AD7980SRMZ-EP	±1.5 LSB max	−55°C to +125°C		10-Lead MSOP	RM-10	C78

[1] Z = RoHS Compliant Part.