12-Bit 310Msps ADC

FEATURES

- 67.6dBFS SNR
- 88dB SFDR
- Low Power: 378mW Total
- Single 1.8V Supply
- DDR LVDS Outputs
- 1.32V_{P-P} Input Range
- 1.25GHz Full Power Bandwidth S/H
- Optional Clock Duty Cycle Stabilizer
- Low Power Sleep and Nap Modes
- Serial SPI Port for Configuration
- Pin-Compatible 12-Bit Versions
- 40-Lead (6mm × 6mm) QFN Package

APPLICATIONS

- Communications
- Cellular Basestations
- Software Defined Radios
- Medical Imaging
- High Definition Video
- Testing and Measurement Instruments

DESCRIPTION

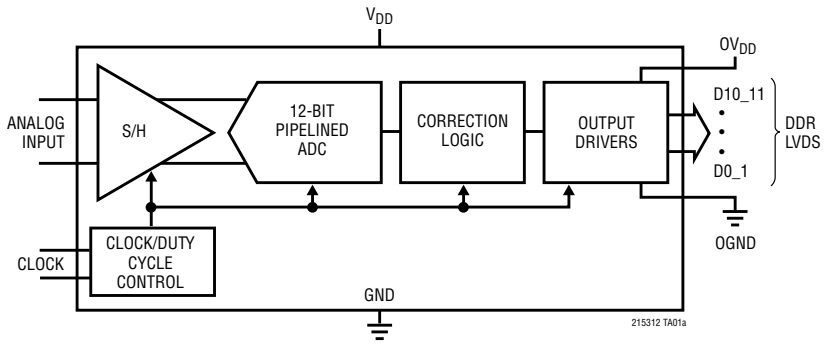
The LTC®2153-12 is a 310Msps 12-bit A/D converter designed for digitizing high frequency, wide dynamic range signals. It is perfect for demanding communications applications with AC performance that includes 67.6dB SNR and 88dB spurious free dynamic range (SFDR). The 1.25GHz input bandwidth allows the ADC to undersample high frequencies with good performance. The latency is only six clock cycles.

DC specs include ±0.6LSB INL (typ), ±0.1LSB DNL (typ) and no missing codes over temperature. The transition noise is 0.6LSB_{RMS}.

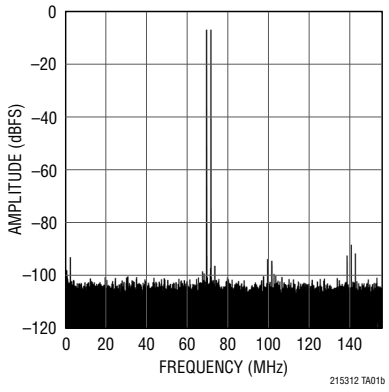
The digital outputs are double data rate (DDR) LVDS.

The ENC^+ and ENC^- inputs can be driven differentially with a sine wave, PECL, LVDS, TTL, or CMOS inputs. An optional clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

TYPICAL APPLICATION



LTC2153-12 32K Point 2-Tone FFT, f_{IN} = 71MHz and 69MHz, 310Msps



ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage
- V_{DD}, OV_{DD} ..... –0.3V to 2V

Analog Input Voltage
- A_{IN}^+, A_{IN}^-, PAR/$\overline{SER}$, SENSE (Note 3) ..... –0.3V to (V_{DD} + 0.2V)

Digital Input Voltage
- ENC^+, ENC^- (Note 3) ..... –0.3V to (V_{DD} + 0.3V)
- $\overline{CS}$, SDI, SCK (Note 4) ..... –0.3V to 3.9V

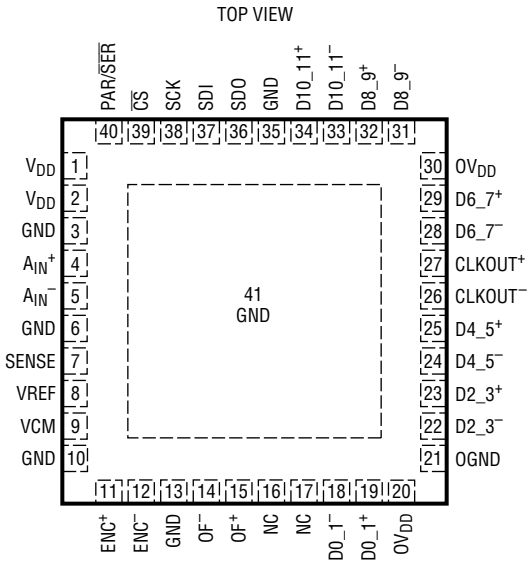
SDO (Note 4) ..... –0.3V to 3.9V

Digital Output Voltage ..... –0.3V to (OV_{DD} + 0.3V)

Operating Temperature Range
- LTC2153C ..... 0°C to 70°C
- LTC2153I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 33°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2153CUJ-12#PBF	LTC2153CUJ-12#TRPBF	LTC2153UJ-12	40-Lead (6mm × 6mm) Plastic QFN	0°C to 70°C
LTC2153IUJ-12#PBF	LTC2153IUJ-12#TRPBF	LTC2153UJ-12	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	Differential Analog Input (Note 6)	●	–1.8	±0.6	1.8	LSB
Differential Linearity Error	Differential Analog Input	●	–0.7	±0.1	0.7	LSB
Offset Error	(Note 7)	●	–12	±5	12	mV
Gain Error	Internal Reference External Reference	 ●	 –4	±1.5 ±1	 3	%FS %FS
Offset Drift				±20		µV/°C
Full-Scale Drift	Internal Reference External Reference			±30 ±10		ppm/°C ppm/°C
Transition Noise				0.6		LSB_{RMS}

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range ($A_{IN}^+ - A_{IN}^-$)	1.74V < V_{DD} < 1.9V			1.32		V_{P-P}
$V_{IN(CM)}$	Analog Input Common Mode ($A_{IN}^+ + A_{IN}^-$)/2	Differential Analog Input (Note 8)	●	V_{CM} – 20mV	V_{CM}	V_{CM} + 20mV	V
V_{SENSE}	External Voltage Reference Applied to SENSE	External Reference Mode	●	1.230	1.250	1.270	V
I_{IN1}	Analog Input Leakage Current	0 < A_{IN}^+, A_{IN}^- < V_{DD}, No Encode	●	–1		1	µA
I_{IN2}	PAR/$\overline{SER}$ Input Leakage Current	0 < PAR/$\overline{SER}$ < V_{DD}	●	–1		1	µA
I_{IN3}	SENSE Input Leakage Current	1.23V < SENSE < 1.27V	●	–1		1	µA
t_{AP}	Sample-and-Hold Acquisition Delay Time				1		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Jitter				0.15		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio				75		dB
BW-3B	Full-Power Bandwidth				1250		MHz

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio	15MHz Input 70MHz Input 140MHz Input	 ●	 65.8	67.6 67.1 67.0	 	dBFS dBFS dBFS
SFDR	Spurious Free Dynamic Range 2nd or 3rd Harmonic	15MHz Input 70MHz Input 140MHz Input	 ●	 70	88 85 80	 	dBFS dBFS dBFS
	Spurious Free Dynamic Range 4th Harmonic or Higher	15MHz Input 70MHz Input 140MHz Input	 ●	 80	98 95 90	 	dBFS dBFS dBFS
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	15MHz Input 70MHz Input 140MHz Input	 ●	 65	67.1 67.0 66.9	 	dBFS dBFS dBFS

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	I_{OUT} = 0		0.439 • V_{DD} – 18mV	0.439 • V_{DD}	0.439 • V_{DD} + 18mV	V
V_{CM} Output Temperature Drift				±37		ppm/°C
V_{CM} Output Resistance	–1mA < I_{OUT} < 1mA			4		Ω
V_{REF} Output Voltage	I_{OUT} = 0		1.225	1.250	1.275	V
V_{REF} Output Temperature Drift				±30		ppm/°C
V_{REF} Output Resistance	–400µA < I_{OUT} < 1mA			7		Ω
V_{REF} Line Regulation	1.74V < V_{DD} < 1.9V			0.6		mV/V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Analog Supply Voltage	(Note 9)	●	1.74	1.8	1.9	V
OV_{DD}	Output Supply Voltage	(Note 9)	●	1.74	1.8	1.9	V
I_{VDD}	Analog Supply Current		●		182	205	mA
I_{OVDD}	Digital Supply Current	1.75mA LVDS Mode 3.5mA LVDS Mode	● ●		28 48.5	34 52	mA mA
P_{DISS}	Power Dissipation	1.75mA LVDS Mode 3.5mA LVDS Mode	● ●		378 415	430 463	mW mW
P_{SLEEP}	Sleep Mode Power	Clock Disabled Clocked at $f_{S(MAX)}$			<5 <5		mW mW
P_{NAP}	Nap Mode Power	Clocked at $f_{S(MAX)}$			124		mW

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ENCODE INPUTS (ENC+, ENC–)							
V_{ID}	Differential Input Voltage	(Note 8)	●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set Externally Set (Note 8)	 ●	 1.1	1.2	 1.5	V V
R_{IN}	Input Resistance	(See Figure 2)			10		kΩ
C_{IN}	Input Capacitance	(Note 8)			2		pF
DIGITAL INPUTS ($\overline{CS}$, SDI, SCK)							
V_{IH}	High Level Input Voltage	V_{DD} = 1.8V	●	1.3			V
V_{IL}	Low Level Input Voltage	V_{DD} = 1.8V	●			0.6	V
I_{IN}	Input Current	V_{IN} = 0V to 3.6V	●	–10		10	µA
C_{IN}	Input Capacitance	(Note 8)			3		pF
SDO OUTPUT (Open-Drain Output. Requires 2k Pull-Up Resistor if SDO Is Used)							
R_{OL}	Logic Low Output Resistance to GND	V_{DD} = 1.8V, SDO = 0V			200		Ω
I_{OH}	Logic High Output Leakage Current	SDO = 0V to 3.6V	●	–10		10	µA
C_{OUT}	Output Capacitance	(Note 8)			4		pF

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL DATA OUTPUTS							
V_{OD}	Differential Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	● ●	247 125	350 175	454 250	mV mV
V_{OS}	Common Mode Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	● ●	1.125 1.125	1.250 1.250	1.375 1.375	V V
R_{TERM}	On-Chip Termination Resistance	Termination Enabled, OV_{DD} = 1.8V			100		Ω

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_S	Sampling Frequency	(Note 9)	●	10		310	MHz
t_L	ENC Low Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	1.5 1.2	1.61 1.61	50 50	ns ns
t_H	ENC High Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	1.5 1.2	1.61 1.61	50 50	ns ns
DIGITAL DATA OUTPUTS							
				MIN	TYP	MAX	UNITS
t_D	ENC to Data Delay	C_L = 5pF (Note 8)	●	1.7	2	2.3	ns
t_C	ENC to CLKOUT Delay	C_L = 5pF (Note 8)	●	1.3	1.6	2	ns
t_{SKEW}	DATA to CLKOUT Skew	$t_D - t_C$ (Note 8)	●	0.3	0.4	0.55	ns
	Pipeline Latency			6		6	Cycles
SPI Port Timing (Note 8)							
t_{SCK}	SCK Period	Write Mode Readback Mode C_{SDO}= 20pF, R_{PULLUP} = 2k	● ●	40 250			ns ns
t_S	$\overline{CS}$ to SCK Set-Up Time		●	5			ns
t_H	SCK to $\overline{CS}$ Hold Time		●	5			ns
t_{DS}	SDI Set-Up Time		●	5			ns
t_{DH}	SDI Hold Time		●	5			ns
t_{DO}	SCK Falling to SDO Valid	Readback Mode, C_{SDO} = 20pF, R_{PULLUP} = 2k	●			125	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND with GND and OGND shorted (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below GND they will be clamped by internal diodes. When these pin voltages are taken above V_{DD} they will not be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND without latchup.

Note 5: V_{DD} = OV_{DD} = 1.8V, f_{SAMPLE} = 310MHz, differential ENC^+/ENC^- = $2V_{P-P}$ sine wave, input range = $1.32V_{P-P}$ with differential drive, unless otherwise noted.

Note 6: Integral nonlinearity is defined as the deviation of a code from a best fit straight line to the transfer curve. The deviation is measured from the center of the quantization band.

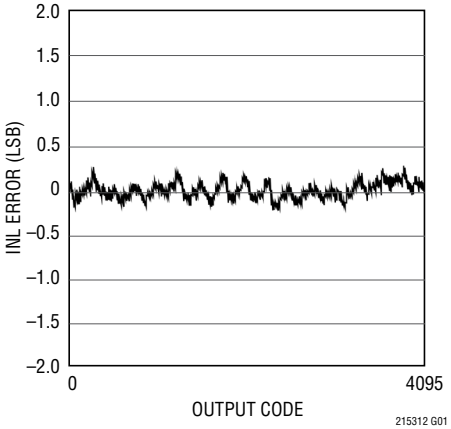
Note 7: Offset error is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111 in 2's complement output mode.

Note 8: Guaranteed by design, not subject to test.

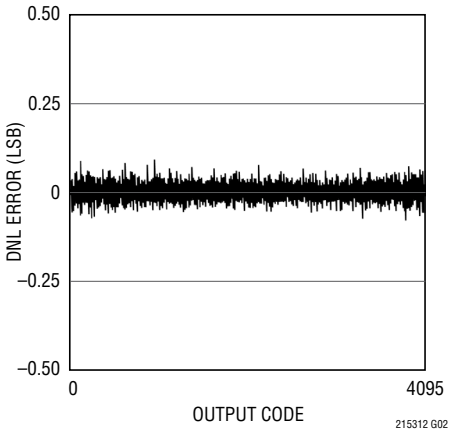
Note 9: Recommended operating conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

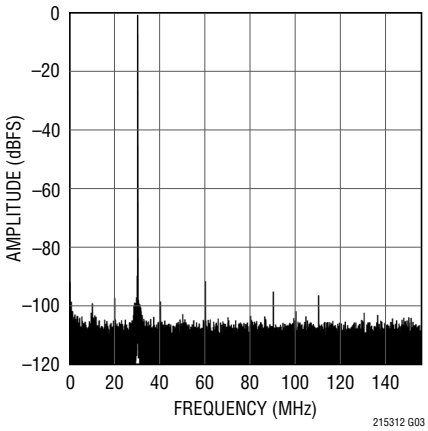
LTC2153-12: Integral Nonlinearity (INL)



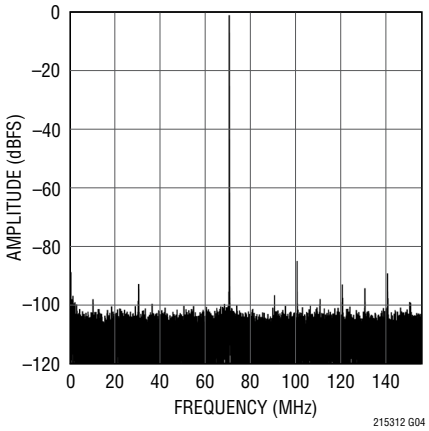
LTC2153-12: Differential Nonlinearity (DNL)



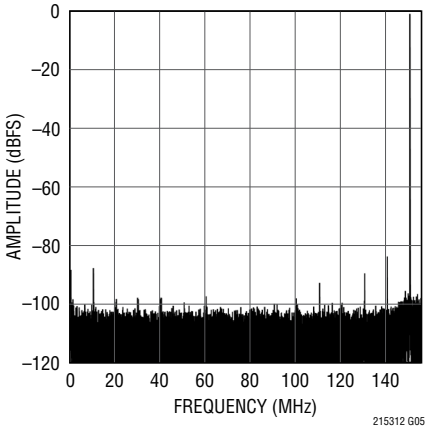
LTC2153-12: 32K Point FFT, f_{IN} = 15MHz, –1dBFS, 310Msps



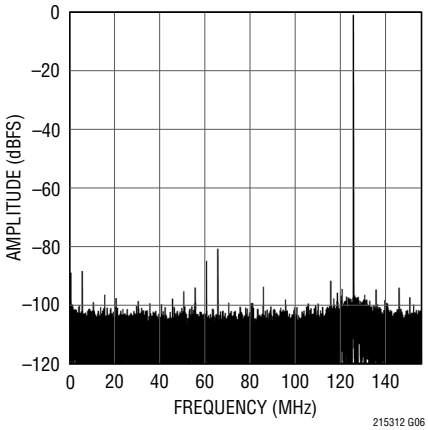
LTC2153-12: 32K Point FFT, f_{IN} = 70MHz, –1dBFS, 310Msps



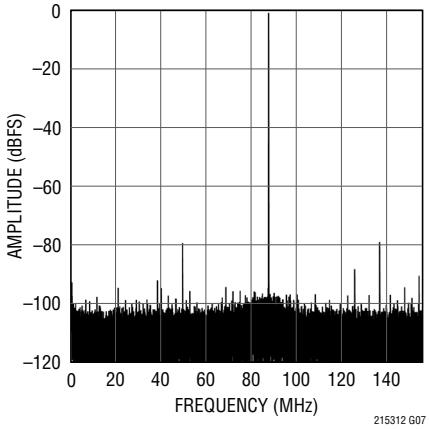
LTC2153-12: 32K Point FFT, f_{IN} = 150MHz, –1dBFS, 310Msps



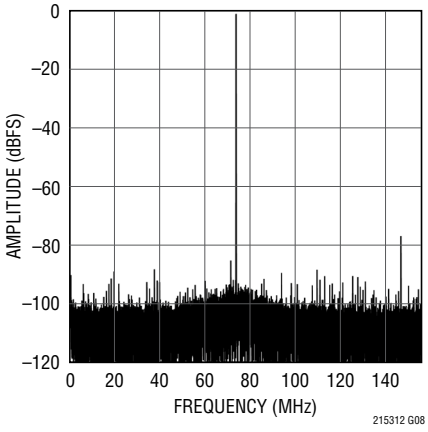
LTC2153-12: 32K Point FFT, f_{IN} = 185MHz, –1dBFS, 310Msps



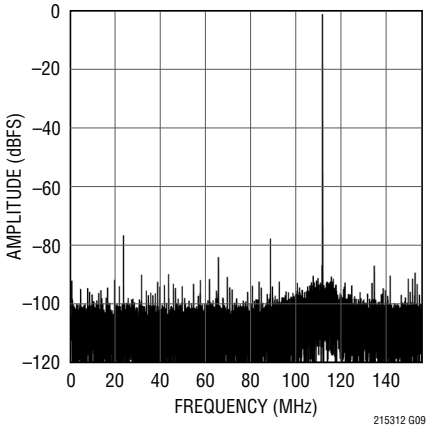
LTC2153-12: 32K Point FFT, f_{IN} = 223MHz, –1dBFS, 310Msps



LTC2153-12: 32K Point FFT, f_{IN} = 383MHz, –1dBFS, 310Msps

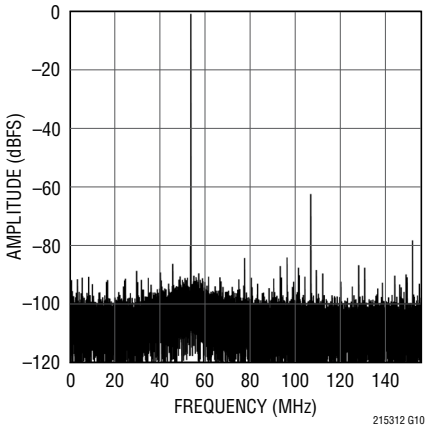


LTC2153-12: 32K Point FFT, f_{IN} = 421MHz, –1dBFS, 310Msps

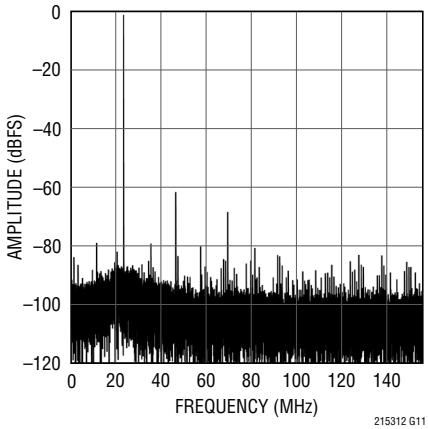


TYPICAL PERFORMANCE CHARACTERISTICS

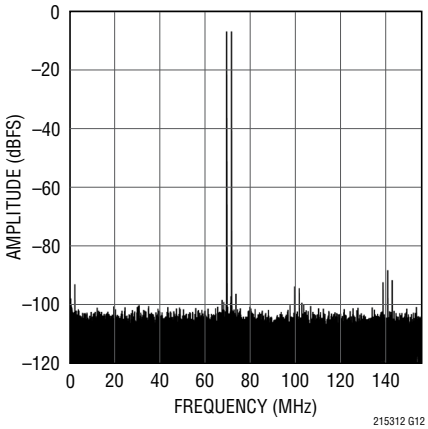
LTC2153-12: 32K Point FFT, f_{IN} = 567MHz, –1dBFS, 310Msps



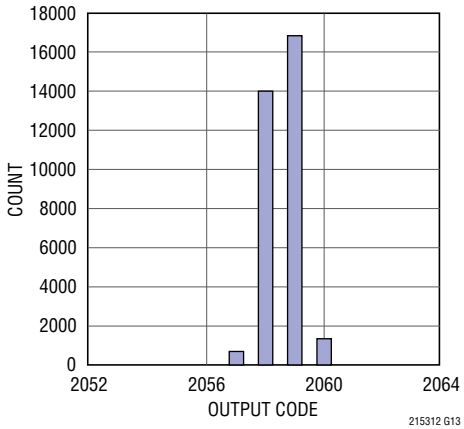
LTC2153-12: 32K Point FFT, f_{IN} = 907MHz, –1dBFS, 310Msps



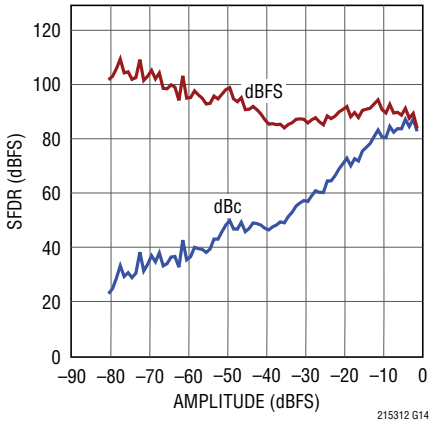
LTC2153-12: 32K Point 2-Tone FFT, f_{IN} = 71MHz and 69MHz, 310Msps



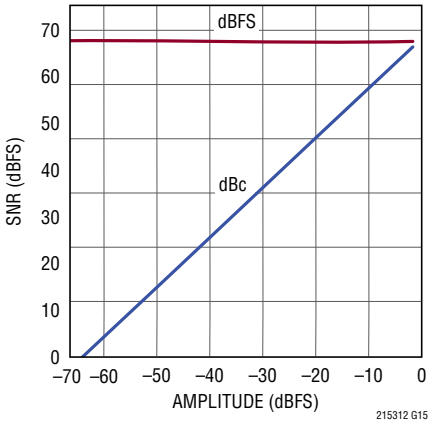
LTC2153-12: Shorted Input Histogram



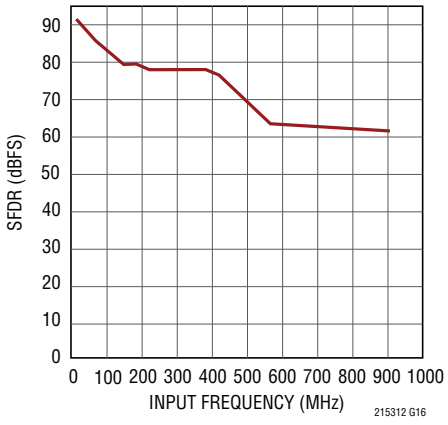
LTC2153-12: SFDR vs Input Level, f_{IN} = 70MHz, 1.32V Range, 310Msps



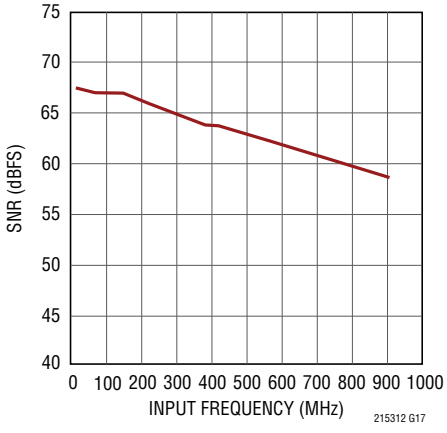
LTC2153-12: SNR vs Input Level, f_{IN} = 70MHz, 1.32V Range, 310Msps



LTC2153-12: SFDR vs Input Frequency, –1dBFS, 1.32V Range, 310Msps

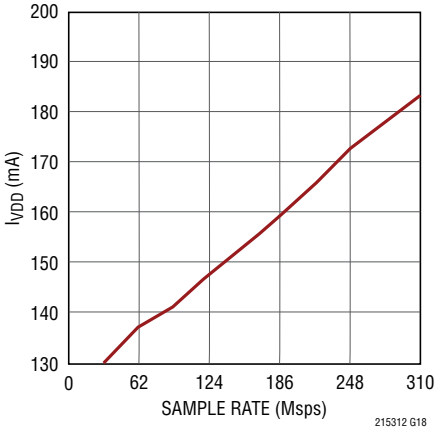


LTC2153-12: SNR vs Input Frequency, –1dBFS, 1.32V Range, 310Msps

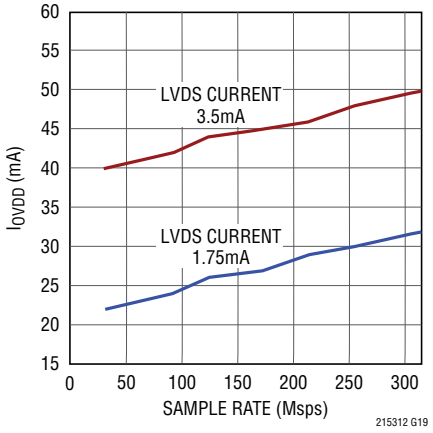


TYPICAL PERFORMANCE CHARACTERISTICS

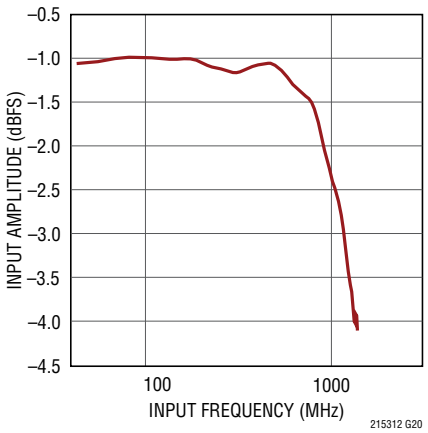
LTC2153-12: I_{VDD} vs Sample Rate, 15MHz Sine Wave Input, –1dBFS



LTC2153-12: I_{OVDD} vs Sample Rate, 15MHz Sine Wave Input, –1dBFS



LTC2153-12: Frequency Response



PIN FUNCTIONS

V_{DD} (Pins 1, 2): 1.8V Analog Power Supply. Bypass to ground with 0.1µF ceramic capacitor. Pins 1, 2 can share a bypass capacitor.

GND (Pins 3, 6, 10, 13, 35, Exposed Pad Pin 41): ADC Power Ground. The exposed pad must be soldered to the PCB ground.

A_{IN}^+ (Pin 4): Positive Differential Analog Input.

A_{IN}^- (Pin 5): Negative Differential Analog Input.

SENSE (Pin 7): Reference Programming Pin. Connecting SENSE to V_{DD} selects the internal reference and a ±0.66V input range. An external reference between 1.23V and 1.27V applied to SENSE selects an input range of ±0.528 • V_{SENSE}.

V_{REF} (Pin 8): Reference Voltage Output. Bypass to ground with a 2.2µF ceramic capacitor. Nominally 1.25V.

V_{CM} (Pin 9): Common Mode Bias Output; nominally equal to 0.439 • V_{DD}. V_{CM} should be used to bias the common mode of the analog inputs. Bypass to ground with a 0.1µF ceramic capacitor.

ENC^+ (Pin 11): Encode Input. Conversion starts on the rising edge.

ENC^- (Pin 12): Encode Complement Input. Conversion starts on the falling edge.

NC (Pins 16, 17): Not Connected.

OV_{DD} (Pins 20, 30): 1.8V Output Driver Supply. Bypass each pin to ground with separate 0.1µF ceramic capacitors.

OGND (Pin 21): LVDS Driver Ground.

SDO (Pin 36): Serial Interface Data Output. In serial programming mode, (PAR/$\overline{SER}$ = 0V), SDO is the optional serial interface data output. Data on SDO is read back from the mode control registers and can be latched on the falling edge of SCK. SDO is an open-drain N-channel MOSFET output that requires an external 2k pull-up resistor from 1.8V to 3.3V. If readback from the mode control registers is not needed, the pull-up resistor is not necessary and SDO can be left unconnected.

SDI (Pin 37): Serial Interface Data Input. In serial programming mode, (PAR/$\overline{SER}$ = 0V), SDI is the serial interface data input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. In parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SDI selects 3.5mA or 1.75mA LVDS output current (see Table 2).

PIN FUNCTIONS

SCK (Pin 38): Serial Interface Clock Input. In serial programming mode, (PAR/$\overline{SER}$ = 0V), SCK is the serial interface clock input. In parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SCK controls the sleep mode (see Table 2).

$\overline{CS}$ (Pin 39): Serial Interface Chip Select Input. In serial programming mode, (PAR/$\overline{SER}$ = 0V), $\overline{CS}$ is the serial interface chip select input. When $\overline{CS}$ is low, SCK is enabled for shifting data on SDI into the mode control registers. In parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), $\overline{CS}$ controls the clock duty cycle stabilizer (see Table 2).

PAR/$\overline{SER}$ (Pin 40): Programming Mode Selection Pin. Connect to ground to enable the serial programming mode. $\overline{CS}$, SCK, SDI and SDO become a serial interface that control the A/D operating modes. Connect to V_{DD} to enable the parallel programming mode where $\overline{CS}$, SCK and SDI become parallel logic inputs that control a reduced set of the A/D operating modes. PAR/$\overline{SER}$ should be connected directly to ground or the V_{DD} of the part and not be driven by a logic signal.

LVDS Outputs (DDR LVDS)

The following pins are differential LVDS outputs. The output current level is programmable. There is an optional internal 100Ω termination resistor between the pins of each LVDS output pair.

$D_{0\_1}^-/D_{0\_1}^+$ to $D_{10\_11}^-/D_{10\_11}^+$ (Pins 18/19, 22/23, 24/25, 28/29, 31/32, 33/34): Double-Data Rate Digital Outputs. Two data bits are multiplexed onto each differential output pair. The even data bits (D0, D2, D4, D6, D8, D10) appear when CLKOUT+ is low. The odd data bits (D1, D3, D5, D7, D9, D11) appear when CLKOUT+ is high.

CLKOUT−, CLKOUT+ (Pins 26, 27): Data Output Clock. The digital outputs normally transition at the same time as the falling and rising edges of CLKOUT+. The phase of CLKOUT+ can also be delayed relative to the digital outputs by programming the mode control registers.

OF−, OF+ (Pins 14, 15): Over/Underflow Digital Output. OF+ is high when an overflow or underflow has occurred. This underflow is valid only when CLKOUT+ is low. In the second half clock cycle, the overflow is set to 0.

FUNCTIONAL BLOCK DIAGRAM

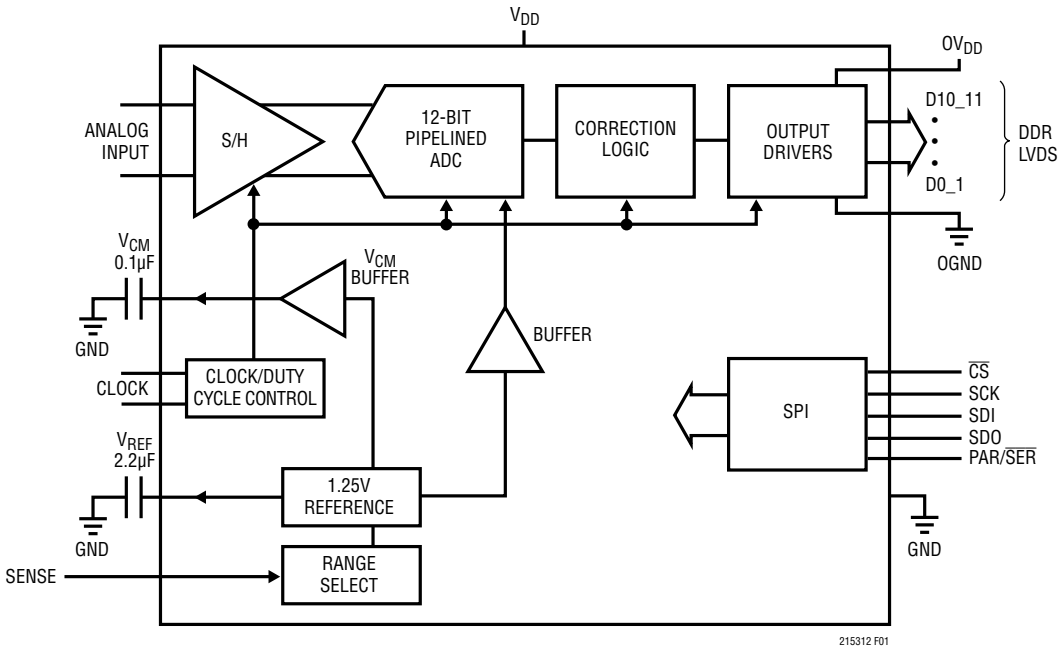
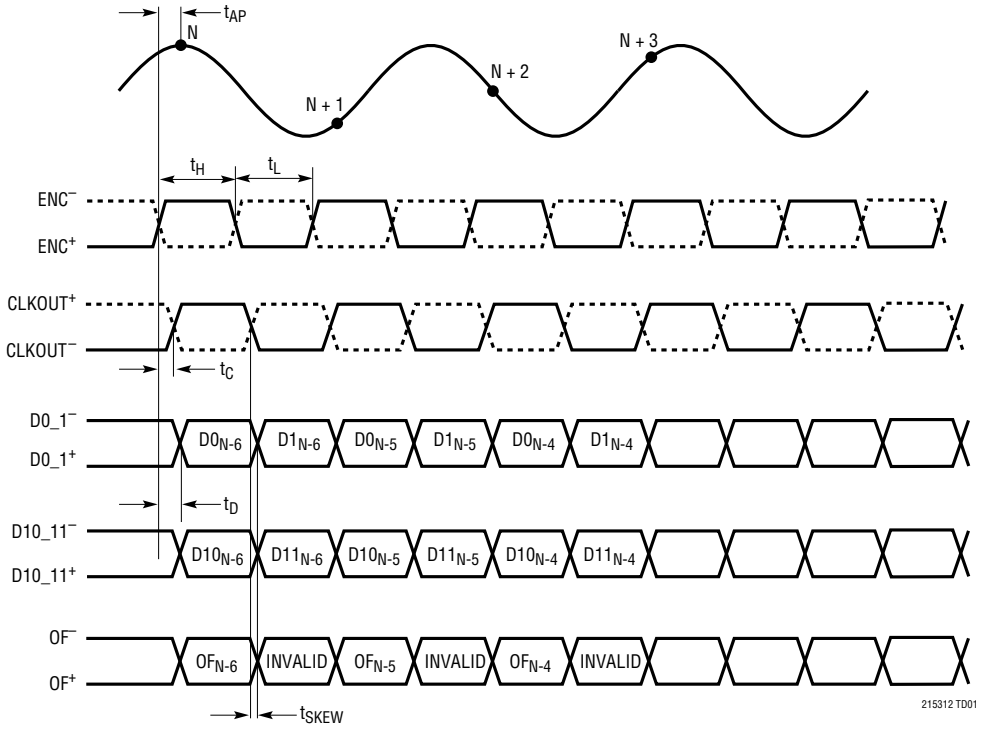


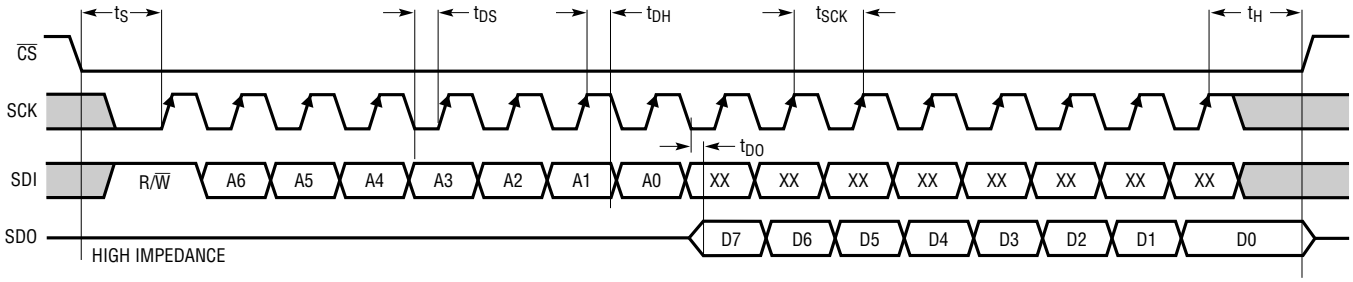
Figure 1. Functional Block Diagram

TIMING DIAGRAMS

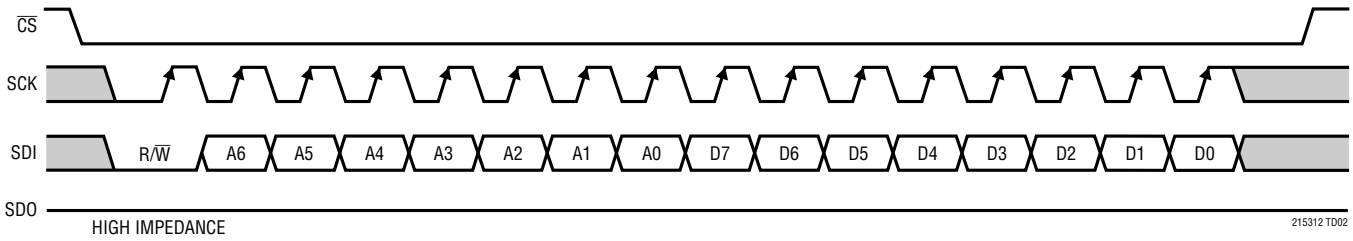
Double Data Rate Output Timing, All Outputs Are Differential LVDS



SPI Port Timing (Readback Mode)



SPI Port Timing (Write Mode)



APPLICATIONS INFORMATION

CONVERTER OPERATION

The LTC2153-12 is a 12-bit 310Msps A/D converter powered by a single 1.8V supply. The analog inputs must be driven differentially. The encode inputs should be driven differentially for optimal performance. The digital outputs are double data rate LVDS. Additional features can be chosen by programming the mode control registers through a serial SPI port.

ANALOG INPUT

The analog input is a differential CMOS sample-and-hold circuits (Figure 2). The inputs must be driven differentially around a common mode voltage set by the V_{CM} output pin, which is nominally 0.439 • V_{DD}. For the 1.32V input range, the input should swing from V_{CM} – 0.33V to V_{CM} + 0.33V. There should be 180° phase difference between the inputs.

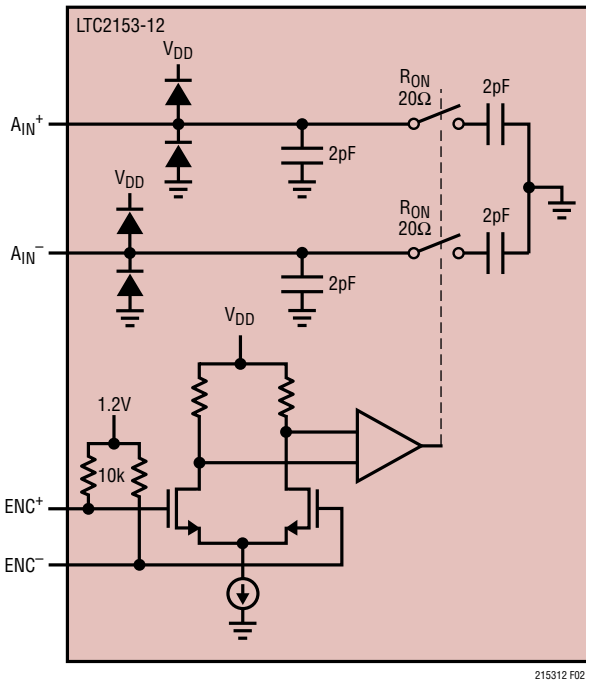


Figure 2. Equivalent Input Circuit. Only One of Two Analog Channels Is Shown

INPUT DRIVE CIRCUITS

Input Filtering

If possible, there should be an RC lowpass filter right at the analog inputs. This lowpass filter isolates the drive circuitry from the A/D sample-and-hold switching, and also limits wide band noise from the drive circuitry. Figure 3 shows an example of an input RC filter. The RC component values should be chosen based on the application's specific input frequency.

Transformer-Coupled Circuits

Figure 3 shows the analog input being driven by an RF transformer with the common mode supplied through a pair of resistors via the V_{CM} pin.

At higher input frequencies a transmission line balun transformer (Figures 4 and 5) has better balance, resulting in lower A/D distortion.

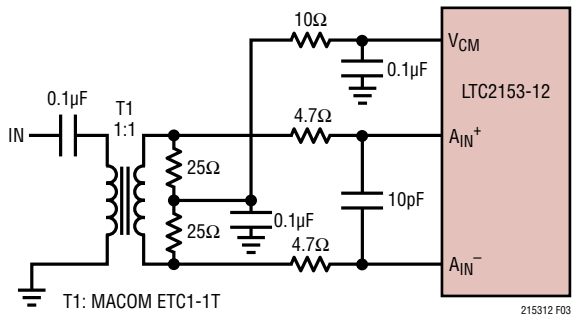


Figure 3. Analog Input Circuit Using a Transformer. Recommended for Input Frequencies from 5MHz to 70MHz

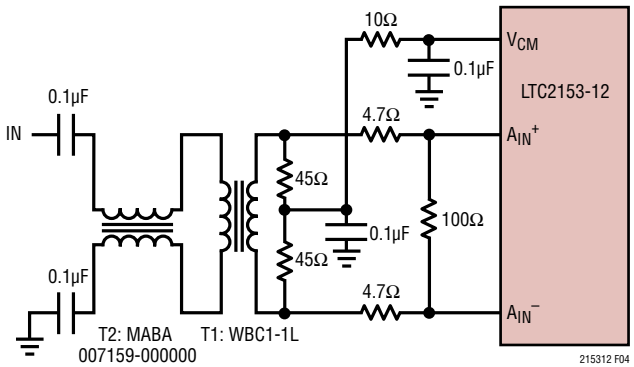


Figure 4. Recommended Front-End Circuit for Input Frequencies from 15MHz to 150MHz

APPLICATIONS INFORMATION

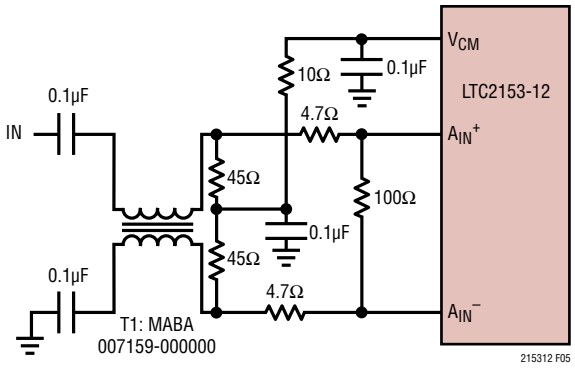


Figure 5. Recommended Front-End Circuit for Input Frequencies from 150MHz to 900MHz

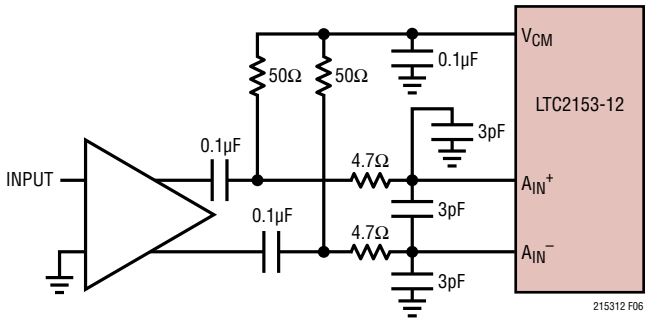


Figure 6. Front-End Circuit Using a High Speed Differential Amplifier

Amplifier Circuits

Figure 6 shows the analog input being driven by a high speed differential amplifier. The output of the amplifier is AC coupled to the A/D so the amplifier's output common mode voltage can be optimally set to minimize distortion.

At very high frequencies an RF gain block will often have lower distortion than a differential amplifier. If the gain block is single-ended, then a transformer circuit (Figures 3 and 5) should convert the signal to differential before driving the A/D. The A/D cannot be driven single-ended.

Reference

The LTC2153-12 has an internal 1.25V voltage reference. For a 1.32V input range with internal reference, connect SENSE to V_{DD}. For a 1.32V input range with an external reference, apply a 1.25V reference voltage to SENSE (Figure 7).

Encode Input

The signal quality of the encode inputs strongly affects the A/D noise performance. The encode inputs should be treated as analog signals—do not route them next to digital traces on the circuit board.

The encode inputs are internally biased to 1.2V through 10k equivalent resistance (Figure 8). If the common mode of the driver is within 1.1V to 1.5V, it is possible to drive the encode inputs directly. Otherwise a transformer or coupling capacitors are needed (Figures 9 and 10). The maximum (peak) voltage of the input signal should never exceed V_{DD} +0.1V or go below –0.1V.

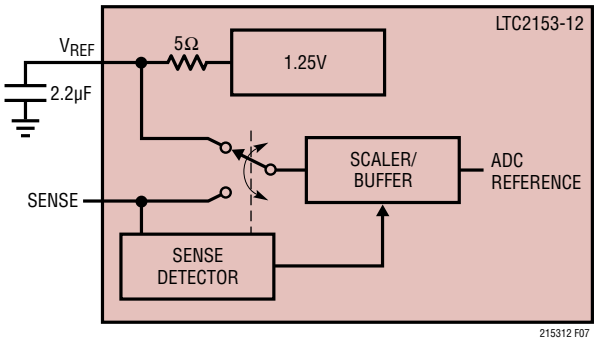


Figure 7. Reference Circuit

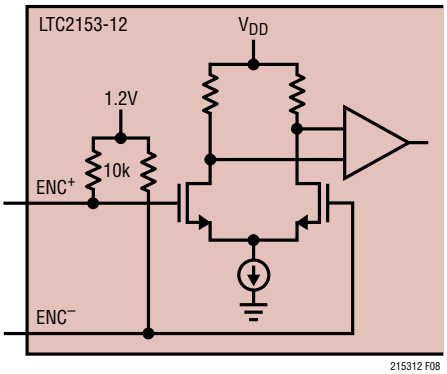


Figure 8. Equivalent Encode Input Circuit

APPLICATIONS INFORMATION

Clock Duty Cycle Stabilizer

For good performance the encode signal should have a 50% (±5%) duty cycle. If the optional clock duty cycle stabilizer circuit is enabled, the encode duty cycle can vary from 30% to 70% and the duty cycle stabilizer will maintain a constant 50% internal duty cycle. The duty cycle stabilizer is enabled via SPI Register A2 (see Table 3) or by $\overline{CS}$ in parallel programming mode.

For applications where the sample rate needs to be changed quickly, the clock duty cycle stabilizer can be disabled. In this case, care should be taken to make the clock a 50% (±5%) duty cycle.

DIGITAL OUTPUTS

The digital outputs are double data rate LVDS signals. T wo data bits are multiplexed and output on each differential output pair. There are six LVDS output pairs, D0_1$^+$/D0_1$^-$ through D10_11$^-$/D10_11$^+$. Overflow (OF$^+$/OF$^-$) and the data output clock (CLKOUT$^+$/CLKOUT$^-$) each have an LVDS output pair.

By default the outputs are standard LVDS levels: 3.5mA output current and a 1.25V output common mode voltage.

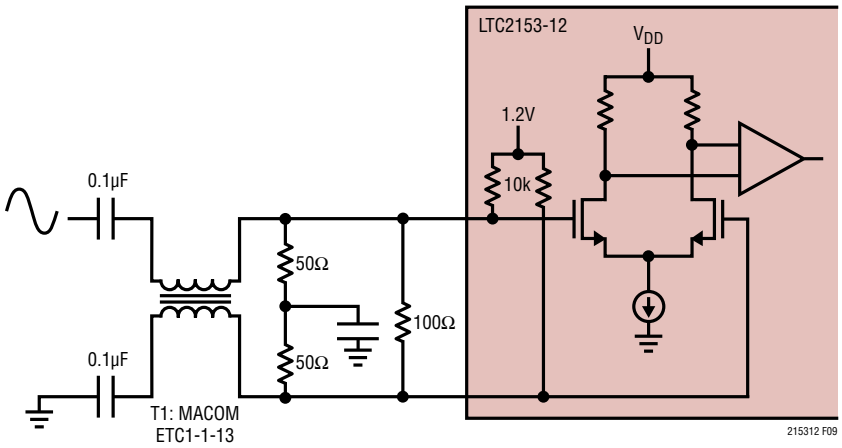


Figure 9. Sinusoidal Encode Drive

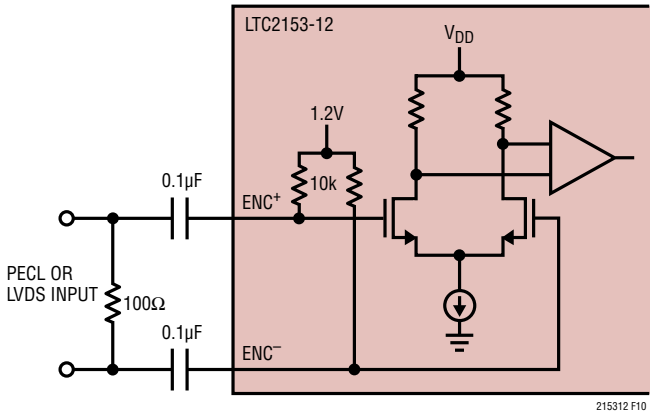


Figure 10. PECL or LVDS Encode Drive

APPLICATIONS INFORMATION

Programmable LVDS Output Current

The default output driver current is 3.5mA. This current can be adjusted by serially programming mode control register A3 (see Table 3). Available current levels are 1.75mA, 2.1mA, 2.5mA, 3mA, 3.5mA, 4mA and 4.5mA.

Optional LVDS Driver Internal Termination

In most cases, using just an external 100Ω termination resistor will give excellent LVDS signal integrity. In addition, an optional internal 100Ω termination resistor can be enabled by serially programming mode control register A3. The internal termination helps absorb any reflections caused by imperfect termination at the receiver. When the internal termination is enabled, the output driver current is doubled to maintain the same output voltage swing.

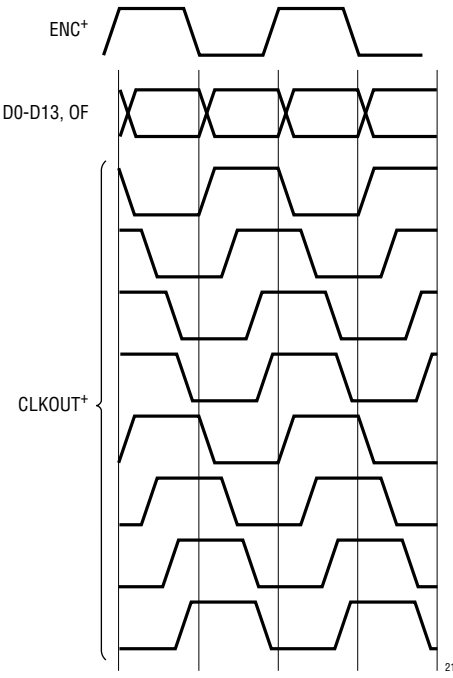
Overflow Bit

The overflow output bit (OF) outputs a logic high when the analog input is either overranged or underranged. The overflow bit has the same pipeline latency as the data bits. When CLKINV is set to 0 in the SPI register A2, the OF signal is valid when CLKOUT+ is low, as shown in the Timing Diagram.

Phase Shifting the Output Clock

To allow adequate set-up and hold time when latching the output data, the CLKOUT+ signal may need to be phase shifted relative to the data output bits. Most FPGAs have this feature; this is generally the best place to adjust the timing.

Alternatively, the ADC can also phase shift the CLKOUT+/CLKOUT– signals by serially programming mode control register A2. The output clock can be shifted by 0°, 45°, 90°, or 135°. To use the phase shifting feature the clock duty cycle stabilizer must be turned on. Another control register bit can invert the polarity of CLKOUT+ and CLKOUT–, independently of the phase shift. The combination of these two features enables phase shifts of 45° up to 315° (Figure 11).



PHASE SHIFT	MODE CONTROL BITS CLKINV	CLKPHASE1	CLKPHASE0
0°	0	0	0
45°	0	0	1
90°	0	1	0
135°	0	1	1
180°	1	0	0
225°	1	0	1
270°	1	1	0
315°	1	1	1

Figure 11. Phase Shifting CLKOUT

APPLICATIONS INFORMATION

DATA FORMAT

Table 1 shows the relationship between the analog input voltage, the digital data output bits and the overflow bit. By default the output data format is offset binary. The 2's complement format can be selected by serially programming mode control register A4.

Table 1. Output Codes vs Input Voltage

$A_{IN}^+ - A_{IN}^-$ (1.32V Range)	OF	D11-D0 (OFFSET BINARY)	D11-D0 (2's COMPLEMENT)
>0.66V	1	1111 1111 1111	0111 1111 1111
+0.66V	0	1111 1111 1111	0111 1111 1111
+0.6596777V	0	1111 1111 1110	0111 1111 1110
+0.0003222V	0	1000 0000 0001	0000 0000 0001
+0.000000V	0	1000 0000 0000	0000 0000 0000
–0.0003222V	0	0111 1111 1111	1111 1111 1111
–0.0006445V	0	0111 1111 1110	1111 1111 1110
–0.6596777V	0	0000 0000 0001	1000 0000 0001
–0.66V	0	0000 0000 0000	1000 0000 0000
< –0.66V	1	0000 0000 0000	1000 0000 0000

Digital Output Randomizer

Interference from the A/D digital outputs is sometimes unavoidable. Digital interference may be from capacitive or inductive coupling or coupling through the ground plane. Even a tiny coupling factor can cause unwanted tones in the ADC output spectrum. By randomizing the digital output before it is transmitted off chip, these unwanted tones can be randomized which reduces the unwanted tone amplitude.

The digital output is randomized by applying an exclusive-OR logic operation between the LSB and all other data output bits. To decode, the reverse operation is applied—an exclusive-OR operation is applied between the LSB and all other bits. The LSB, OF and CLKOUT outputs are not affected. The output randomizer is enabled by serially programming mode control register A4.

Alternate Bit Polarity

Another feature that may reduce digital feedback on the circuit board is the alternate bit polarity mode. When this mode is enabled, all of the odd bits (D1, D3, D5, D7, D9, D11) are inverted before the output buffers. The even bits (D0, D2, D4, D6, D8, D10), OF and CLKOUT are not affected. This can reduce digital currents in the circuit board ground plane and reduce digital noise, particularly for very small analog input signals.

The digital output is decoded at the receiver by inverting the odd bits (D1, D3, D5, D7, D9, D11). The alternate bit polarity mode is independent of the digital output randomizer—either both or neither function can be on at the same time. The alternate bit polarity mode is enabled by serially programming mode control register A4.

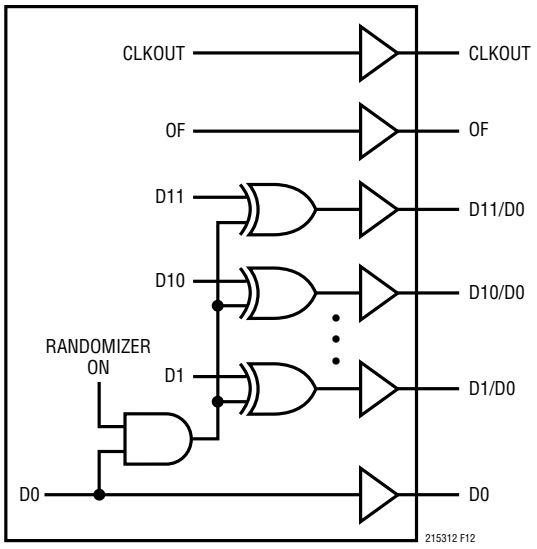


Figure 12. Functional Equivalent of Digital Output Randomizer

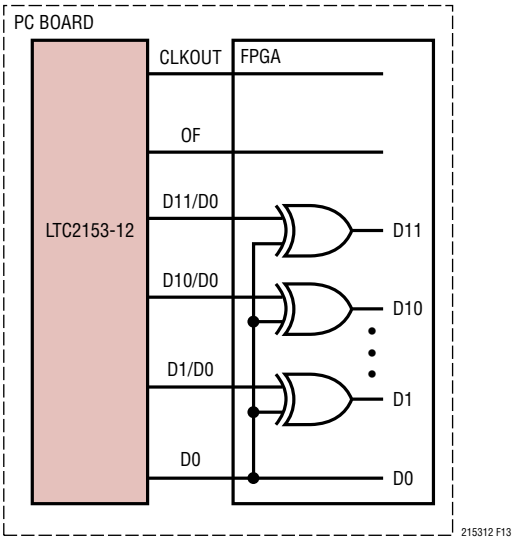


Figure 13. Decoding a Randomized Digital Output Signal

APPLICATIONS INFORMATION

Digital Output Test Patterns

To allow in-circuit testing of the digital interface to the A/D, there are several test modes that force the A/D data outputs (OF, D11 to D0) to known values:

All 1s: All outputs are 1

All 0s: All outputs are 0

Alternating: Outputs change from all 1s to all 0s on alternating samples

Checkerboard: Outputs change from 1010101010101 to 0101010101010 on alternating samples.

The digital output test patterns are enabled by serially programming mode control register A4. When enabled, the test patterns override all other formatting modes: 2's complement, randomizer, alternate-bit polarity.

Output Disable

The digital outputs may be disabled by serially programming mode control register A3. All digital outputs including OF and CLKOUT are disabled. The high impedance disabled state is intended for long periods of inactivity, it is not designed for multiplexing the data bus between multiple converters.

Sleep Mode

The A/D may be placed in sleep mode to conserve power. In sleep mode the entire A/D converter is powered down, resulting in < 5mW power consumption. If the encode input signal is not disabled, the power consumption will be higher (up to 5mW at 310Msps). Sleep mode is enabled by mode control register A1 (serial programming mode), or by SCK (parallel programming mode).

The amount of time required to recover from sleep mode depends on the size of the bypass capacitor on V_{REF}. For the suggested value in Figure 1, the A/D will stabilize after 0.1ms + 2500 • t_p where t_p is the period of the sampling clock.

Nap Mode

In nap mode the A/D core is powered down while the internal reference circuits stay active, allowing faster wake-up. Recovering from nap mode requires at least 100 clock cycles.

Wake-up time from nap mode is guaranteed only if the clock is kept running, otherwise sleep mode wake-up conditions apply.

Nap mode is enabled by setting register A1 in the serial programming mode.

DEVICE PROGRAMMING MODES

The operating modes of the LTC2153-12 can be programmed by either a parallel interface or a simple serial interface. The serial interface has more flexibility and can program all available modes. The parallel interface is more limited and can only program some of the more commonly used modes.

Parallel Programming Mode

To use the parallel programming mode, PAR/$\overline{SER}$ should be tied to V_{DD}. The $\overline{CS}$, SCK and SDI pins are binary logic inputs that set certain operating modes. These pins can be tied to V_{DD} or ground, or driven by 1.8V, 2.5V, or 3.3V CMOS logic. Table 2 shows the modes set by $\overline{CS}$, SCK and SDI.

Table 2. Parallel Programming Mode Control Bits (PAR/$\overline{SER}$ = V_{DD})

PIN	DESCRIPTION
$\overline{CS}$	Clock Duty Cycle Stabilizer Control Bit 0 = Clock Duty Cycle Stabilizer Off 1 = Clock Duty Cycle Stabilizer On
SCK	Power Down Control Bit 0 = Normal Operation 1 = Sleep Mode (entire ADC is powered down)
SDI	LVDS Current Selection Bit 0 = 3.5mA LVDS Current Mode 1 = 1.75mA LVDS Current Mode

APPLICATIONS INFORMATION

Serial Programming Mode

To use the serial programming mode, PAR/$\overline{SER}$ should be tied to ground. The $\overline{CS}$, SCK, SDI and SDO pins become a serial interface that program the A/D control registers. Data is written to a register with a 16-bit serial word. Data can also be read back from a register to verify its contents.

Serial data transfer starts when $\overline{CS}$ is taken low. The data on the SDI pin is latched at the first sixteen rising edges of SCK. Any SCK rising edges after the first sixteen are ignored. The data transfer ends when $\overline{CS}$ is taken high again.

The first bit of the 16-bit input word is the R/$\overline{W}$ bit. The next seven bits are the address of the register (A6:A0). The final eight bits are the register data (D7:D0).

If the R/$\overline{W}$ bit is low, the serial data (D7:D0) will be written to the register set by the address bits (A6:A0). If the R/$\overline{W}$ bit is high, data in the register set by the address bits (A6:A0) will be read back on the SDO pin (see the Timing Diagrams). During a readback command the register is not updated and data on SDI is ignored.

The SDO pin is an open-drain output that pulls to ground with a 200Ω impedance. If register data is read back through SDO, an external 2k pull-up resistor is required. If serial data is only written and readback is not needed, then SDO can be left floating and no pull-up resistor is needed. Table 3 shows a map of the mode control registers.

Software Reset

If serial programming is used, the mode control registers should be programmed as soon as possible after the power supplies turn on and are stable. The first serial command must be a software reset which will reset all register data bits to logic 0. To perform a software reset it is necessary to write 1 in register A0 (Bit D7). After the reset is complete, Bit D7 is automatically set back to zero. This register is write-only.

GROUNDING AND BYPASSING

The LTC2153-12 requires a printed circuit board with a clean unbroken ground plane in the first layer beneath the ADC. A multilayer board with an internal ground plane is recommended. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

High quality ceramic bypass capacitors should be used at the V_{DD}, OV_{DD}, V_{CM}, V_{REF} pins. Bypass capacitors must be located as close to the pins as possible. Size 0402 ceramic capacitors are recommended. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The analog inputs, encode signals, and digital outputs should not be routed next to each other. Ground fill and grounded vias should be used as barriers to isolate these signals from each other.

HEAT TRANSFER

Most of the heat generated by the LTC2153-12 is transferred from the die through the bottom-side exposed pad and package leads onto the printed circuit board. For good electrical and thermal performance, the exposed pad must be soldered to a large grounded pad on the PC board. This pad should be connected to the internal ground planes by an array of vias.

APPLICATIONS INFORMATION

Table 3. Serial Programming Mode Register Map (PAR/$\overline{SER}$ = GND). X indicates an unused bit that is read back as 0

REGISTER A0: RESET REGISTER (ADDRESS 00h) Write Only

D7	D6	D5	D4	D3	D2	D1	D0
RESET	X	X	X	X	X	X	X

Bit 7 **RESET** Software Reset Bit

0 = Reset Disabled
1 = Software Reset. All mode control registers are reset to 00h. This bit is automatically set back to zero after the reset is complete.

Bits 6-0 Unused Bits

REGISTER A1: POWER-DOWN REGISTER (ADDRESS 01h)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	SLEEP	NAP	0	0

Bits 7-4 Unused Bit

Bit 3 **SLEEP**

0 = Normal Operation
1 = Power Down Entire ADC

Bit 2 **NAP**

0 = Normal Mode
1 = Low Power Mode

Bit 1-0 Must be set to 0

REGISTER A2: TIMING REGISTER (ADDRESS 02h)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	CLKINV	CLKPHASE1	CLKPHASE0	DCS

Bits 7-4 Unused Bit

Bit 3 **CLKINV** Output Clock Invert Bit
0 = Normal CLKOUT Polarity (as shown in the Timing Diagrams)
1 = Inverted CLKOUT Polarity

Bits 2-1 **CLKPHASE1:CLKPHASE0** Output Clock Phase Delay Bits
00 = No CLKOUT Delay (as shown in the Timing Diagrams)
01 = $CLKOUT^+/CLKOUT^-$ delayed by 45° (Clock Period • 1/8)
10 = $CLKOUT^+/CLKOUT^-$ delayed by 90° (Clock Period • 1/4)
11 = $CLKOUT^+/CLKOUT^-$ delayed by 135° (Clock Period • 3/8)
Note: If the CLKOUT phase delay feature is used, the clock duty cycle stabilizer must also be turned on.

Bit 0 **DCS** Clock Duty Cycle Stabilizer Bit
0 = Clock Duty Cycle Stabilizer Off
1 = Clock Duty Cycle Stabilizer On

APPLICATIONS INFORMATION

REGISTER A3: OUTPUT MODE REGISTER (ADDRESS 03h)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	ILVDS2	ILVDS1	ILVDS0	TERMON	OUTOFF

Bits 7-5 Unused Bit

Bits 4-2 **ILVDS2:ILVDS0** LVDS Output Current Bits
000 = 3.5mA LVDS Output Driver Current
001 = 4.0mA LVDS Output Driver Current
010 = 4.5mA LVDS Output Driver Current
011 = Not Used
100 = 3.0mA LVDS Output Driver Current
101 = 2.5mA LVDS Output Driver Current
110 = 2.1mA LVDS Output Driver Current
111 = 1.75mA LVDS Output Driver Current

Bit 1 **TERMON** LVDS Internal Termination Bit
0 = Internal Termination Off
1 = Internal Termination On. LVDS output driver current is 2× the current set by ILVDS2:ILVDS0

Bit 0 **OUTOFF** Digital Output Mode Control Bits
0 = Digital Outputs Are Enabled
1 = Digital Outputs Are Disabled (High Impedance)

REGISTER A4: DATA FORMAT REGISTER (ADDRESS 04h)

D7	D6	D5	D4	D3	D2	D1	D0
OUTTEST2	OUTTEST1	OUTTEST0	ABP	0	DTESTON	RAND	TWOSCOMP

Bits 7-5 **OUTTEST2:OUTTEST0** Digital Output Test Pattern Bits
000 = All Digital Outputs = 0
001 = All Digital Outputs = 1
010 = Alternating Output Pattern. OF, D11-D0 alternate between 0 0000 0000 0000 and 1 1111 1111 1111
100 = Checkerboard Output Pattern. OF, D11-D0 alternate between 1 0101 0101 0101 and 0 1010 1010 1010
Note 1: Other bit combinations are not used.

Bit 4 **ABP** Alternate Bit Polarity Mode Control Bit
0 = Alternate Bit Polarity Mode Off
1 = Alternate Bit Polarity Mode On

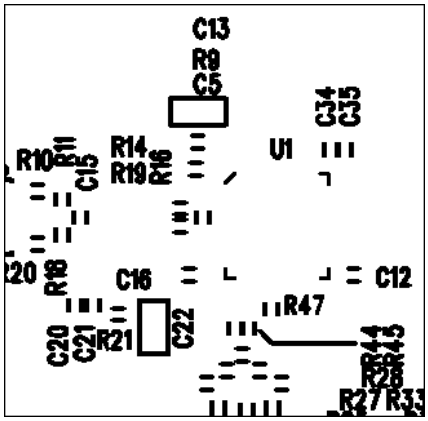
Bit 3 Must Be Set to 0

Bit 2 **DTESTON** Enable the digital output test patterns (set by Bits 7-5)
0 = Normal Mode
1 = Enable the Digital Output Test Patterns

Bit 1 **RAND** Data Output Randomizer Mode Control Bit
0 = Data Output Randomizer Mode Off
1 = Data Output Randomizer Mode On

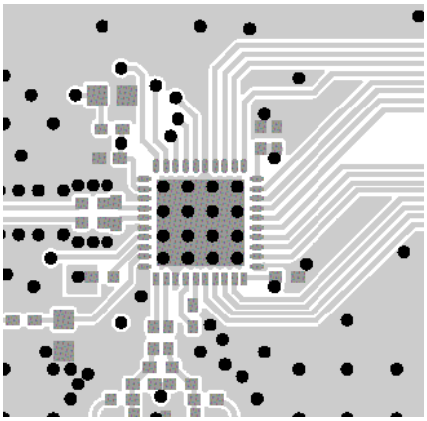
Bit 0 **TWOSCOMP** Two's Complement Mode Control Bit
0 = Offset Binary Data Format
1 = Two's Complement Data Format

APPLICATIONS INFORMATION



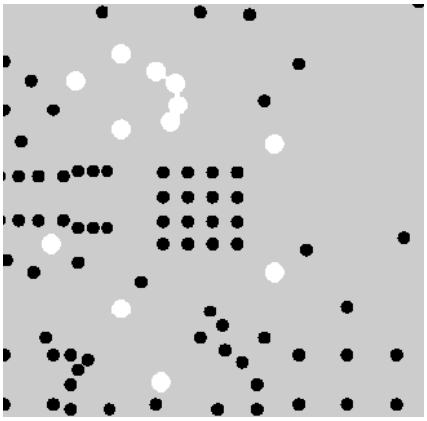
215312 F14

Silkscreen Top



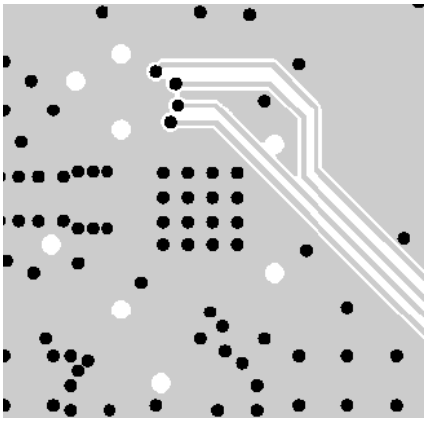
215312 F15

Inner Layer 1



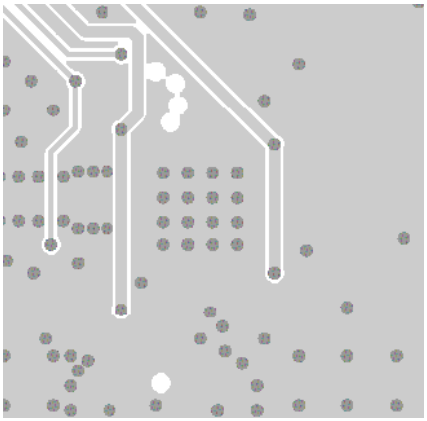
215312 F16

Inner Layer 2



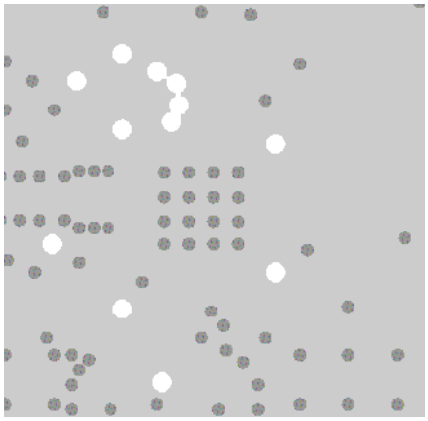
215312 F17

Inner Layer 3



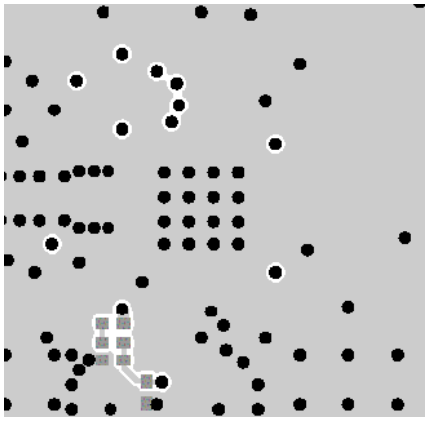
215312 F18

Inner Layer 4



215312 F19

Inner Layer 5

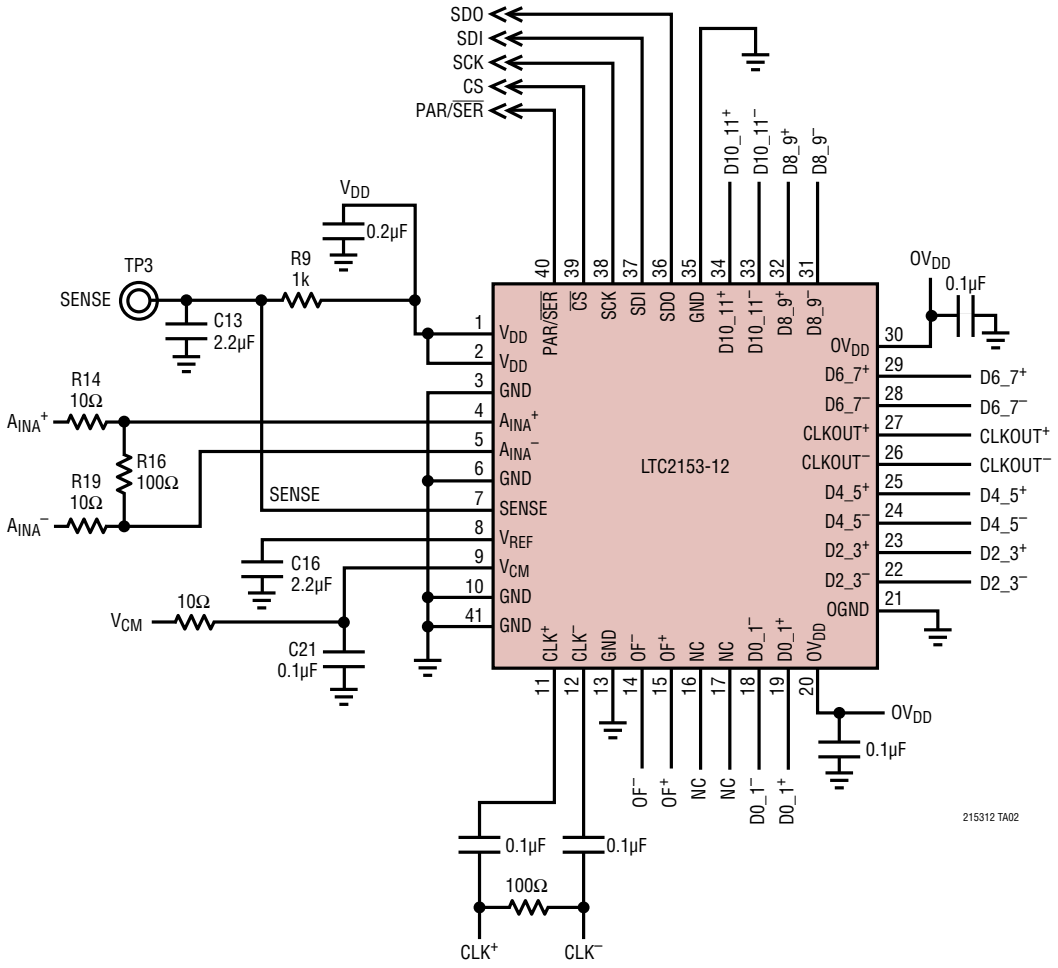


215312 F20

Bottom Layer

TYPICAL APPLICATIONS

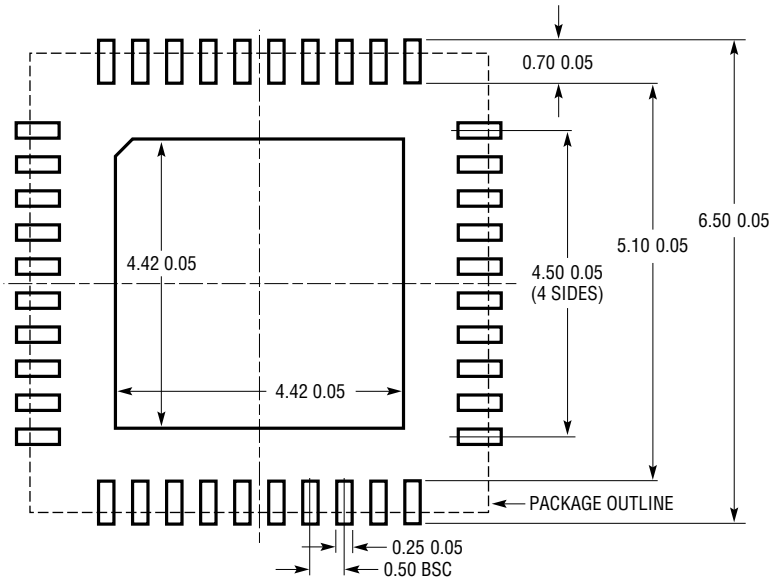
2153-12 Schematic



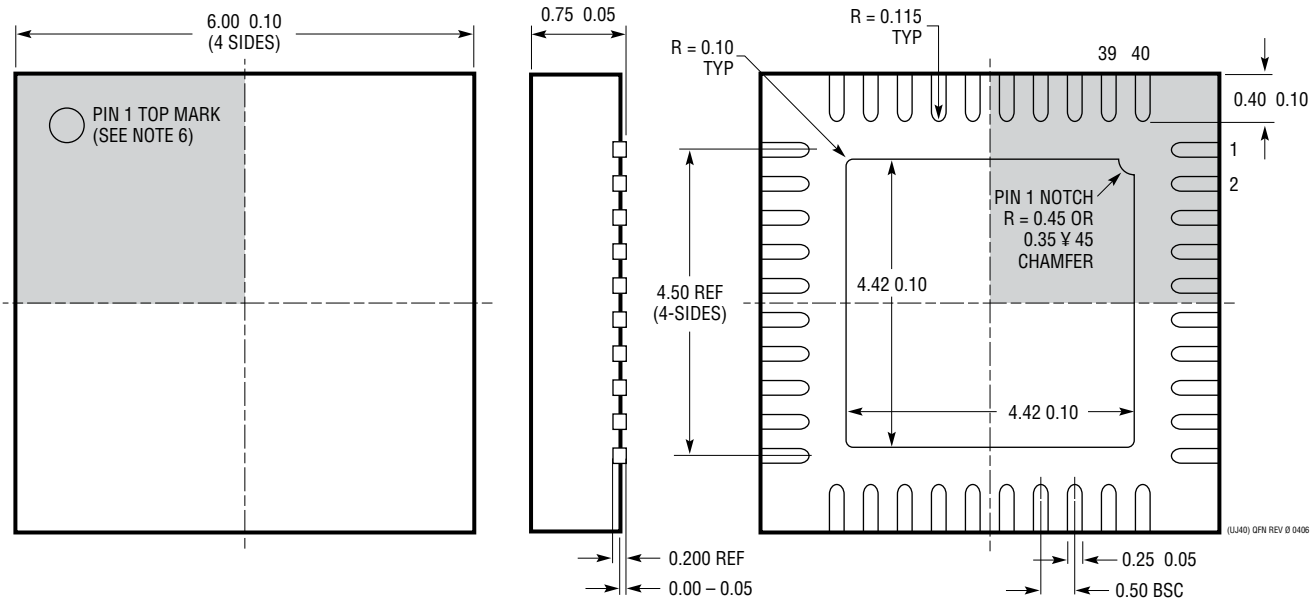
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UJ Package
40-Lead Plastic QFN (6mm × 6mm)
(Reference LTC DWG # 05-08-1728 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



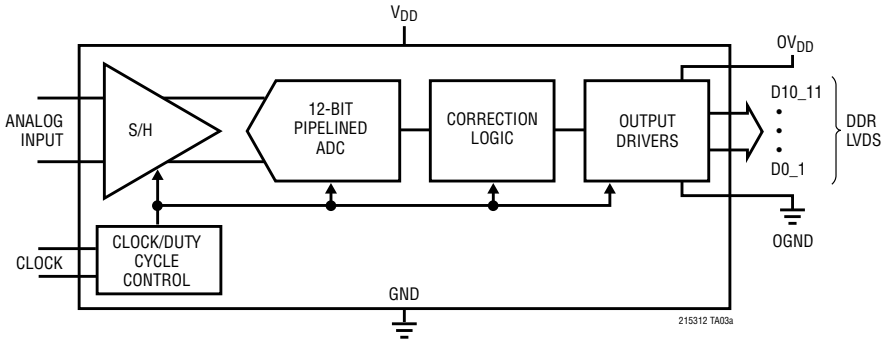
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

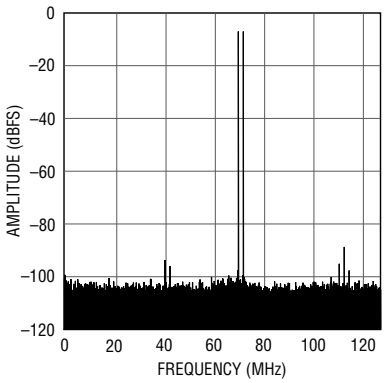
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/14	Changed the pipeline latency to 6 Updated G15	5 and 10 7

TYPICAL APPLICATION



LTC2153-12: 32K Point 2-Tone FFT, f_{IN} = 71MHz and 69MHz, 310Msps



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC2208	16-Bit, 130Msps, 3.3V ADC, LVDS Outputs	1250mW, 77.7dB SNR, 100dB SFDR, 64-Lead QFN Package
LTC2158-14	14-Bit, 310Msps, 1.8V Dual ADC, DDR LVDS Outputs	724mW, 68.8dB SNR, 88dB SFDR, 64-Lead QFN Package
LTC2157-14/LTC2156-14/ LTC2155-14	14-Bit Dual, 250Msps/210Msps/170Msps, 1.8V Dual ADC, DDR LVDS Outputs	605mW/565mW/511mW, 70dB SNR, 90dB SFDR, 9mm × 9mm 64-Lead QFN Package
LTC2152-14/LTC2151-14/ LTC2150-14	14-Bit, 250Msps/210Msps/170Msps, 1.8V Single ADC, DDR LVDS Outputs	338mW/316mW/290mW, 70dB SNR, 90dB SFDR, 6mm × 6mm 40-Lead QFN Package
LTC2153-14	14-Bit, 310Msps 1.8V Single ADC, DDR LVDS Outputs	401mW, 68.8dB SNR, 88dB SFDR, 6mm × 6mm 40-Lead QFN Package
RF Mixers/Demodulators		
LT5517	40MHz to 900MHz Direct Conversion Quadrature Demodulator	High IIP3: 21dBm at 800MHz, Integrated LO Quadrature Generator
LT5527	400MHz to 3.7GHz High Linearity Downconverting Mixer	24.5dBm IIP3 at 900MHz, 23.5dBm IIP3 at 3.5GHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports
LT5575	800MHz to 2.7GHz Direct Conversion Quadrature Demodulator	High IIP3: 28dBm at 900MHz, Integrated LO Quadrature Generator, Integrated RF and LO Transformer
Amplifiers/Filters		
LTC6409	10GHz GBW, 1.1nV/√Hz Differential Amplifier/ADC Driver	88dB SFDR at 100MHz, Input Range Includes Ground 52mA Supply Current, 3mm × 2mm QFN Package
LTC6412	800MHz, 31dB Range, Analog-Controlled Variable Gain Amplifier	Continuously Adjustable Gain Control, 35dBm OIP3 at 240MHz, 10dB Noise Figure, 4mm × 4mm QFN-24 Package
LTC6420-20	1.8GHz Dual Low Noise, Low Distortion Differential ADC Drivers for 300MHz IF	Fixed Gain 10V/V, 1nV/√Hz Total Input Noise, 80mA Supply Current per Amplifier, 3mm × 4mm QFN-20 Package
Receiver Subsystems		
LTM9002	14-Bit Dual Channel IF/Baseband Receiver Subsystem	Integrated High Speed ADC, Passive Filters and Fixed Gain Differential Amplifiers
LTM9003	12-Bit Digital Predistortion Receiver	Integrated 12-Bit ADC Down-Converter Mixer with 0.4GHz to 3.8GHz Input Frequency Range

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LTC2153-12
LT 1214 REV A • PRINTED IN USA