Ultralow Noise, 200 mA, CMOS Linear Regulator

Enhanced Product

ADP151-EP

FEATURES

- Ultralow noise: 9 µV rms
- Input voltage range: 2.2 V to 5.5 V
- Low quiescent current
  - I_{GND} = 10 µA with 0 load
  - I_{GND} = 265 µA with 200 mA load
- Low shutdown current: <1 µA
- Low dropout voltage: 150 mV at 200 mA load
- Accuracy over line, load, and temperature: −2.5%/+3%
- PSRR performance of 70 dB at 10 kHz
- Current-limit and thermal overload protection
- Internal pull-down resistor on EN input
- 5-lead TSOT package
- Enhanced processing (EP) for −55°C to +125°C operation

APPLICATIONS

- RF, VCO, and PLL power supplies
- Portable and battery-powered equipment
- Post dc-to-dc regulation
- Portable medical devices
- Aeronautic and military operating temperature environment

TYPICAL APPLICATION CIRCUIT

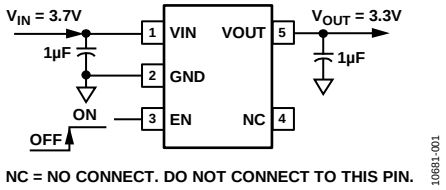

Figure 1. TSOT ADP151-EP with Fixed Output Voltage, 3.3 V

GENERAL DESCRIPTION

The ADP151-EP is an ultralow noise, low dropout linear regulator that operates from 2.2 V to 5.5 V and provides up to 200 mA of output current. The low 150 mV dropout voltage at 200 mA load improves efficiency and allows operation over a wide input voltage range.

Using an innovative circuit topology, the ADP151-EP achieves ultralow noise performance without the necessity of a bypass capacitor, making it ideal for noise-sensitive analog and RF applications. The ADP151-EP also achieves ultralow noise performance without compromising PSRR or transient line and load performance. The low 265 µA of quiescent current at 200 mA load makes the ADP151-EP suitable for battery-operated portable equipment.

The ADP151-EP also includes an internal pull-down resistor on the EN input.

The ADP151-EP is specifically designed for stable operation with tiny 1 µF, ±30% ceramic input and output capacitors to meet the requirements of high performance, space constrained applications.

The ADP151-EP is capable of 16 fixed output voltage options, ranging from 1.1 V to 3.3 V.

Short-circuit and thermal overload protection circuits prevent damage in adverse conditions. The ADP151-EP is available in a tiny 5-lead TSOT package.

Additional application and technical information can be found in the ADP151 data sheet.

Rev. 0

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REVISION HISTORY

7/12—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = (V_{OUT} + 0.4 V) or 2.2 V, whichever is greater; EN = V_{IN}, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −55°C to +125°C	2.2		5.5	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 0 µA		10		µA
		I_{OUT} = 0 µA, T_J = −55°C to +125°C			20	µA
		I_{OUT} = 100 µA		20		µA
		I_{OUT} = 100 µA, T_J = −55°C to +125°C			40	µA
		I_{OUT} = 10 mA		60		µA
		I_{OUT} = 10 mA, T_J = −55°C to +125°C			90	µA
		I_{OUT} = 200 mA		265		µA
		I_{OUT} = 200 mA, T_J = −55°C to +125°C			350	µA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND		0.2		µA
		EN = GND, T_J = −55°C to +125°C			1.0	µA
OUTPUT VOLTAGE ACCURACY						
	V_{OUT}	I_{OUT} = 10 mA	−1		+1	%
	V_{OUT}	T_J = −55°C to +125°C				
		V_{OUT} < 1.8 V				
		100 µA < I_{OUT} < 200 mA, V_{IN} = (V_{OUT} + 0.4 V) to 5.5 V	−3		+3	%
		V_{OUT} ≥ 1.8 V				
		100 µA < I_{OUT} < 200 mA, V_{IN} = (V_{OUT} + 0.4 V) to 5.5 V	−2.5		+3	%
REGULATION						
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.4 V) to 5.5 V, T_J = −55°C to +125°C	−0.05		+0.05	%/V
Load Regulation[1]	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{OUT} < 1.8 V				%/mA
		I_{OUT} = 100 µA to 200 mA		0.006		%/mA
		I_{OUT} = 100 µA to 200 mA, T_J = −55°C to +125°C			0.012	%/mA
		V_{OUT} ≥ 1.8 V				
		I_{OUT} = 100 µA to 200 mA		0.003		%/mA
		I_{OUT} = 100 µA to 200 mA, T_J = −55°C to +125°C			0.008	%/mA
DROPOUT VOLTAGE[2]	$V_{DROPOUT}$	I_{OUT} = 10 mA		10		mV
		I_{OUT} = 10 mA, T_J = −55°C to +125°C			30	mV
		I_{OUT} = 200 mA		150		mV
		I_{OUT} = 200 mA, T_J = −55°C to +125°C			230	mV
START-UP TIME[3]	$t_{START-UP}$	VOUT = 3.3 V		180		µs
CURRENT-LIMIT THRESHOLD[4]	I_{LIMIT}	T_J = 0°C to +125°C	220	300	400	mA
UNDERVOLTAGE LOCKOUT		T_J = −55°C to +125°C				
Input Voltage Rising	$UVLO_{RISE}$				1.96	V
Input Voltage Falling	$UVLO_{FALL}$		1.28			V
Hysteresis	$UVLO_{HYS}$			120		mV
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
EN INPUT						
EN Input Logic High	V_{IH}	2.2 V ≤ V_{IN} ≤ 5.5 V	1.2			V
EN Input Logic Low	V_{IL}	2.2 V ≤ V_{IN} ≤ 5.5 V			0.4	V
EN Input Pull-Down Resistance	R_{EN}	V_{IN} = V_{EN} = 5.5 V		2.6		MΩ
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 3.3 V		9		µV rms
		10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 2.5 V		9		µV rms
		10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 1.1 V		9		µV rms

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY REJECTION RATIO	PSRR					
$V_{IN} = V_{OUT} + 0.5$ V		10 kHz, V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 10 mA		70		dB
		100 kHz, V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 10 mA		55		dB
$V_{IN} = V_{OUT} + 1$ V		10 kHz, V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 10 mA		70		dB
		100 kHz, V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 10 mA		55		dB
		10 kHz, V_{IN} = 2.2 V, V_{OUT} = 1.1 V, I_{OUT} = 10 mA		70		dB
		100 kHz, V_{IN} = 2.2 V, V_{OUT} = 1.1 V, I_{OUT} = 10 mA		55		dB

[1] Based on an end-point calculation using 0.1 mA and 200 mA loads. See Figure 4 for typical load regulation performance for loads less than 1 mA.
[2] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 2.2 V.
[3] Start-up time is defined as the time between the rising edge of EN and V_{OUT} being at 90% of its nominal value.
[4] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V (that is, 2.7 V).

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Minimum Input and Output Capacitance[1]	C_{MIN}	T_A = −55°C to +125°C	0.7			µF
Capacitor ESR	R_{ESR}	T_A = −55°C to +125°C	0.001		0.2	Ω

[1] The minimum input and output capacitance should be greater than 0.7 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	−0.3 V to +6.5 V
VOUT to GND	−0.3 V to VIN
EN to GND	−0.3 V to +6.5 V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−55°C to +125°C
Operating Ambient Temperature Range	−55°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP151-EP can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

The maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

The junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 in. × 3 in. circuit board. See JESD51-7 for detailed information on the board construction.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

See JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
5-Lead TSOT	174	43	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

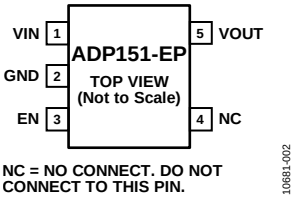

Figure 2. 5-Lead TSOT Pin Configuration

Table 5. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	VIN	Regulator Input Supply. Bypass VIN to GND with a 1 µF or greater capacitor.
2	GND	Ground.
3	EN	Enable Input. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
4	NC	No Connect. Not connected internally.
5	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 1 µF or greater capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

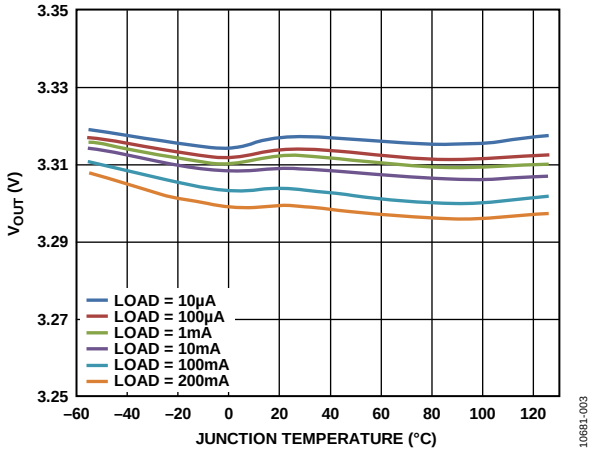

Figure 3. Output Voltage vs. Junction Temperature

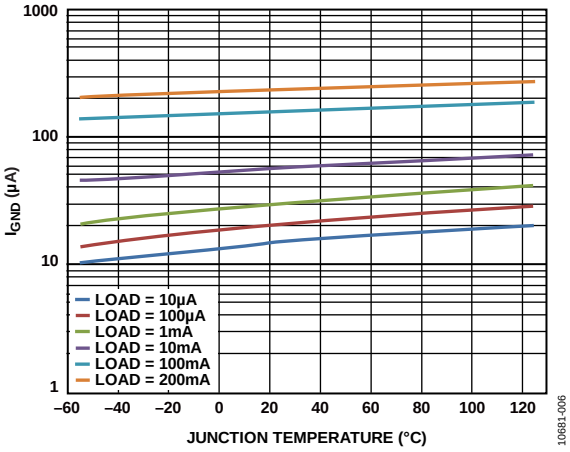

Figure 6. Ground Current vs. Junction Temperature

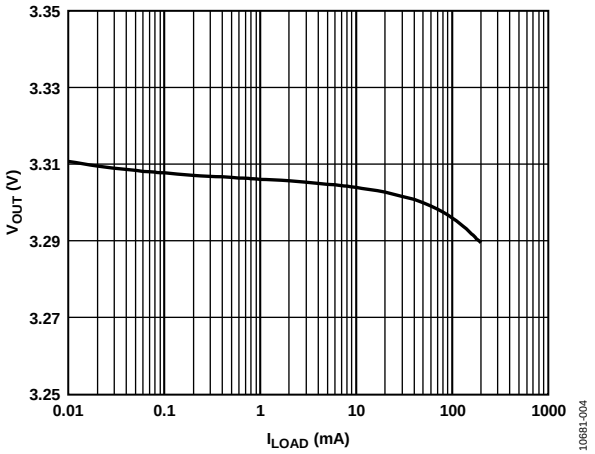

Figure 4. Output Voltage vs. Load Current

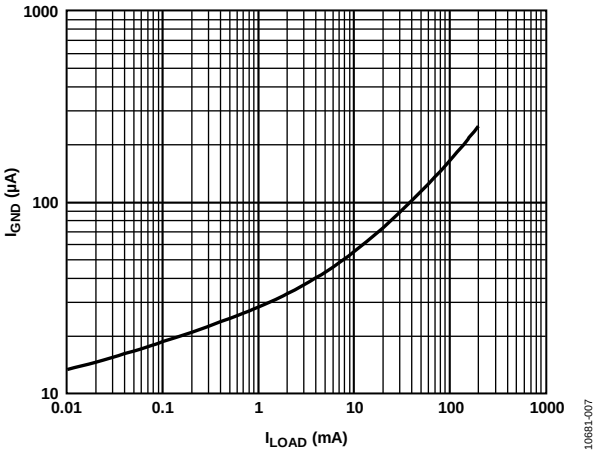

Figure 7. Ground Current vs. Load Current

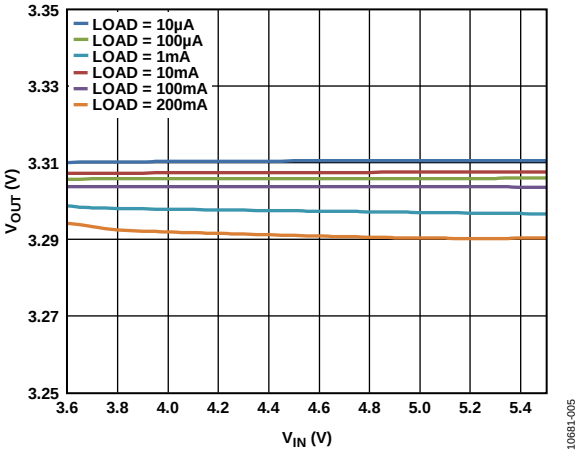

Figure 5. Output Voltage vs. Input Voltage

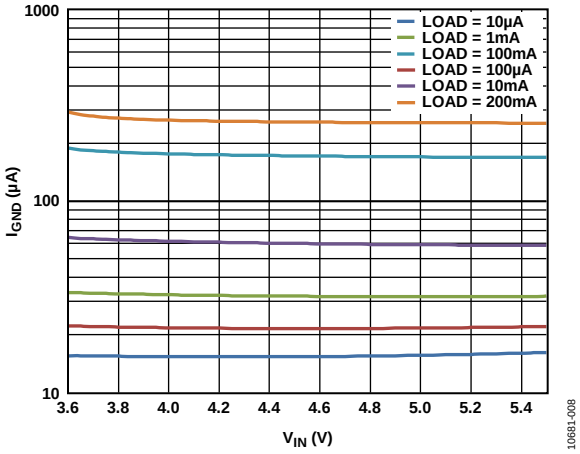

Figure 8. Ground Current vs. Input Voltage

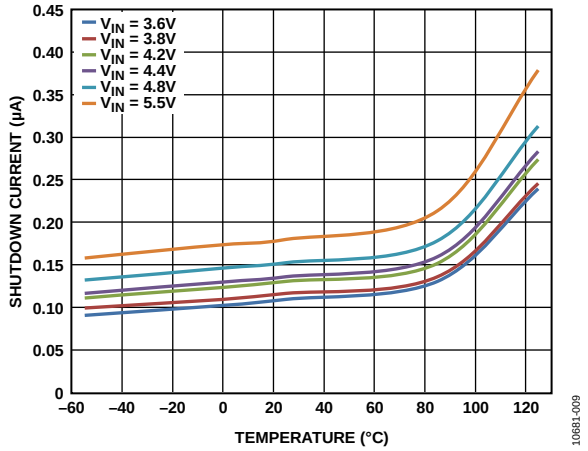

Figure 9. Shutdown Current vs. Temperature at Various Input Voltages

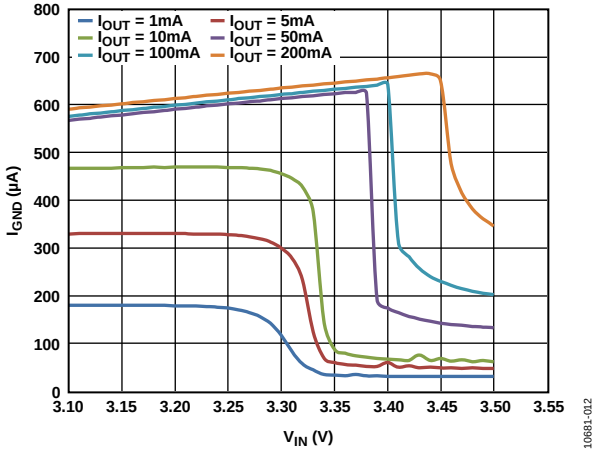

Figure 12. Ground Current vs. Input Voltage (in Dropout)

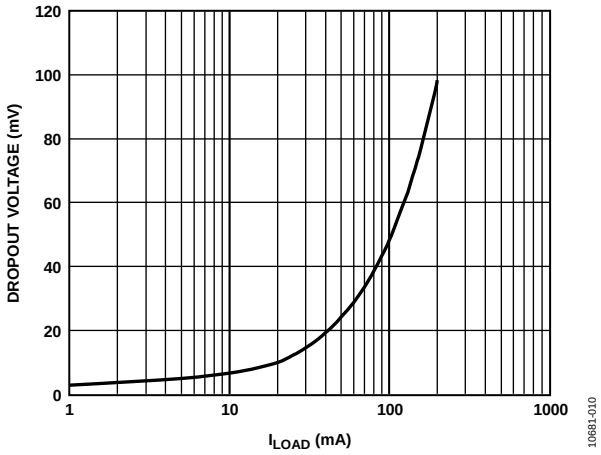

Figure 10. Dropout Voltage vs. Load Current

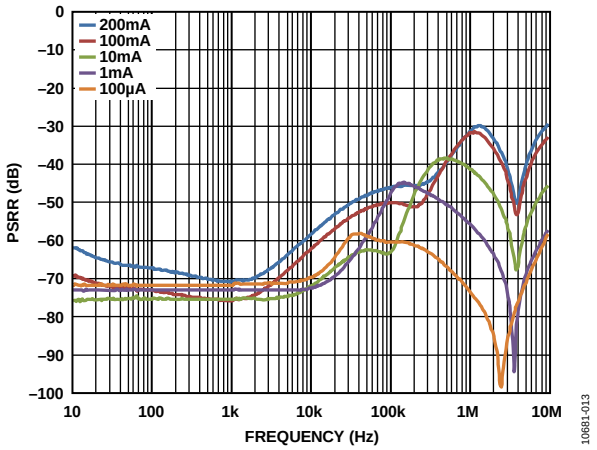

Figure 13. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 1.2 V, V_{IN} = 2.2 V

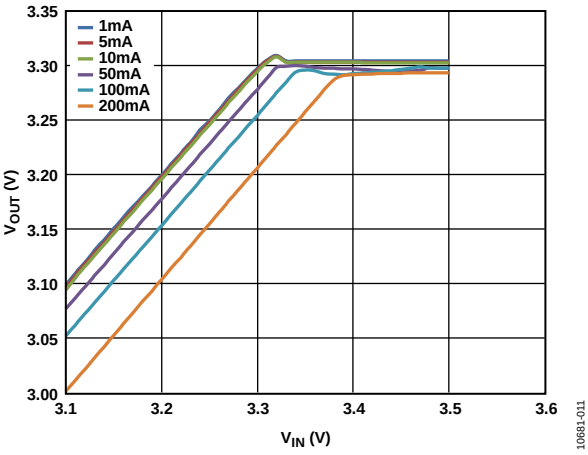

Figure 11. Output Voltage vs. Input Voltage (in Dropout)

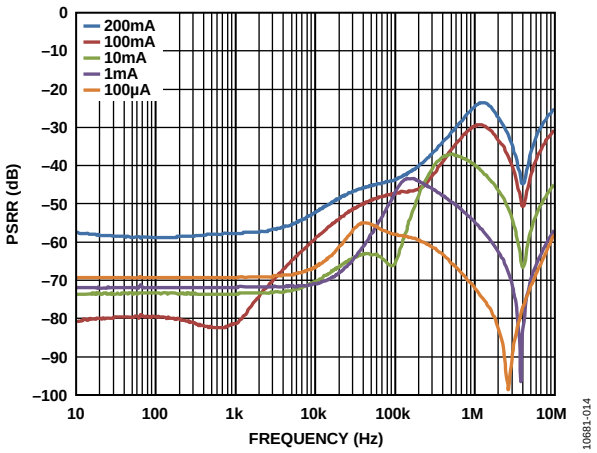

Figure 14. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 2.8 V, V_{IN} = 3.3 V

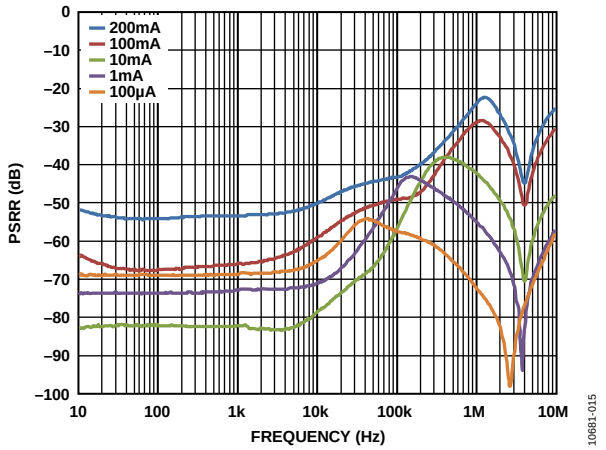

Figure 15. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 3.3 V, V_{IN} = 3.8 V

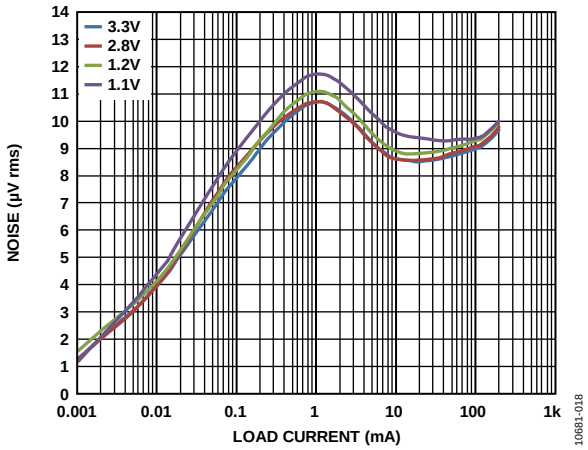

Figure 18. Output Noise vs. Load Current and Output Voltage, V_{IN} = 5 V, C_{OUT} = 1 µF

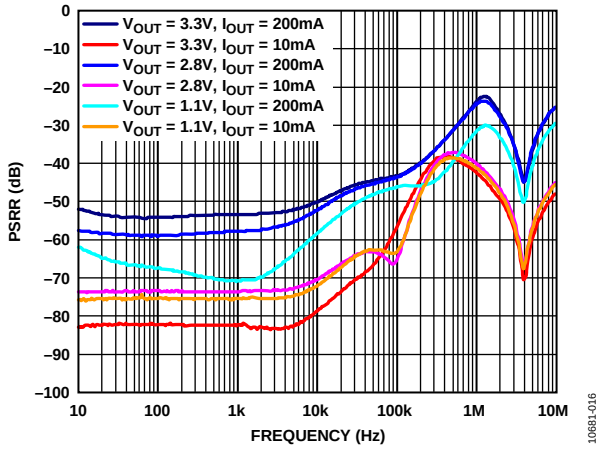

Figure 16. Power Supply Rejection Ratio vs. Frequency at Various Output Voltages and Load Currents, $V_{OUT} - V_{IN}$ = 0.5 V, except for V_{OUT} = 1.1 V, V_{IN} = 2.2 V

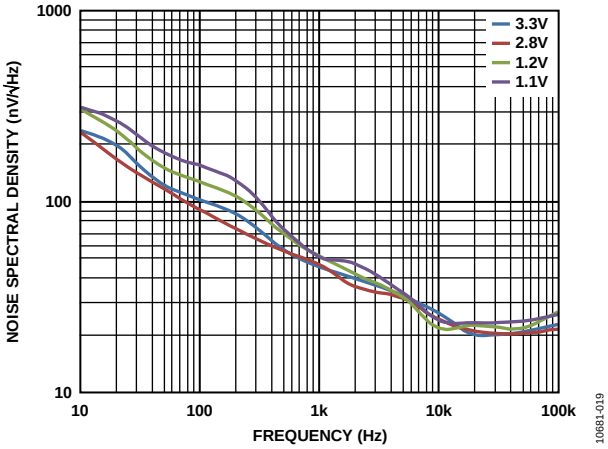

Figure 19. Output Noise Spectral Density vs. Frequency, V_{IN} = 5 V, I_{LOAD} = 10 mA, C_{OUT} = 1 µF

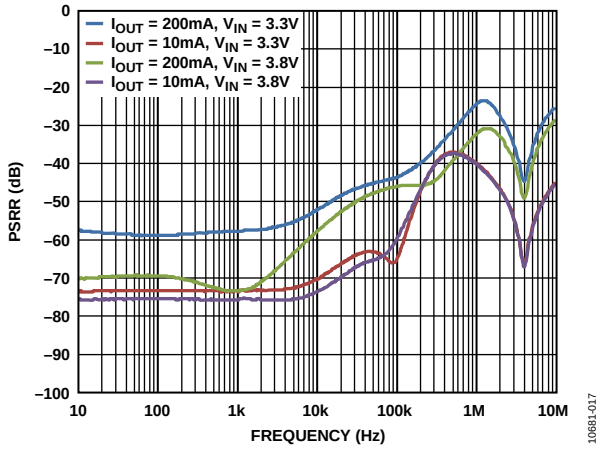

Figure 17. Power Supply Rejection Ratio vs. Frequency at Various Voltages and Load Currents, V_{OUT} = 2.8 V

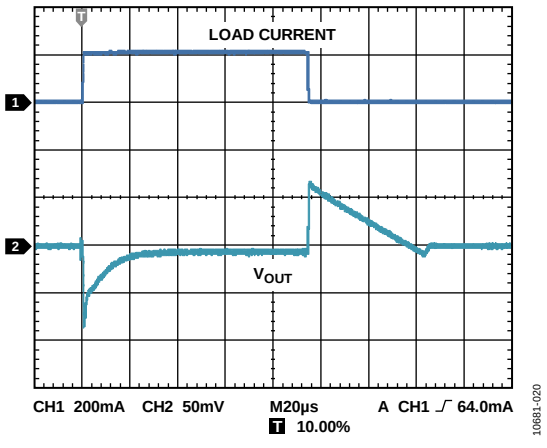

Figure 20. Load Transient Response, C_{IN}, C_{OUT} = 1 µF, I_{LOAD} = 1 mA to 200 mA

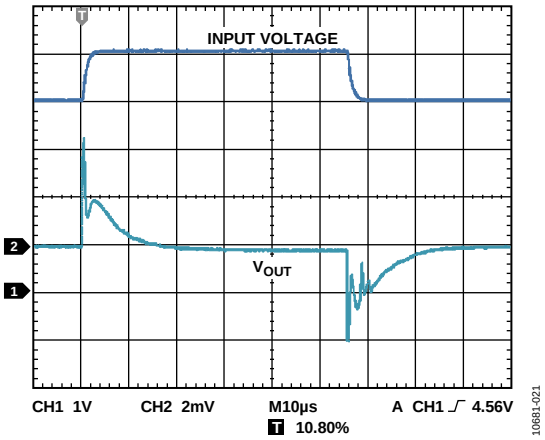

Figure 21. Line Transient Response, C_{IN}, C_{OUT} = 1 µF, I_{LOAD} = 200 mA

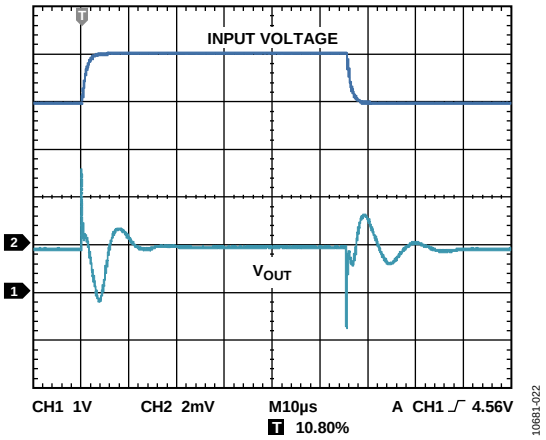

Figure 22. Line Transient Response, C_{IN}, C_{OUT} = 1 µF, I_{LOAD} = 1 mA

APPLICATIONS INFORMATION

THERMAL CONSIDERATIONS

In most applications, the ADP151-EP does not dissipate much heat due to its high efficiency. However, in applications with a high ambient temperature and a high supply voltage to output voltage differential, the heat dissipated in the package can cause the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 150°C, the converter enters thermal shutdown. It recovers only after the junction temperature has decreased below 135°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is very important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 1.

To guarantee reliable operation, the junction temperature of the ADP151-EP must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds that are used and the amount of copper used to solder the package GND pins to the PCB.

Table 6 shows typical θ_{JA} values of the 5-lead TSOT for various PCB copper sizes. Table 7 shows the typical Ψ_{JB} values of the 5-lead TSOT.

Table 6. Typical θ_{JA} Values

Copper Size (mm²)	θ_{JA} (°C/W)
0[1]	174
50	156
100	150
300	138
500	135

[1] Device soldered to minimum size pin traces.

Table 7. Typical Ψ_{JB} Values

Model	Ψ_{JB} (°C/W)
TSOT	43

The junction temperature of the ADP151-EP can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (2)$$

where:
I_{LOAD} is the load current.
I_{GND} is the ground current.
V_{IN} and V_{OUT} are input and output voltages, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (3)$$

As shown in Equation 3, for a given ambient temperature, input-to-output voltage differential and continuous load current, there exists a minimum copper size requirement for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 23 through Figure 28 shows junction temperature calculations for various ambient temperatures, load currents, V_{IN}-to-V_{OUT} differentials, and areas of PCB copper.

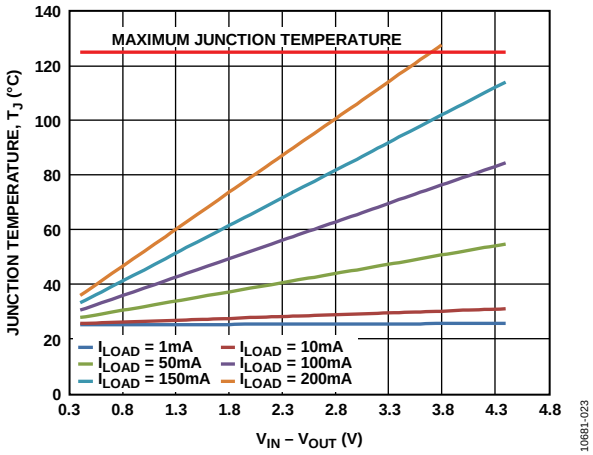

Figure 23. TSOT 500 mm² of PCB Copper, T_A = 25°C

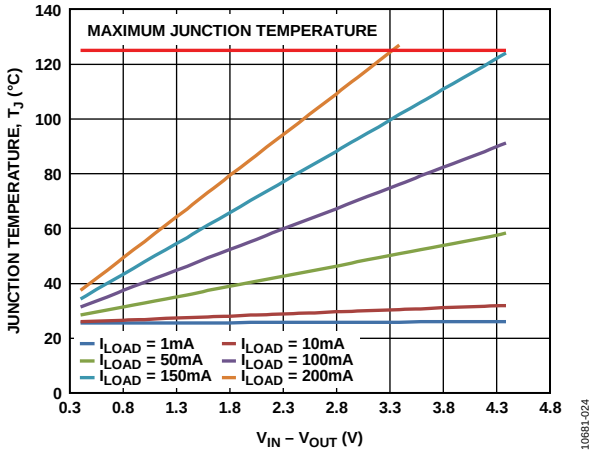

Figure 24. TSOT 100 mm² of PCB Copper, T_A = 25°C

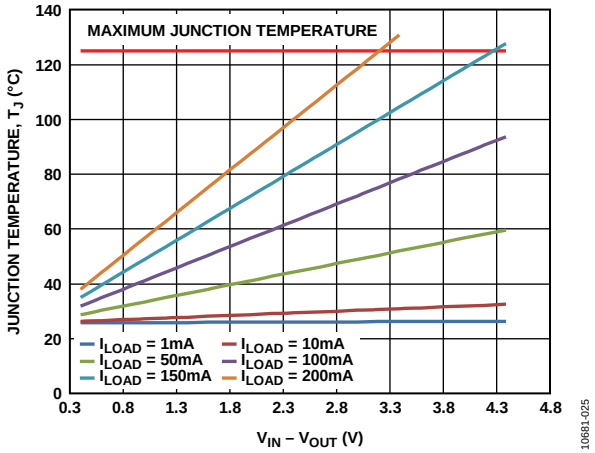

Figure 25. TSOT 50 mm² of PCB Copper, T_A = 25°C

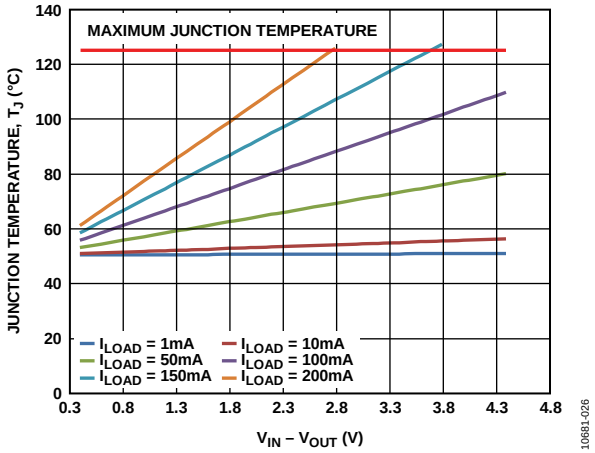

Figure 26. TSOT 500 mm² of PCB Copper, T_A = 50°C

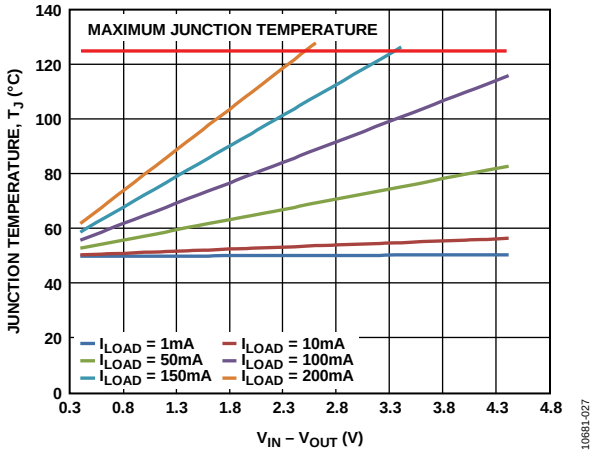

Figure 27. TSOT 100 mm² of PCB Copper, T_A = 50°C

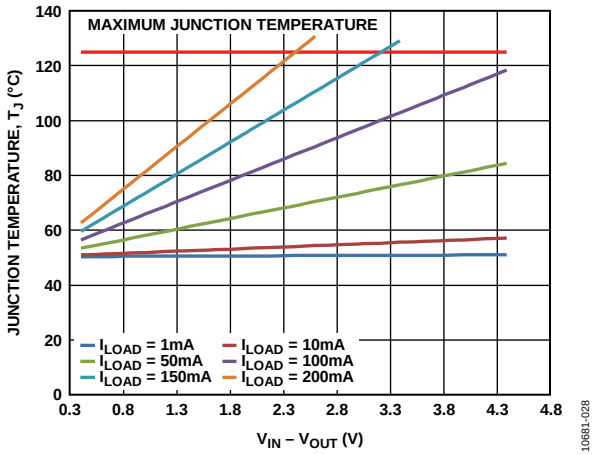

Figure 28. TSOT 50 mm² of PCB Copper, T_A = 50°C

In the case where the board temperature is known, use the thermal characterization parameter, Ψ_{JB}, to estimate the junction temperature rise (see Figure 29). Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (4)$$

The typical value of Ψ_{JB} is 43°C/W for the 5-lead TSOT package.

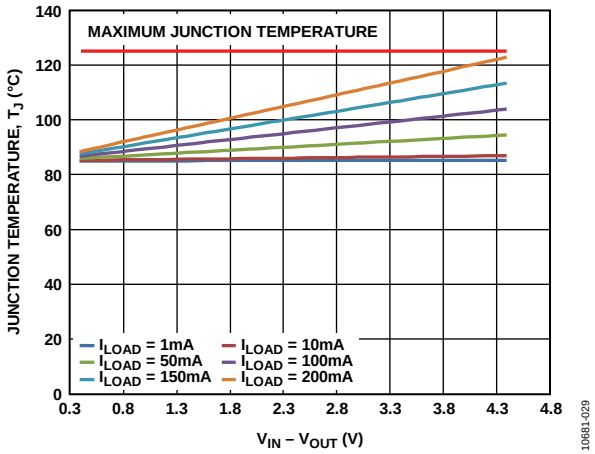

Figure 29. TSOT, T_A = 85°C

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP151-EP. However, as listed in Table 6, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Use of 0402 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

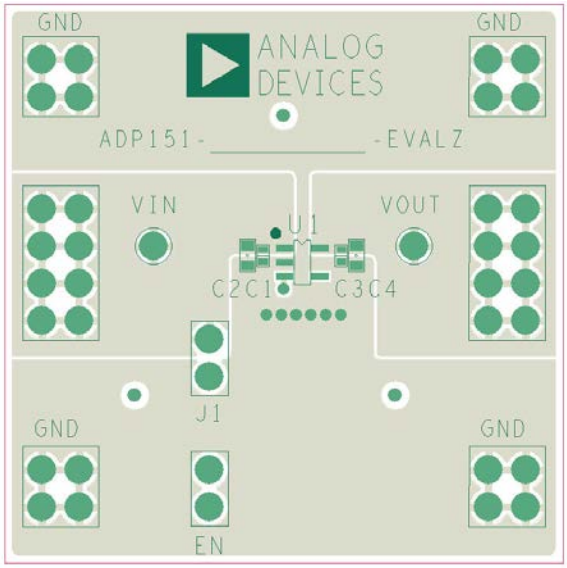

Figure 30. Example TSOT PCB Layout

OUTLINE DIMENSIONS

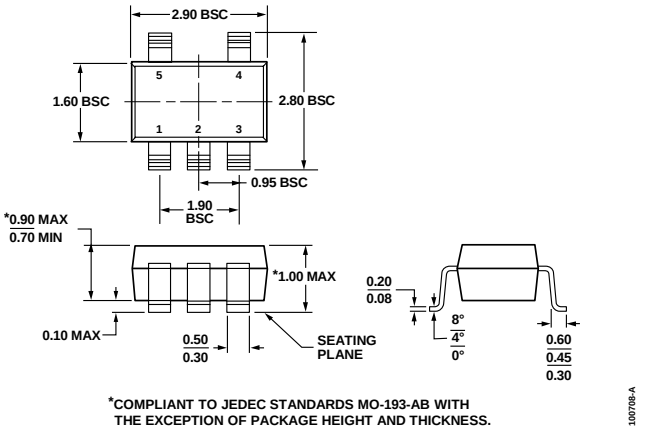

Figure 31. 5-Lead Thin Small Outline Transistor Package [TSOT] (UJ-5)
Dimensions show in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)[2]	Package Description	Package Option	Branding
ADP151TUJZ3.3-EPR2	−55°C to +125°C	3.3	5-Lead TSOT	UJ-5	LJ2

[1] Z = RoHS Compliant Part.
[2] For additional voltage options for the ADP151TUJZ package option, contact a local Analog Devices, Inc., sales or distribution representative.

NOTES

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