150 µV Maximum Offset Voltage Op Amp

OP07D

FEATURES

Low offset voltage: 150 µV max
Input offset drift: 1.5 µV/°C max
Low noise: 0.25 µV p-p
High gain CMRR and PSRR: 115 dB min
Low supply current: 1.1 mA
Wide supply voltage range: ±4 V to ±18 V operation

APPLICATIONS

Medical and industrial instrumentation
Sensors and controls
- **Thermocouple**
- **RTDs**
- **Strain bridges**
- **Shunt current measurements**

Precision filters

GENERAL DESCRIPTION

The OP07D is a precision, ultralow offset amplifier. It integrates low power (1.1 mA typical), low input bias current (±1 nA maximum), and high CMRR/PSRR (130 dB) in the small DIP package. Operation is fully specified from ±5 V to ±15 V supply.

The OP07D provides higher accuracy than industry-standard OP07-type amplifiers due to Analog Devices' iPolar™ process, which supports enhanced performance in a smaller footprint. These performance enhancements include wider output swing, lower power, and higher CMRR (common-mode rejection ratio) and PSRR (power supply rejection ratio). The OP07D maintains stability of offsets and gain virtually regardless of variations in time or temperature. Excellent linearity and gain accuracy can be maintained at high closed-loop gains.

The OP07D is fully specified over the extended industrial temperature range of −40°C to +125°C. The OP07D amplifier is available in 8-lead DIP and the popular 8-lead, narrow SOIC lead-free packages.

PIN CONFIGURATIONS

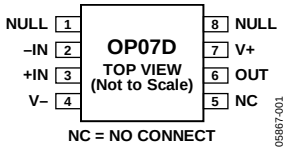

Figure 1. 8-Lead SOIC_N (R-8), 8-Lead DIP (N-8)

Rev. A

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REVISION HISTORY

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Changes to Figure 42 12
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Changes to Ordering Guide 14

12/05—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±5.0 V, T_A = 25°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			40	150	µV
		0°C ≤ T_A ≤ 70°C			250	µV
		−40°C ≤ T_A ≤ +125°C			350	µV
Input Bias Current	I_B			0.2	1	nA
		−40°C ≤ T_A ≤ +125°C			1	nA
Input Offset Current	I_{OS}			0.1	1	nA
		−40°C ≤ T_A ≤ +125°C			1	nA
Input Voltage Range			−3.5		+3.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3 V	120	127		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Open-Loop Gain	A_{VO}	R_L = 2 kΩ to ground, V_O = ±3 V	1000	10,000		V/mV
		−40°C ≤ T_A ≤ +125°C	1000			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	0°C ≤ T_A ≤ 70°C		0.5	1.8	µV/°C
		−40°C ≤ T_A ≤ +125°C		0.5	1.4	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_{OUT}	R_L = 10 kΩ to ground	±3.95	±4.1		V
		−40°C ≤ T_A ≤ +125°C	±3.95			V
		R_L = 2 kΩ to ground	±3.9	±4		V
		−40°C ≤ T_A ≤ +125°C	±3.9			V
Short-Circuit Current	I_{SC}			27		mA
Output Current	I_O	V_O = 3.5 V		15		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.0 V to ±18.0 V	115	130		dB
		0°C ≤ T_A ≤ 70°C	115			dB
		−40°C ≤ T_A ≤ +125°C	110			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		1.1	1.25	mA
		0°C ≤ T_A ≤ 70°C			1.45	mA
		−40°C ≤ T_A ≤ +125°C			1.75	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.2		V/µs
Gain Bandwidth Product	GBP			0.6		MHz
Phase Margin				80		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		0.28		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		10		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.074		pA/√Hz

V_S = ±15 V, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			45	150	µV
		0°C ≤ T_A ≤ 70°C			250	µV
		−40°C ≤ T_A ≤ +125°C			350	µV
Input Bias Current	I_B			0.2	1	nA
		−40°C ≤ T_A ≤ +125°C			1	nA
Input Offset Current	I_{OS}			0.2	1	nA
		−40°C ≤ T_A ≤ +125°C			1	nA
Input Voltage Range			−13.5		+13.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13.0 V	120	140		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Open-Loop Gain	A_{VO}	R_L = 2 kΩ to ground, V_O = ±11 V	1000	10,000		V/mV
		−40°C ≤ T_A ≤ +125°C	1000			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	0°C ≤ T_A ≤ 70°C		0.5	2.5	µV/°C
		−40°C ≤ T_A ≤ +125°C		0.5	1.5	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_{OUT}	R_L = 10 kΩ to ground	±13.95	±14		V
		−40°C ≤ T_A ≤ +125°C	±13.9			V
		R_L = 2 kΩ to ground	±13.75	±13.8		V
		−40°C ≤ T_A ≤ +125°C	±13.7			V
Short-Circuit Current	I_{SC}			30		mA
Output Current	I_O	V_O = 13.5 V		15		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.0 V to ±18.0 V	115	130		dB
		0°C ≤ T_A ≤ 70°C	115			dB
		−40°C ≤ T_A ≤ +125°C	110			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		1.1	1.3	mA
		0°C ≤ T_A ≤ 70°C			1.55	mA
		−40°C ≤ T_A ≤ +125°C			1.85	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.2		V/µs
Gain Bandwidth Product	GBP			0.6		MHz
Phase Margin				80		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		0.25		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		10		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.074		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	±V supply
Differential Input Voltage	±0.7 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead DIP (N-8)	103	43	°C/W
8-Lead SOIC (R-8)	158	43	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

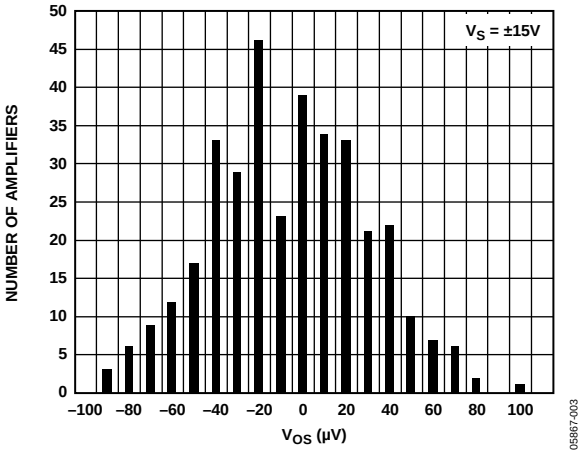


Figure 2. Number of Amplifiers vs. Offset Voltage

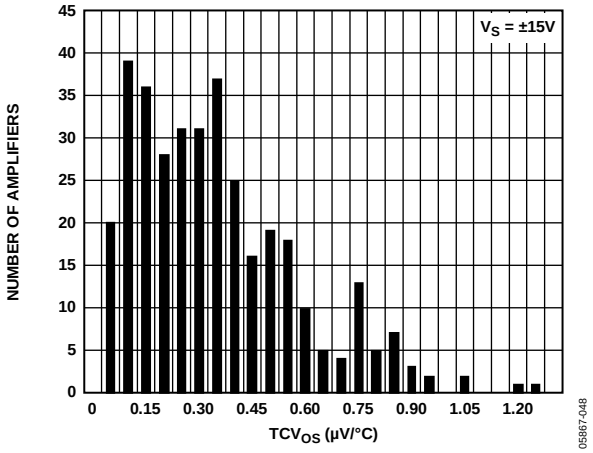


Figure 5. Number of Amplifiers vs. TCV_{OS}

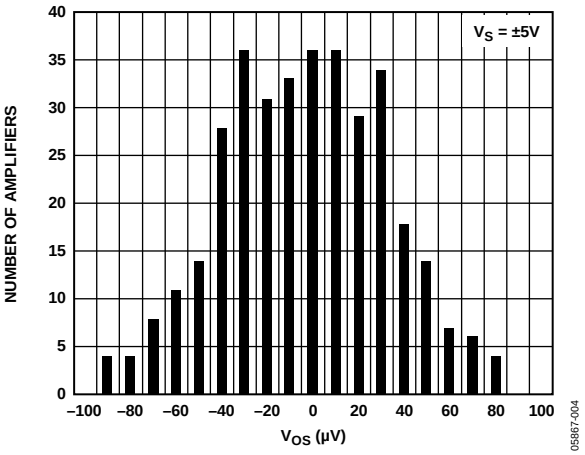


Figure 3. Number of Amplifiers vs. Offset Voltage

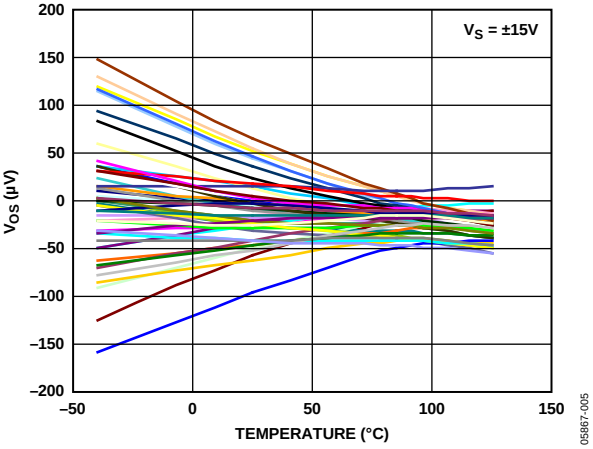


Figure 6. Offset Voltage vs. Temperature

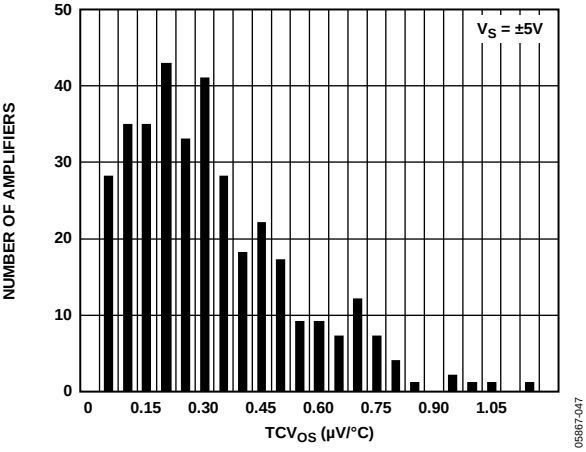


Figure 4. Number of Amplifiers vs. TCV_{OS}

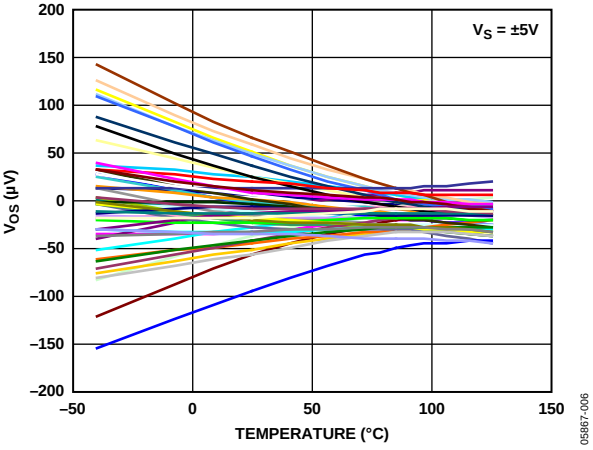


Figure 7. Offset Voltage vs. Temperature

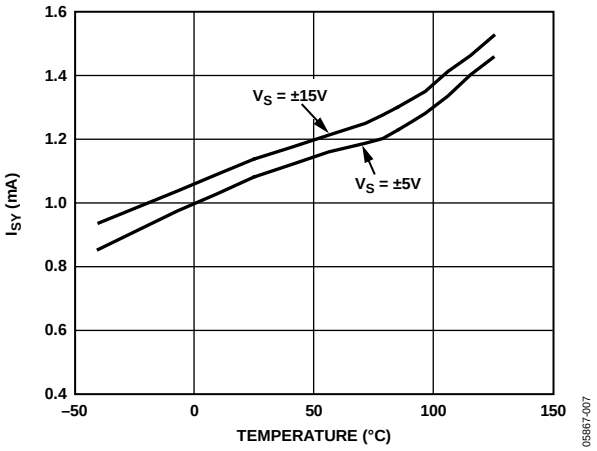


Figure 8. Supply Current vs. Temperature

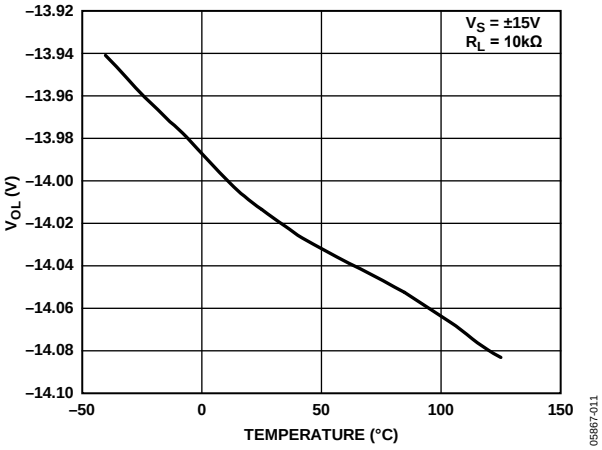


Figure 11. Negative Output Voltage Swing vs. Temperature

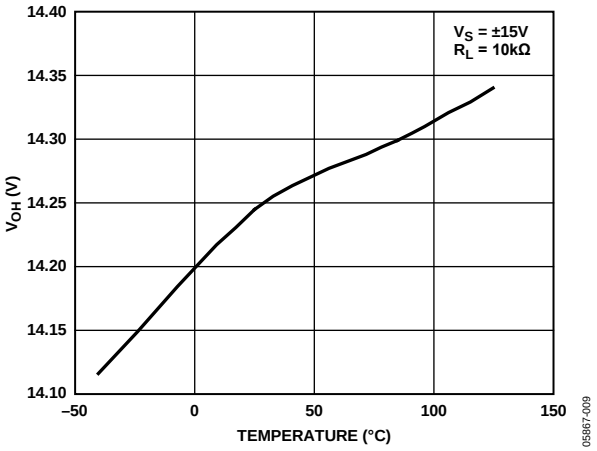


Figure 9. Positive Output Voltage Swing vs. Temperature

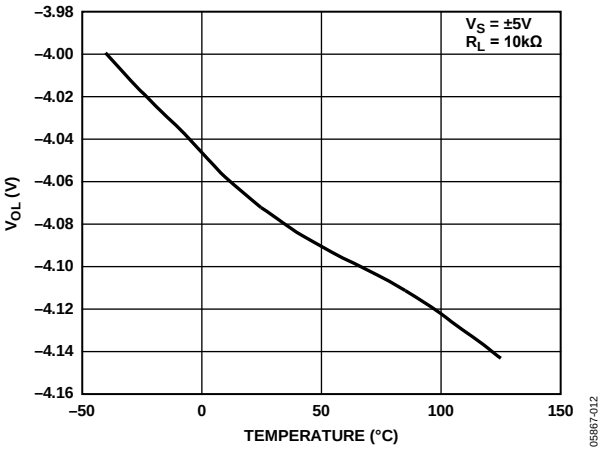


Figure 12. Negative Output Voltage Swing vs. Temperature

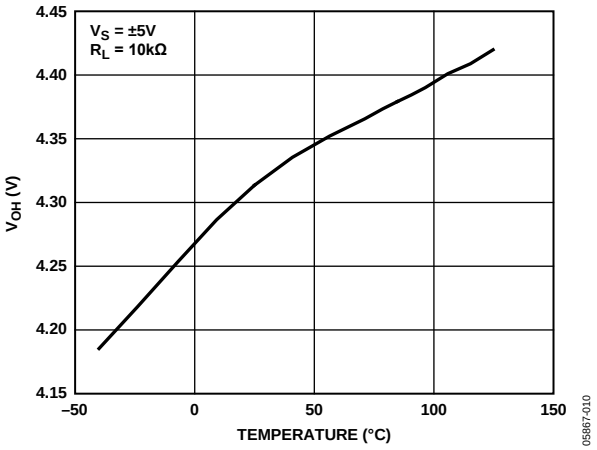


Figure 10. Positive Output Voltage Swing vs. Temperature

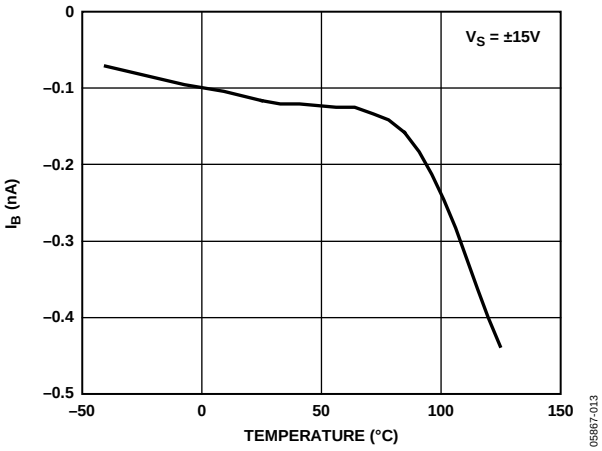


Figure 13. Input Bias Current vs. Temperature

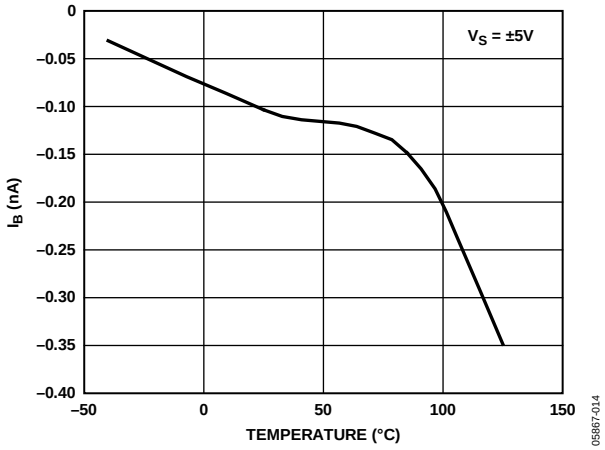


Figure 14. Input Bias Current vs. Temperature

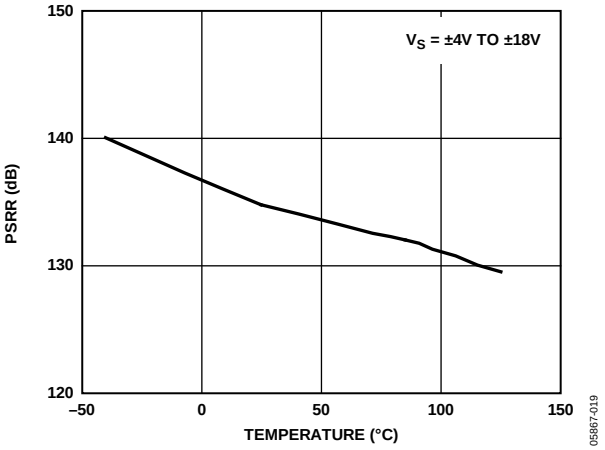


Figure 17. PSRR vs. Temperature

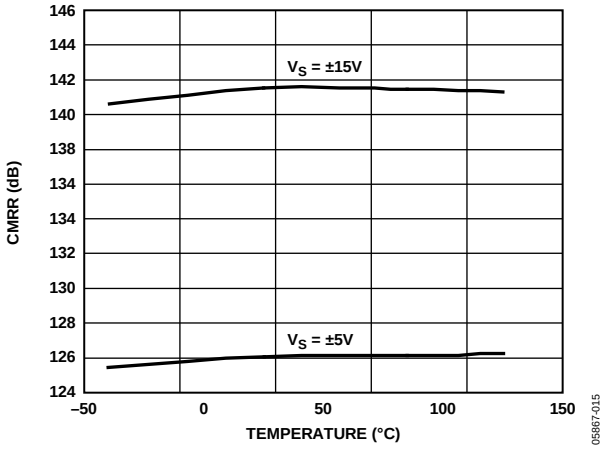


Figure 15. CMRR vs. Temperature

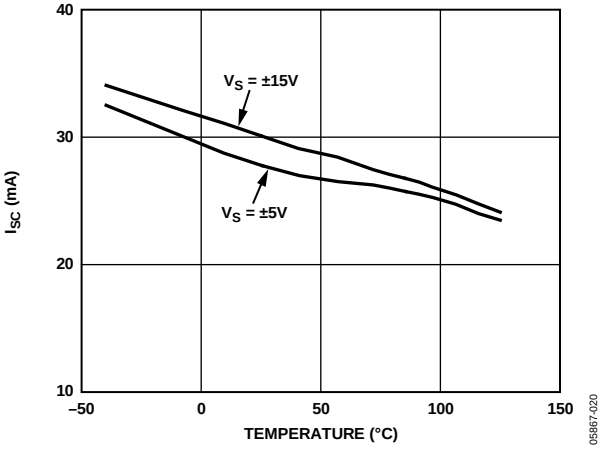


Figure 18. Short-Circuit Current vs. Temperature

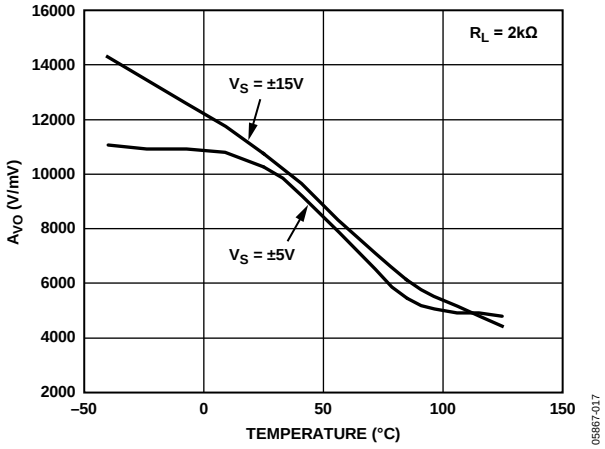


Figure 16. Open-Loop Gain vs. Temperature

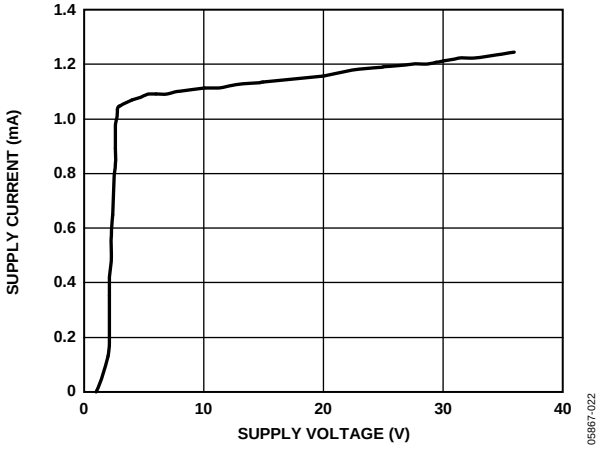


Figure 19. Supply Current vs. Supply Voltage

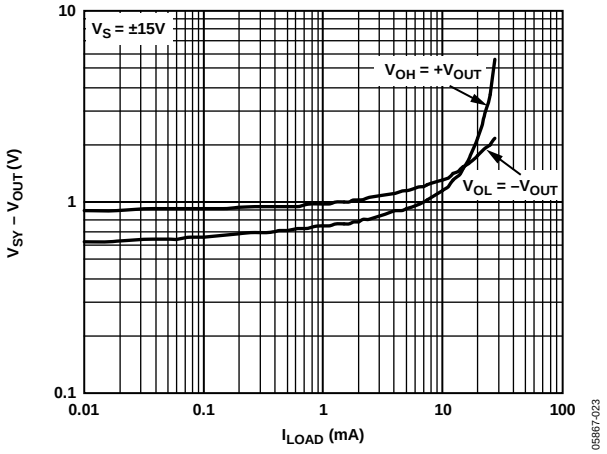


Figure 20. Output Voltage Swing vs. Load Current

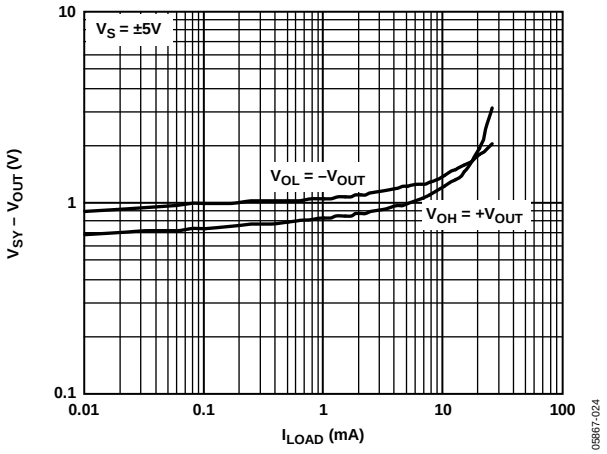


Figure 21. Output Voltage Swing vs. Load Current

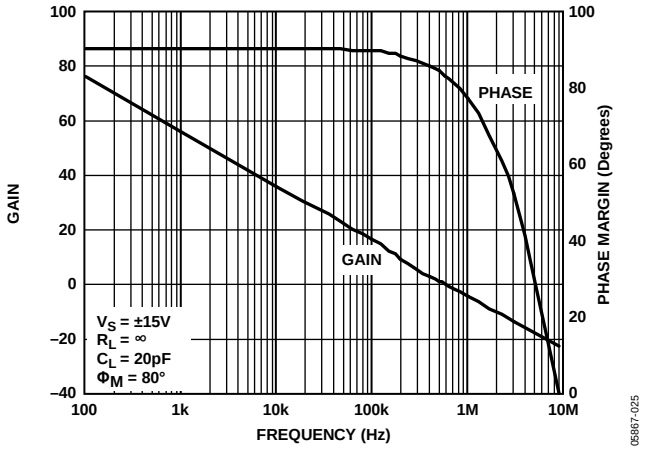


Figure 22. Open-Loop Gain and Phase vs. Frequency

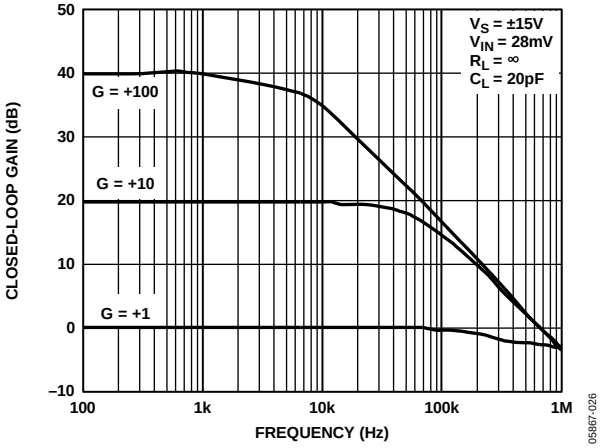


Figure 23. Closed-Loop Gain vs. Frequency

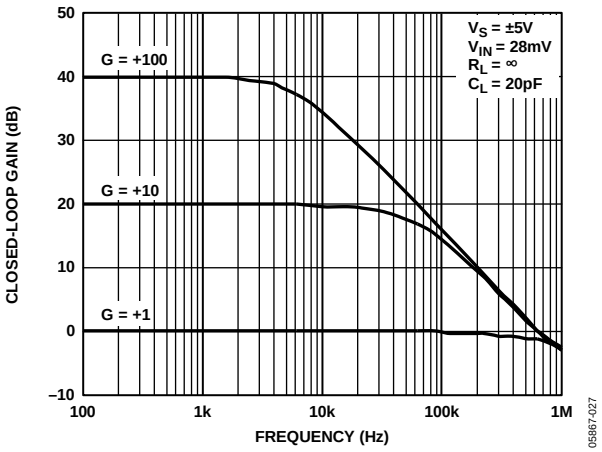


Figure 24. Closed-Loop Gain vs. Frequency

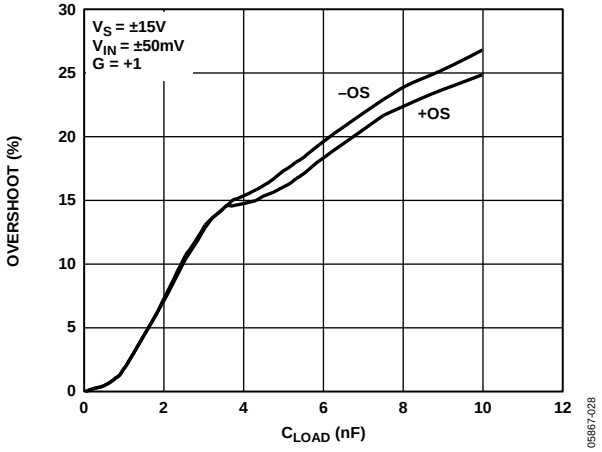


Figure 25. Overshoot vs. Capacitive Load

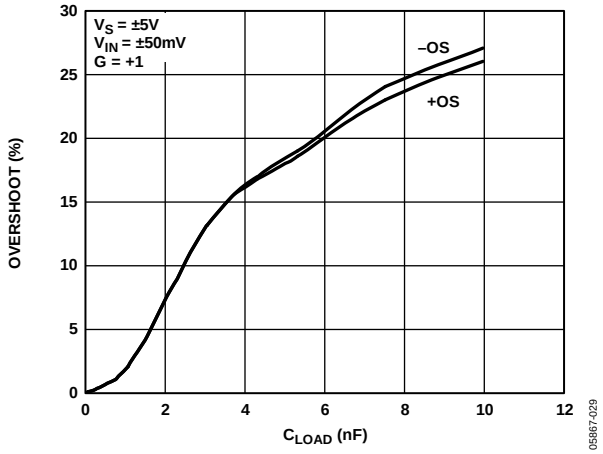


Figure 26. Overshoot vs. Capacitive Load

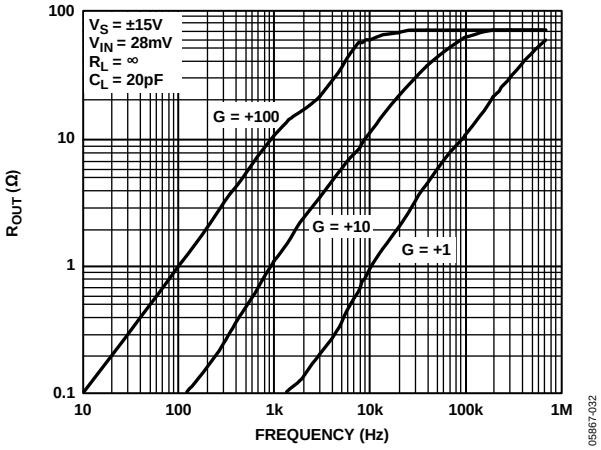


Figure 29. Output Impedance vs. Frequency

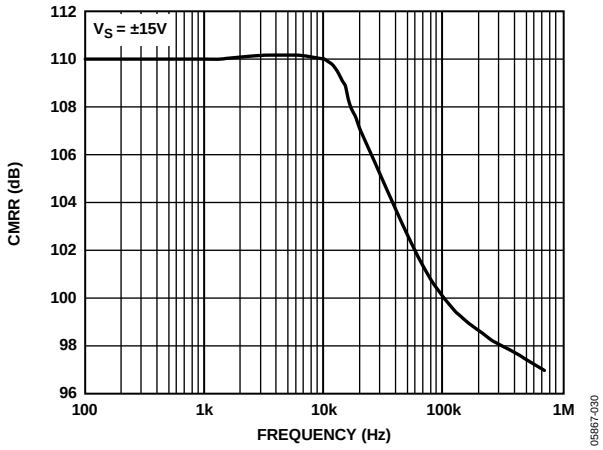


Figure 27. CMRR vs. Frequency

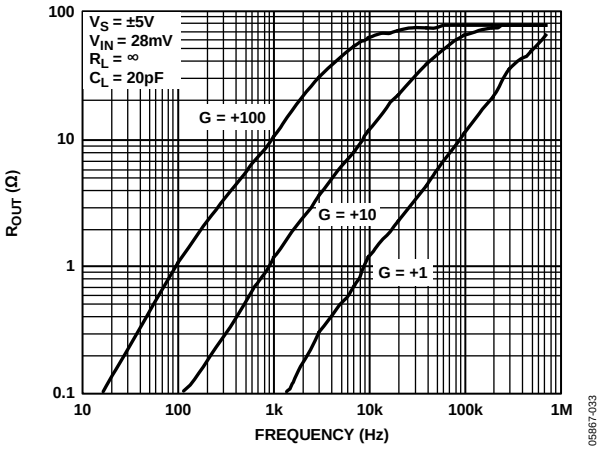


Figure 30. Output Impedance vs. Frequency

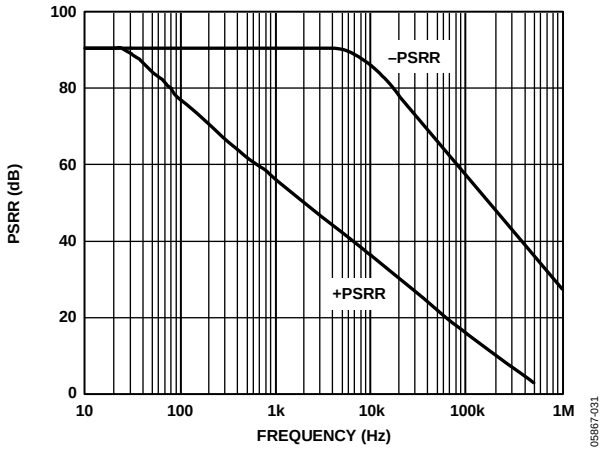


Figure 28. PSRR vs. Frequency

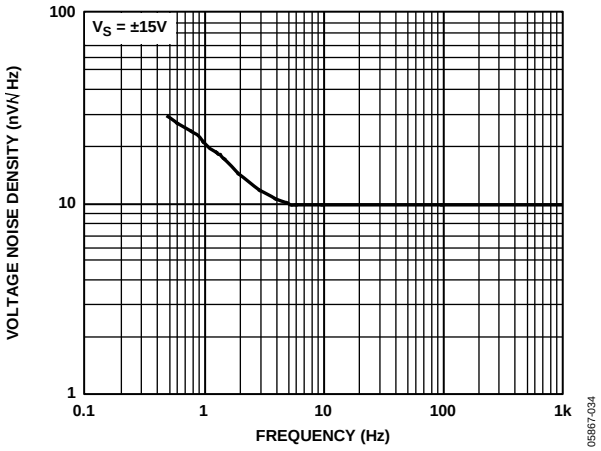


Figure 31. Voltage Noise Density vs. Frequency

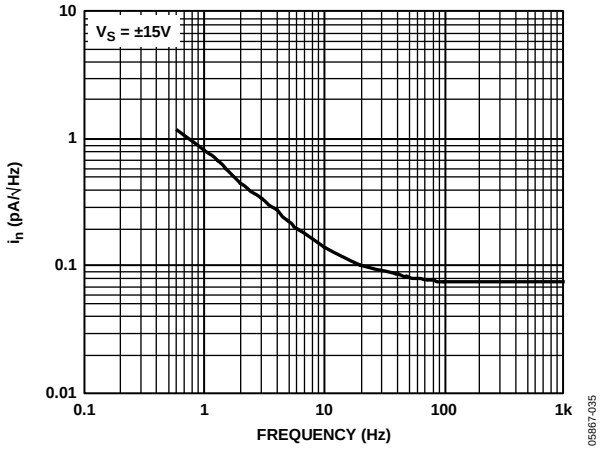


Figure 32. Current Noise Density vs. Frequency

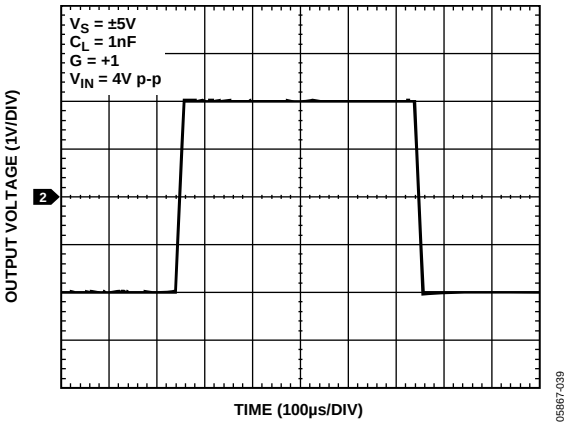


Figure 35. Large-Signal Transient

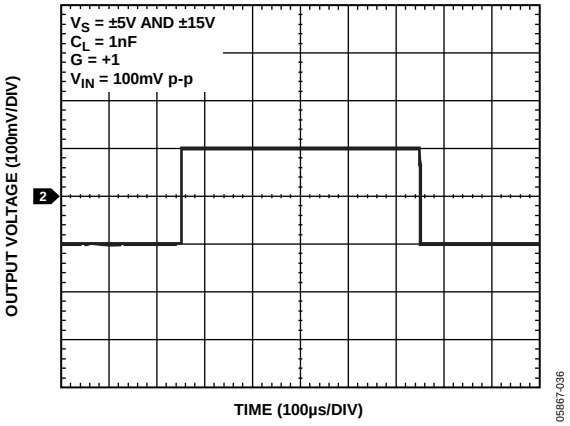


Figure 33. Small-Signal Transient

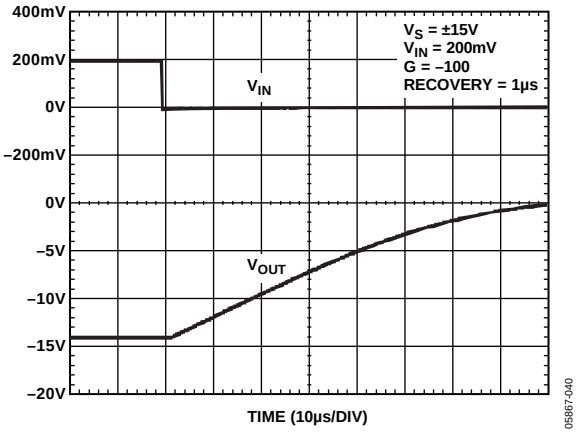


Figure 36. Positive Overload Recovery

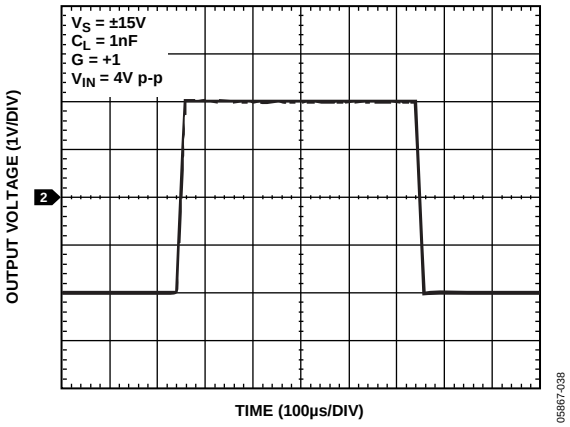


Figure 34. Large-Signal Transient

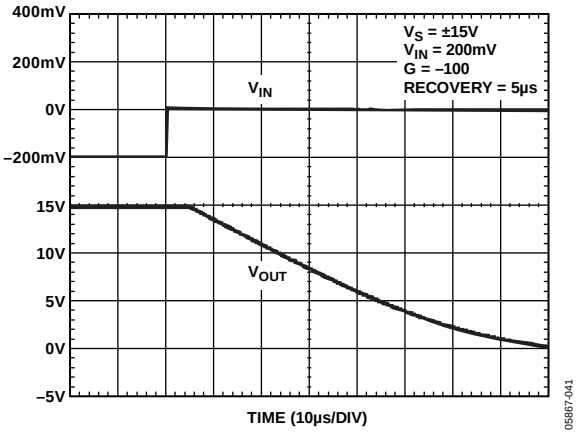


Figure 37. Negative Overload Recovery

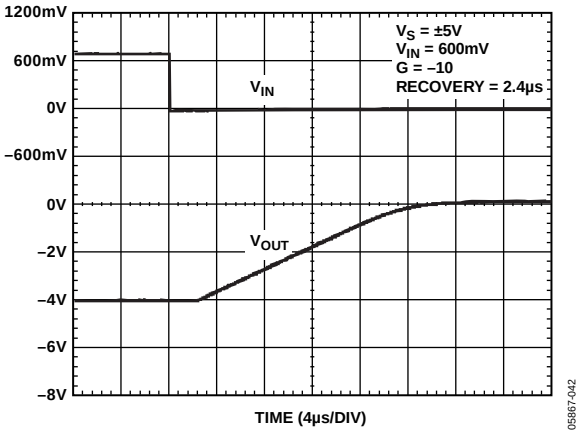


Figure 38. Positive Overload Recovery

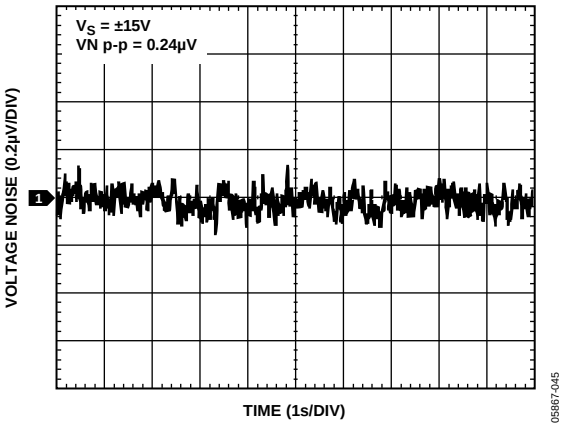


Figure 41. Voltage Noise (0.1 Hz to 10 Hz)

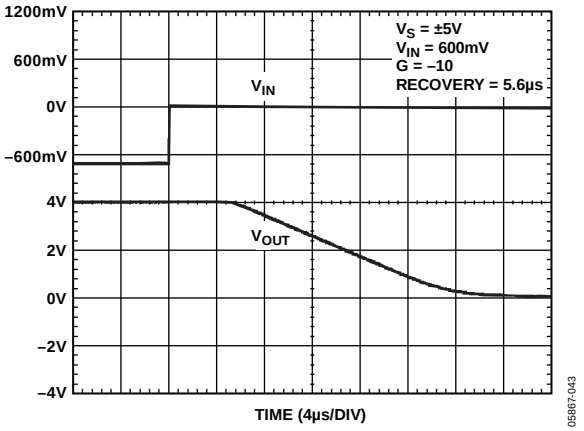


Figure 39. Negative Overload Recovery

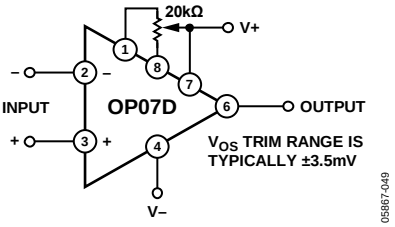


Figure 42. Optional Offset Nulling Circuit

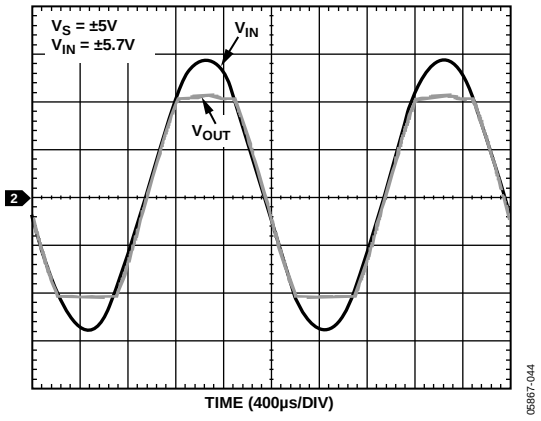
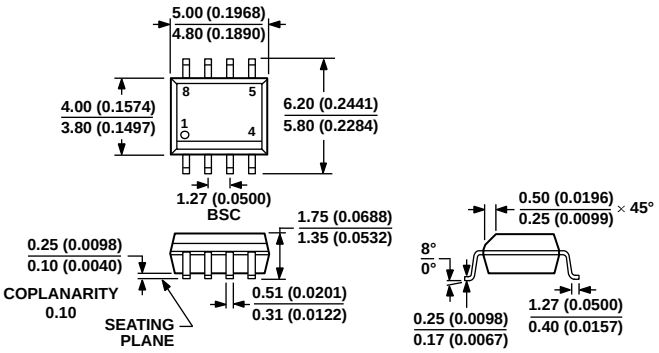


Figure 40. No Phase Reversal

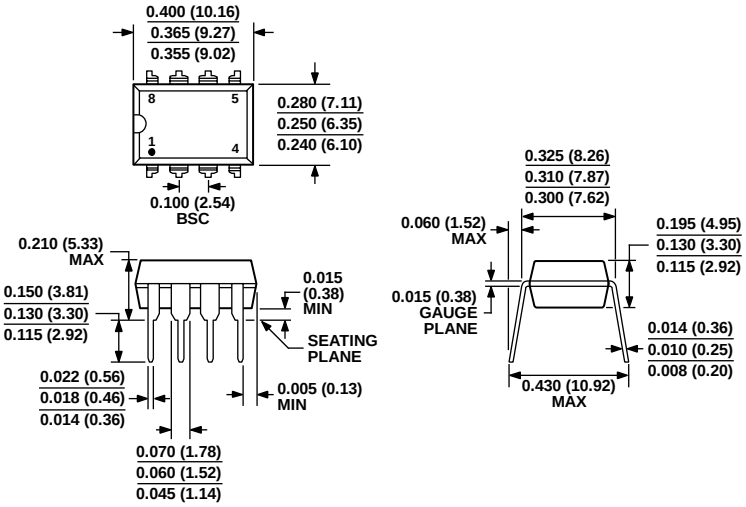
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 43. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 44. 8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
OP07DNZ	−40°C to +125°C	8-Lead PDIP	N-8
OP07DRZ	−40°C to +125°C	8-Lead SOIC_N	R-8
OP07DRZ-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8
OP07DRZ-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8

[1] Z = RoHS Compliant Part.

NOTES

NOTES

D05867–0–2/11(A)