Precision Rail-to-Rail Input and Output Op Amps

FEATURES

- **Rail-to-Rail Input and Output**
- **90μV $V_{OS(MAX)}$ for $V_{CM} = V^-$ to V^+**
- **High Common Mode Rejection Ratio: 97dB Min**
- **C-Load™ Stable Version (LT1219)**
- High A_{VOL}: 500V/mV Minimum Driving 10kΩ Load
- Wide Supply Range:
  2V to ±15V (LT1218/LT1219)
  2V to ±5V (LT1218L/LT1219L)
- Shutdown Mode: I_S < 30μA
- Low Supply Current: 420μA Max
- Low Input Bias Current: 18nA Typical
- 300kHz Gain-Bandwidth Product (LT1218)
- Slew Rate: 0.10V/μs (LT1218)

APPLICATIONS

- Driving A/D Converters
- Test Equipment Amplifiers
- MUX Amplifiers

DESCRIPTION

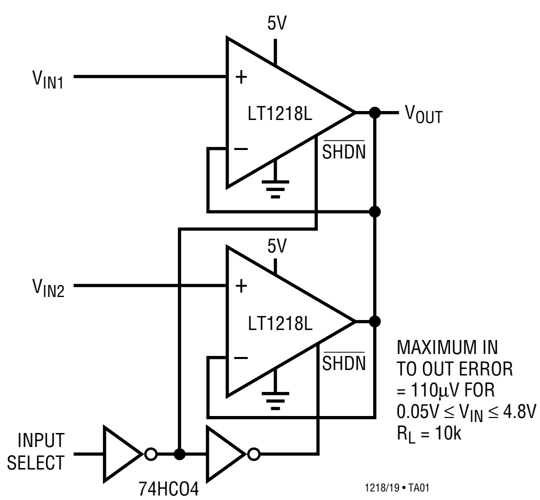
The LT®1218/LT1219 are bipolar op amps which combine rail-to-rail input and output operation with precision specifications. Unlike other rail-to-rail amplifiers, the LT1218/LT1219's input offset voltage is a low 90μV across the entire rail-to-rail input range, not just a portion of it. Using a patented technique, both input stages of the LT1218/LT1219 are trimmed: one at the negative supply and the other at the positive supply. The resulting common mode rejection of 97dB minimum is much better than other rail-to-rail input op amps. A minimum open-loop gain of 500V/mV into a 10k load virtually eliminates all gain error.

The LT1218 has conventional compensation which assures stability for capacitive loads of 1000pF or less. The LT1219 has compensation that requires the use of a 0.1μF output capacitor, which improves the amplifier's supply rejection and reduces output impedance at high frequencies. The output capacitor's filtering action also reduces high frequency noise, which is beneficial when driving A/D converters.

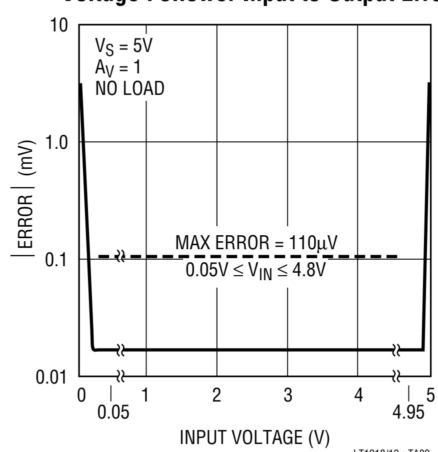
High and low voltage versions of the devices are offered. Operation is specified for 3V, 5V and ±5V supplies for the LT1218L/LT1219L and 3V, 5V and ±15V for the LT1218/LT1219.

TYPICAL APPLICATION

MUX Amplifier



Voltage Follower Input to Output Error

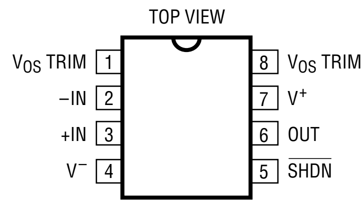


ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- LT1218/LT1219 .... ±18V
- LT1218L/LT1219L .... ±8V

Input Current .... ±15mA
Output Short-Circuit Duration (Note 1) .... Continuous
Operating Temperature Range .... –40°C to 85°C
Specified Temperature Range (Note 3) ... –40°C to 85°C
Storage Temperature Range .... –65°C to 150°C
Junction Temperature .... 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 190°C/W (S8)

ORDER PART NUMBER
LT1218CN8
LT1218CS8
LT1218LCN8
LT1218LCS8
LT1219CN8
LT1219CS8
LT1219LCN8
LT1219LCS8

S8 PART MARKING	
1218	1219
1218L	1219L

Consult factory for Industrial and Military grades.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_O = half supply, $V_{\overline{SHDN}}$ = V^+, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V^+ V_{CM} = $V^–$		25 25	90 90	µV µV
ΔV_{OS}	Input Offset Voltage Shift	V_{CM} = $V^–$ to V^+		15	70	µV
I_B	Input Bias Current	V_{CM} = V^+ V_{CM} = $V^–$	 –70	30 –18	70	nA nA
ΔI_B	Input Bias Current Shift	V_{CM} = $V^–$ to V^+		50	140	nA
I_{OS}	Input Offset Current	V_{CM} = V^+ V_{CM} = $V^–$		5 2	18 18	nA nA
ΔI_{OS}	Input Offset Current Shift	V_{CM} = $V^–$ to V^+		5	18	nA
e_n	Input Noise Voltage Density	f = 1kHz		33		nV/√Hz
i_n	Input Noise Current Density	f = 1kHz		0.09		pA/√Hz
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 50mV to 4.8V, R_L = 10k V_S = 3V, V_O = 50mV to 2.8V, R_L = 10k	250 200	1000 750		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = $V^–$ to V^+ V_S = 3V, V_{CM} = $V^–$ to V^+	97 92	110 106		dB dB
PSRR	Power Supply Rejection Ratio	V_S = 2.3V to 12V, V_{CM} = 0V, V_O = 0.5V	90	100		dB
V_{OL}	Output Voltage Swing LOW	No Load I_{SINK} = 0.5mA I_{SINK} = 2.5mA		4 45 120	12 90 240	mV mV mV
V_{OH}	Output Voltage Swing HIGH	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 2.5mA	V^+ – 0.012 V^+ – 0.130 V^+ – 0.400	V^+ – 0.003 V^+ – 0.065 V^+ – 0.210		V V V
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	5 4	10 7		mA mA
I_S	Supply Current	V_S = 5V V_S = 3V		370 370	420 410	µA µA
	Positive Supply Current, SHDN	V_S = 5V, $V_{\overline{SHDN}}$ = 0V V_S = 3V, $V_{\overline{SHDN}}$ = 0V		9 6	30 20	µA µA

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = 5V, 0V$; $V_S = 3V, 0V$; $V_{CM} = V_O$ = half supply, $V_{\overline{SHDN}} = V^+$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SR	Slew Rate (LT1218/LT1218L) (LT1219/LT1219L)	$A_V = -1$ $A_V = -1$		0.10 0.05		V/μs V/μs
GBW	Gain Bandwidth Product (LT1218/LT1218L) (LT1219/LT1219L)	 $A_V = 1000$ $A_V = 1000$		 0.30 0.15		 MHz MHz

$0°C \le T_A \le 70°C$, $V_S = 5V, 0V$; $V_S = 3V, 0V$; $V_{CM} = V_O$ = half supply, $V_{\overline{SHDN}} = V^+$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^-$	● ●		75 75	200 200	μV μV
V_{OS} TC	Input Offset Drift	(Note 2)	●		1	3	μV/°C
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+	●		25	80	μV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^-$	● ●	 –75	30 –18	75	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^-$ to V^+	●		50	150	nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^-$	● ●		5 3	25 25	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+	●		5	25	nA
A_{VOL}	Large-Signal Voltage Gain	$V_S = 5V$, $V_O = 50mV$ to $4.8V$, $R_L = 10k$ $V_S = 3V$, $V_O = 50mV$ to $2.8V$, $R_L = 10k$	● ●	250 150	1000 750		V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_S = 5V$, $V_{CM} = V^-$ to V^+ $V_S = 3V$, $V_{CM} = V^-$ to V^+	● ●	96 91	104 106		dB dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.3V$ to $12V$, $V_{CM} = 0V$, $V_O = 0.5V$	●	88	100		dB
V_{OL}	Output Voltage Swing LOW	No Load $I_{SINK} = 0.5mA$ $I_{SINK} = 2.5mA$	● ● ●		4 45 130	14 100 290	mV mV mV
V_{OH}	Output Voltage Swing HIGH	No Load $I_{SOURCE} = 0.5mA$ $I_{SOURCE} = 2.5mA$	● ● ●	$V^+ - 0.014$ $V^+ - 0.150$ $V^+ - 0.480$	$V^+ - 0.004$ $V^+ - 0.075$ $V^+ - 0.240$		V V V
I_{SC}	Short-Circuit Current	$V_S = 5V$ $V_S = 3V$	● ●	4 3	7 6		mA mA
I_S	Supply Current	$V_S = 5V$ $V_S = 3V$	● ●		370 370	485 475	μA μA
	Positive Supply Current, SHDN	$V_S = 5V$, $V_{\overline{SHDN}} = 0V$ $V_S = 3V$, $V_{\overline{SHDN}} = 0V$	● ●		9 6	36 26	μA μA

$-40°C \le T_A \le 85°C$, $V_S = 5V, 0V$; $V_S = 3V, 0V$; $V_{CM} = V_O$ = half supply, $V_{\overline{SHDN}} = V^+$, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+ - 0.15$ $V_{CM} = V^- + 0.15$	● ●			400 400	μV μV
V_{OS} TC	Input Offset Drift	(Note 2)	●		1	4	μV/°C
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^+ - 0.15$ to $V^- + 0.15$	●		30	105	μV
I_B	Input Bias Current	$V_{CM} = V^+ - 0.15$ $V_{CM} = V^- + 0.15$	● ●	 –80		80	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^+ - 0.15$ to $V^- + 0.15$	●			160	nA
I_{OS}	Input Offset Current	$V_{CM} = V^+ - 0.15$ $V_{CM} = V^- + 0.15$	● ●			40 40	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^+ - 0.15$ to $V^- + 0.15$	●			40	nA

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$, V_S = 5V, 0V; V_S = 3V, 0V; $V_{CM} = V_O$ = half supply, $V_{\overline{SHDN}} = V^+$, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 50mV to 4.8V, R_L = 10k V_S = 3V, V_O = 50mV to 2.8V, R_L = 10k	● ●	150 100	500 500		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, $V_{CM} = V^+ - 0.15$ to $V^- + 0.15$ V_S = 3V, $V_{CM} = V^+ - 0.15$ to $V^- + 0.15$	● ●	93 88	102 100		dB dB
PSRR	Power Supply Rejection Ratio	V_S = 2.3V to 12V, V_{CM} = 0V, V_O = 0.5V	●	86	100		dB
V_{OL}	Output Voltage Swing LOW	No Load I_{SINK} = 0.5mA I_{SINK} = 2.5mA	● ● ●		5 50 130	15 105 300	mV mV mV
V_{OH}	Output Voltage Swing HIGH	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 2.5mA	● ● ●	$V^+ - 0.015$ $V^+ - 0.160$ $V^+ - 0.500$	$V^+ - 0.004$ $V^+ - 0.070$ $V^+ - 0.250$		mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	● ●	4 3	7 7		mA mA
I_S	Supply Current	V_S = 5V V_S = 3V	● ●		410 400	505 495	µA µA
	Positive Supply Current, SHDN	V_S = 5V, $V_{\overline{SHDN}}$ = 0V V_S = 3V, $V_{\overline{SHDN}}$ = 0V	● ●		15 13	50 40	µA µA

LT1218L/LT1219L only; T_A = 25°C, V_S = ±5V, V_{CM} = 0V, V_O = 0V, $V_{\overline{SHDN}}$ = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^-$		35 35	140 140	µV µV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+		20	70	µV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^-$	 –70	30 –18	70	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^-$ to V^+		50	140	nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^-$		5 2	18 18	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+		5	18	nA
A_{VOL}	Large-Signal Voltage Gain	V_O = –4.7V to 4.7V, R_L = 10k V_O = –4.5V to 4.5V, R_L = 2k	500 300	2800 1300		V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to V^+	103	114		dB
V_{OL}	Output Voltage Swing LOW	No Load I_{SINK} = 0.5mA I_{SINK} = 5mA		$V^- + 0.004$ $V^- + 0.045$ $V^- + 0.180$	$V^- + 0.012$ $V^- + 0.090$ $V^- + 0.525$	V V V
V_{OH}	Output Voltage Swing HIGH	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 5mA	$V^+ - 0.012$ $V^+ - 0.130$ $V^+ - 0.800$	$V^+ - 0.003$ $V^+ - 0.065$ $V^+ - 0.350$		V V V
I_{SC}	Short-Circuit Current		6	12		mA
I_S	Supply Current			400	430	µA
	Positive Supply Current, SHDN	$V_{\overline{SHDN}}$ = 0V		10	40	µA
SR	Slew Rate (LT1218/LT1218L) (LT1219/LT1219L)	A_V = –1, R_L = Open, V_O = ±3.5V A_V = –1, R_L = Open, V_O = ±3.5V	0.06 0.03	0.10 0.05		V/µs V/µs
GBW	Gain-Bandwidth Product (LT1218/LT1218L) (LT1219/LT1219L)	 A_V = 1000 A_V = 1000	 0.2 0.1	 0.30 0.15		 MHz MHz

ELECTRICAL CHARACTERISTICS

LT1218L/LT1219L only; 0°C ≤ T_A ≤ 70°C, V_S = ±5V, V_{CM} = 0V, V_O = 0V, $V_{\overline{SHDN}}$ = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^-$	● ●		100 100	250 250	µV µV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+	●		30	90	µV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^-$	● ●	 –75	30 –18	75	nA nA
ΔI_B	Input Bias Current	$V_{CM} = V^-$ to V^+	●		50	150	nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^-$	● ●		5 3	25 25	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+	●		5	20	nA
A_{VOL}	Large-Signal Voltage Gain	V_O = –4.7V to 4.7V, R_L = 10k V_O = –4.5V to 4.5V, R_L = 2k	● ●	375 275	2800 1300		V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to V^+	●	100	110		dB
V_{OL}	Output Voltage Swing LOW	No Load I_{SINK} = 0.5mA I_{SINK} = 5mA	● ● ●		V^- + 0.004 V^- + 0.045 V^- + 0.200	V^- + 0.014 V^- + 0.100 V^- + 0.580	V V V
V_{OH}	Output Voltage Swing HIGH	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 5mA	● ● ●	V^+ – 0.014 V^+ – 0.150 V^+ – 0.920	V^+ – 0.004 V^+ – 0.075 V^+ – 0.450		V V V
I_{SC}	Short-Circuit Current		●	5	10		mA
I_S	Supply Current		●		400	495	µA
	Positive Supply Current, SHDN	$V_{\overline{SHDN}}$ = 0V	●		11	54	µA

LT1218L, LT1219L only; –40°C ≤ T_A ≤ 85°C, V_S = ±5V; V_{CM} = 0V, V_O = 0V, $V_{\overline{SHDN}}$ = 5V, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+ - 0.15$ $V_{CM} = V^- + 0.15$	● ●		125 125	500 500	µV µV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^+ - 0.15$ to $V^- + 0.15$	●		35	120	µV
I_B	Input Bias Current	$V_{CM} = V^+ - 0.15$ $V_{CM} = V^- + 0.15$	● ●	 –80		80	nA nA
ΔI_B	Input Bias Current	$V_{CM} = V^+ - 0.15$ to $V^- + 0.15$	●			160	nA
I_{OS}	Input Offset Current Shift	$V_{CM} = V^+ - 0.15$ $V_{CM} = V^- + 0.15$	● ●			40 40	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} =$ $V^+ - 0.15$ to $V^- + 0.15$	●			40	nA
A_{VOL}	Large-Signal Voltage Gain	V_O = –4.7V to 4.7V, R_L = 10k V_O = –4.5V to 4.5V, R_L = 2k	● ●	300 200	2000 600		V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^+ - 0.15$ to $V^- + 0.15$	●	98	109		dB
V_{OL}	Output Voltage Swing LOW	No Load I_{SINK} = 0.5mA I_{SINK} = 2.5mA	● ● ●		V^- + 0.005 V^- + 0.050 V^- + 0.200	V^- + 0.015 V^- + 0.105 V^- + 0.620	V V V
V_{OH}	Output Voltage Swing HIGH	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 2.5mA	● ● ●	V^+ – 0.015 V^+ – 0.160 V^+ – 1.000	V^+ – 0.004 V^+ – 0.070 V^+ – 0.400		V V V
I_{SC}	Short-Circuit Current		●	5	10		mA
I_S	Supply Current		●		420	525	µA
	Positive Supply Current, SHDN	$V_{\overline{SHDN}}$ = 0V	●		18	60	µA

ELECTRICAL CHARACTERISTICS

LT1218/LT1219 only; $T_A = 25°C$, $V_S = ±15V$, $V_{CM} = 0V$, $V_O = 0V$, $V_{\overline{SHDN}} = 15V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^-$		85 85	200 200	µV µV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+		30	70	µV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^-$	 –70	30 –18	70	nA nA
ΔI_B	Input Bias Current	$V_{CM} = V^-$ to V^+		50	140	nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^-$		5 2	18 18	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+		5	18	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = –14.7V$ to $14.7V$, $R_L = 10k$ $V_O = –10V$ to $10V$, $R_L = 2k$	1000 500	4000 2000		V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to V^+	113	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = ±5V$ to $±15V$	100	110		dB
V_{OL}	Output Voltage Swing LOW	No Load $I_{SINK} = 0.5mA$ $I_{SINK} = 5mA$		$V^- + 0.004$ $V^- + 0.045$ $V^- + 0.270$	$V^- + 0.012$ $V^- + 0.090$ $V^- + 0.525$	V V V
V_{OH}	Output Voltage Swing HIGH	No Load $I_{SOURCE} = 0.5mA$ $I_{SOURCE} = 5mA$	$V^+ – 0.012$ $V^+ – 0.130$ $V^+ – 0.800$	$V^+ – 0.003$ $V^+ – 0.065$ $V^+ – 0.580$		V V V
I_{SC}	Short-Circuit Current		10	20		mA
I_S	Supply Current			425	550	µA
	Positive Supply Current, SHDN	$V_{\overline{SHDN}} = 0V$		15	40	µA
SR	Slew Rate (LT1218/LT1218L) (LT1219/LT1219L)	$A_V = –1$ $A_V = –1$		0.10 0.05		V/µs V/µs
GBW	Gain Bandwidth Product (LT1218/LT1218L) (LT1219/LT1219L)	 $A_V = 1000$ $A_V = 1000$		 0.28 0.15		 MHz MHz

LT1218/LT1219 only; $0°C \le T_A \le 70°C$, $V_S = ±15V$, $V_{CM} = 0V$, $V_O = 0V$, $V_{\overline{SHDN}} = 15V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^-$	● ●		120 120	300 300	µV µV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+	●		50	105	µV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^-$	● ●	 –75	30 –18	75	nA nA
ΔI_B	Input Bias Current	$V_{CM} = V^-$ to V^+	●		50	150	nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^-$	● ●		5 3	25 25	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+	●		5	20	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = –14.7V$ to $14.7V$, $R_L = 10k$ $V_O = –10V$ to $10V$, $R_L = 2k$	● ●	750 500	3000 1500		V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to V^+	●	109	114		dB
PSRR	Power Supply Rejection Ratio	$V_S = ±5V$ to $±15V$	●	97	110		dB
V_{OL}	Output Voltage Swing LOW	No Load $I_{SINK} = 0.5mA$ $I_{SINK} = 5mA$	● ● ●		$V^- + 0.004$ $V^- + 0.045$ $V^- + 0.310$	$V^- + 0.014$ $V^- + 0.100$ $V^- + 0.580$	V V V
V_{OH}	Output Voltage Swing HIGH	No Load $I_{SOURCE} = 0.5mA$ $I_{SOURCE} = 5mA$	● ● ●	$V^+ – 0.014$ $V^+ – 0.150$ $V^+ – 0.920$	$V^+ – 0.003$ $V^+ – 0.075$ $V^+ – 0.700$		V V V

LINEAR TECHNOLOGY

ELECTRICAL CHARACTERISTICS

LT1218/LT1219 only; 0°C ≤ T_A ≤ 70°C, V_S = ±15V, V_{CM} = 0V, V_O = 0V, $V_{\overline{SHDN}}$ = 15V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SC}	Short-Circuit Current		●	8	17		mA
I_S	Supply Current		●		450	600	µA
	Positive Supply Current, SHDN	$V_{\overline{SHDN}}$ = 0V	●		20	54	µA

LT1218, LT1219 only; –40°C ≤ T_A ≤ 85°C, V_S = ±15V; V_{CM} = 0V = V_O = 0V, $V_{\overline{SHDN}}$ = 15V, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+ - 0.15$ $V_{CM} = V^- + 0.15$	● ●		150 150	600 600	µV µV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^+ - 0.15$ to $V^- + 0.15$	●		50	165	µV
I_B	Input Bias Current	$V_{CM} = V^+ - 0.15$ $V_{CM} = V^- + 0.15$	● ●	 –80		80 	nA nA
ΔI_B	Input Bias Current	$V_{CM} = V^+ - 0.15$ to $V^- + 0.15$	●			160	nA
I_{OS}	Input Offset Current	$V_{CM} = V^+ - 0.15$ $V_{CM} = V^- + 0.15$	● ●			40 40	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^+ - 0.15$ to $V^- + 0.15$	●			40	nA
A_{VOL}	Large-Signal Voltage Gain	V_O = –14.7V to 14.7V, R_L = 10k V_O = –10V to 10V, R_L = 2k	● ●	500 400	3000 1000		V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^+ - 0.15$ to $V^- + 0.15$	●	105	114		dB
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	●	96	110		dB
V_{OL}	Output Voltage Swing LOW	No Load I_{SINK} = 0.5mA I_{SINK} = 2.5mA	● ● ●		$V^- + 0.005$ $V^- + 0.050$ $V^- + 0.200$	$V^- + 0.015$ $V^- + 0.105$ $V^- + 0.620$	V V V
V_{OH}	Output Voltage Swing HIGH	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 2.5mA	● ● ●	$V^+ - 0.015$ $V^+ - 0.160$ $V^+ - 1.000$	$V^+ - 0.004$ $V^+ - 0.070$ $V^+ - 0.400$		V V V
I_{SC}	Short-Circuit Current		●	5	14		mA
I_S	Supply Current		●			650	µA
	Positive Supply Current, SHDN	$V_{\overline{SHDN}}$ = 0V	●			60	µA

The ● denotes specifications which apply over the full operating temperature range.

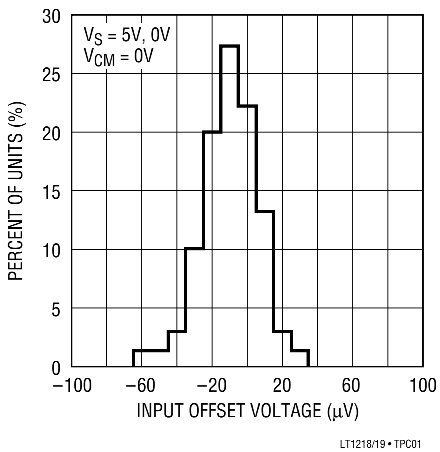
Note 1: A heat sink may be required to keep the junction temperature below the Absolute Maximum Rating when the output is shorted indefinitely.

Note 2: This parameter is not 100% tested.

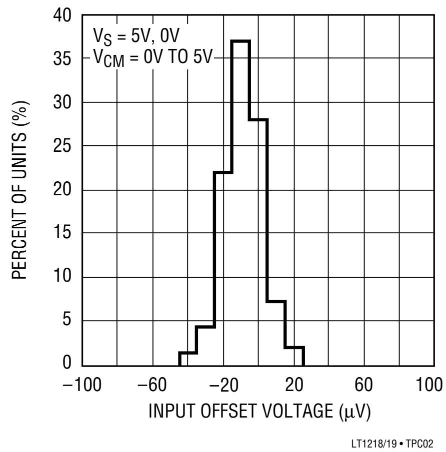
Note 3: The LT1218/LT1219 are designed, characterized and expected to meet these extended temperature limits, but are not tested at –40°C and 85°C. Guaranteed I grade part are available: consult factory.

TYPICAL PERFORMANCE CHARACTERISTICS

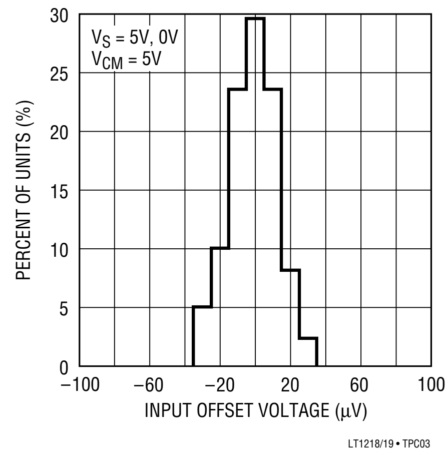
V_{OS} Distribution, V_{CM} = 0V



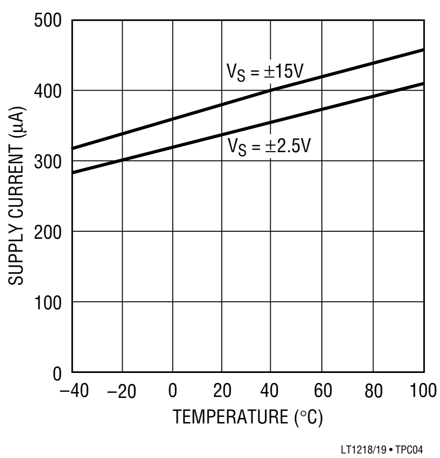
V_{OS} Shift, V_{CM} = 0V to 5V



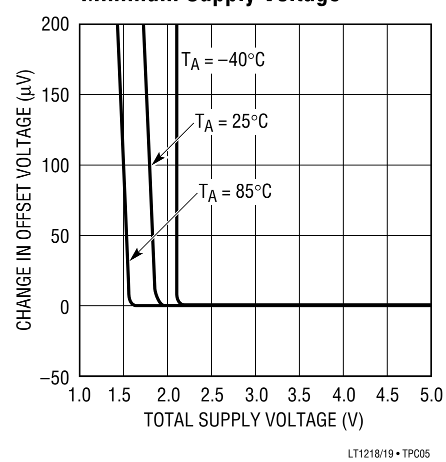
V_{OS} Distribution, V_{CM} = 5V



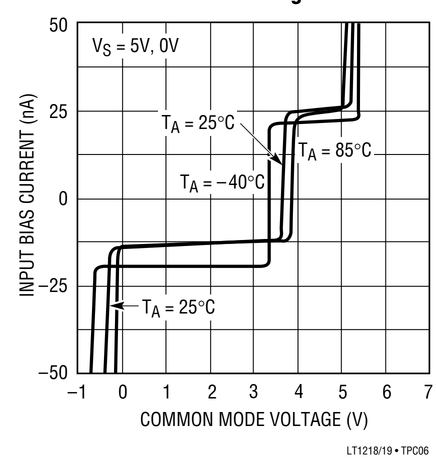
Supply Current vs Temperature



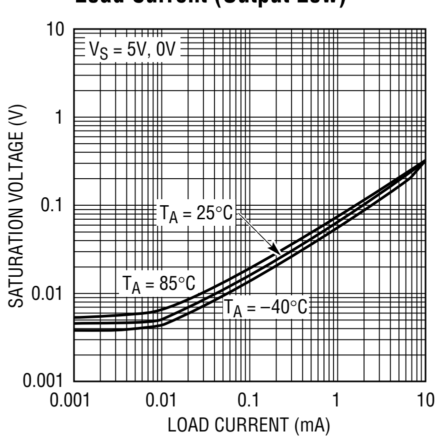
Minimum Supply Voltage



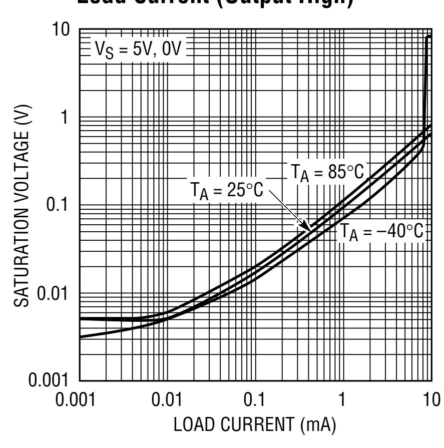
Input Bias Current vs Common Mode Voltage



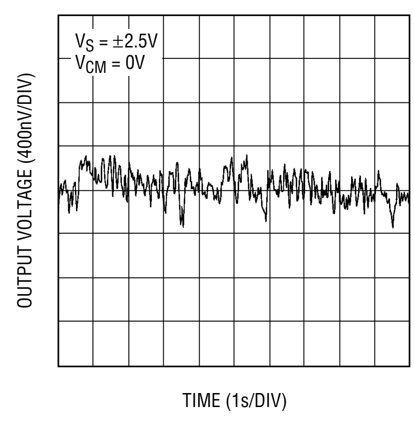
Output Saturation Voltage vs Load Current (Output Low)



Output Saturation Voltage vs Load Current (Output High)

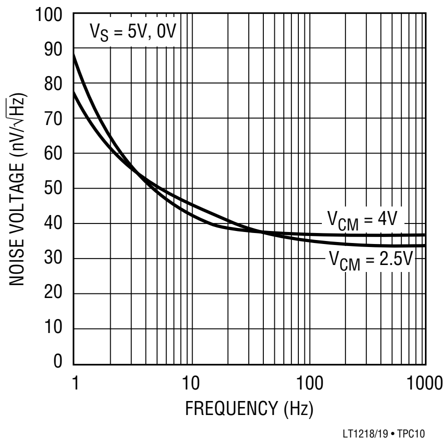


0.1Hz to 10Hz Output Voltage Noise

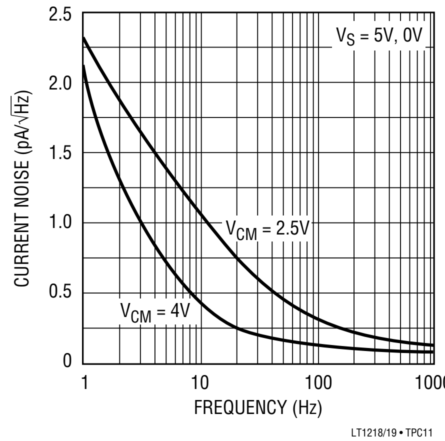


TYPICAL PERFORMANCE CHARACTERISTICS

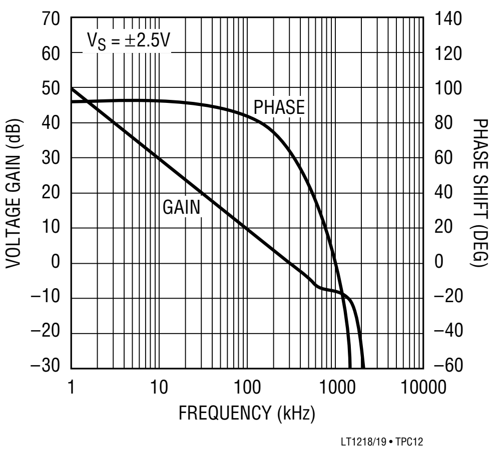
Noise Voltage Spectrum



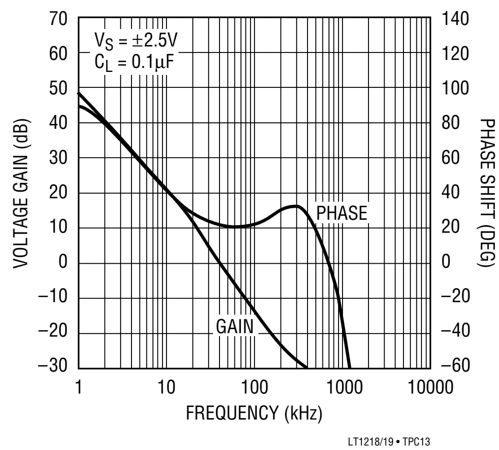
Noise Current Spectrum



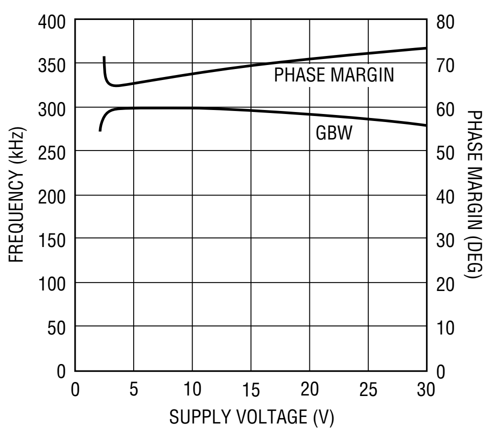
LT1218 Gain and Phase Shift vs Frequency



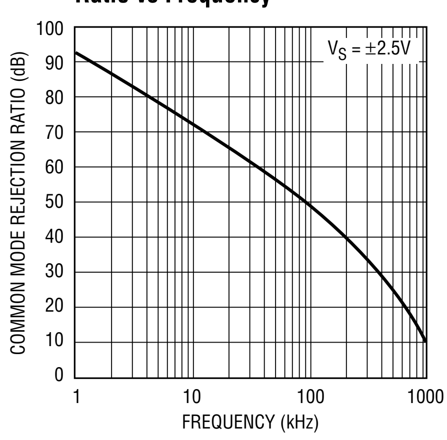
LT1219 Gain and Phase Shift vs Frequency



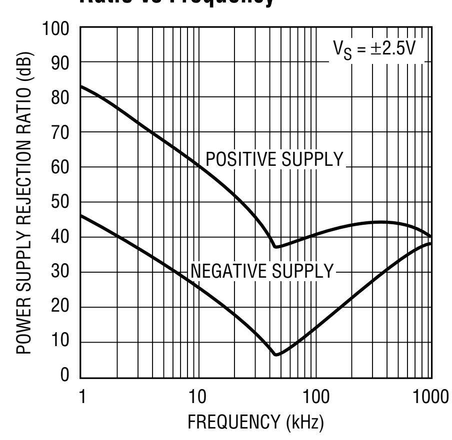
LT1218 Gain Bandwidth and Phase Margin vs Supply Voltage



LT1218 Common Mode Rejection Ratio vs Frequency

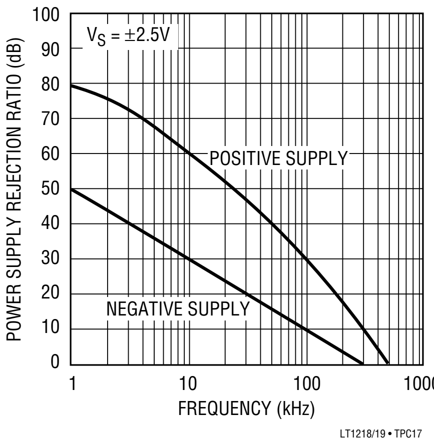


LT1219 Power Supply Rejection Ratio vs Frequency

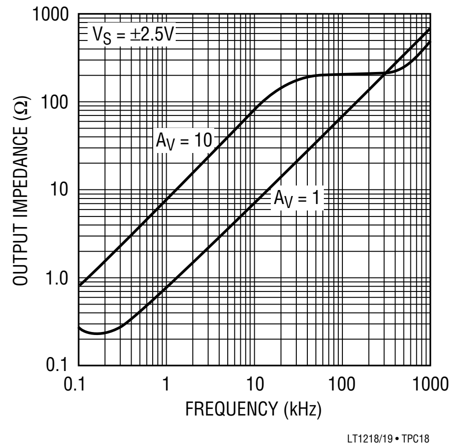


TYPICAL PERFORMANCE CHARACTERISTICS

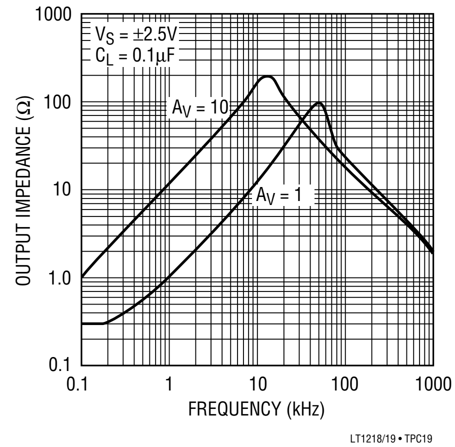
LT1218 Power Supply Rejection Ratio vs Frequency



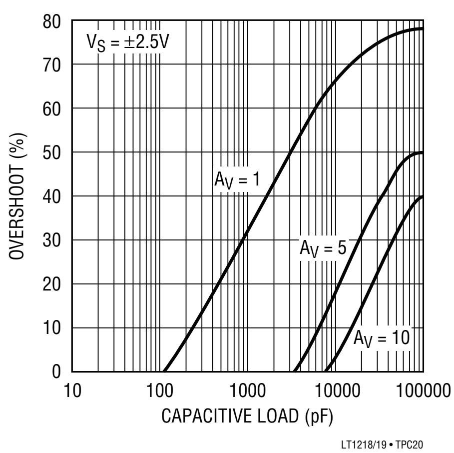
LT1218 Closed Loop Output Impedance vs Frequency



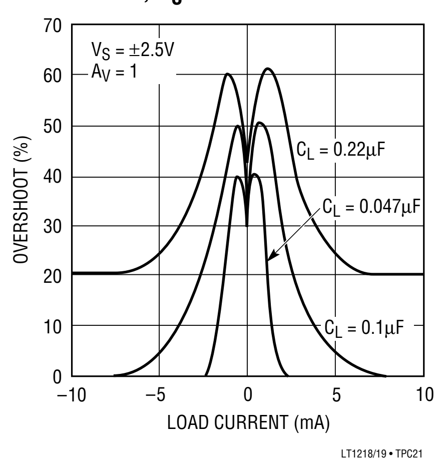
LT1219 Closed Loop Output Impedance vs Frequency



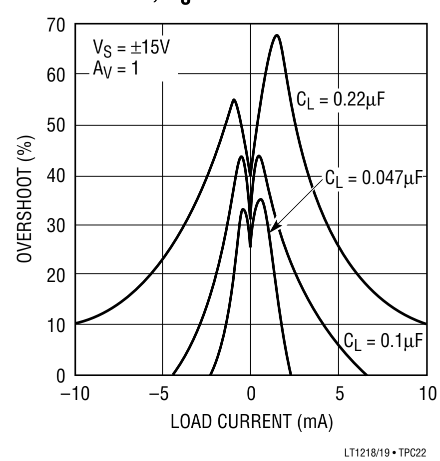
LT1218 Capacitive Load Handling



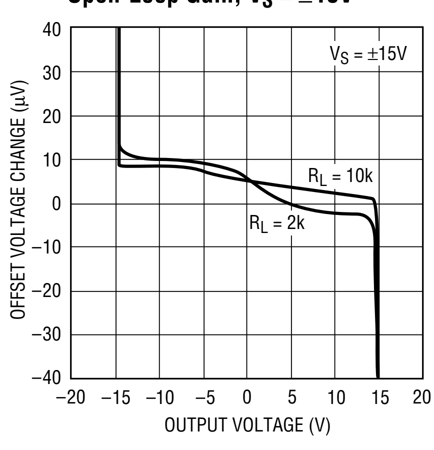
LT1219 Overshoot vs Load Current, $V_S = \pm2.5V$



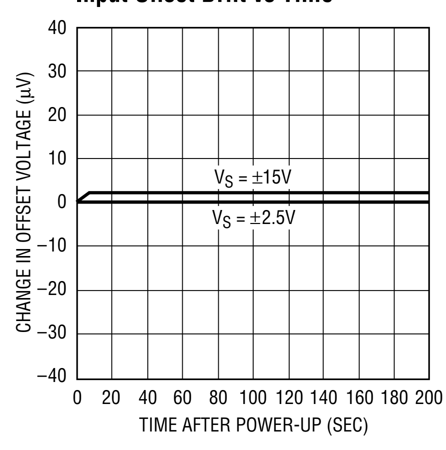
LT1219 Overshoot vs Load Current, $V_S = \pm15V$



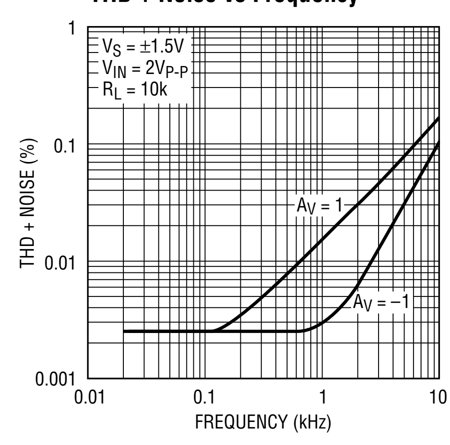
Open-Loop Gain, $V_S = \pm15V$



Input Offset Drift vs Time

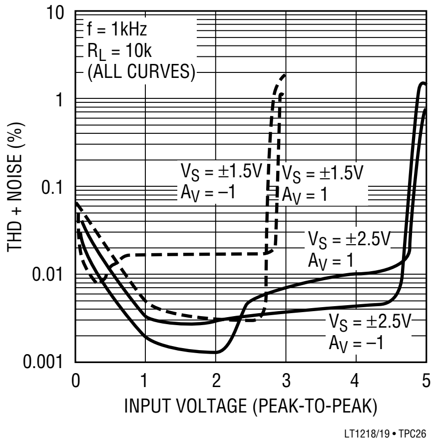


THD + Noise vs Frequency

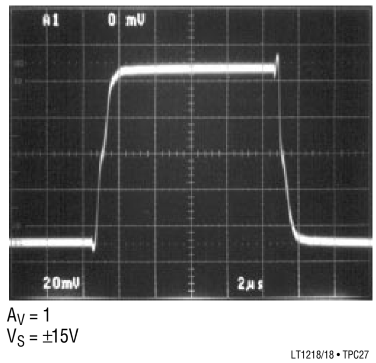


TYPICAL PERFORMANCE CHARACTERISTICS

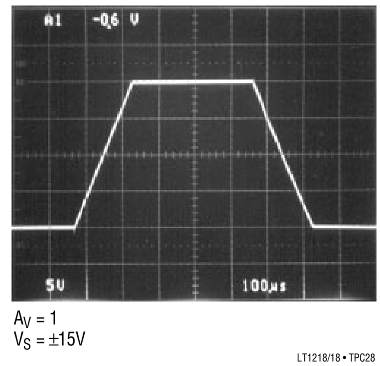
THD + Noise vs Peak-to-Peak Voltage



Small-Signal Response $V_S = \pm15V$



Large-Signal Response $V_S = \pm15V$



APPLICATIONS INFORMATION

Rail-to-Rail Operation

The LT1218/LT1219 differ from conventional op amps in the design of both the input and output stages. Figure 1 shows a simplified schematic of the amplifier. The input stage consists of two differential amplifiers, a PNP stage Q1/Q2 and an NPN stage Q3/Q4, which are active over different portions of the input common mode range. Lateral devices are used in both input stages, eliminating the need for clamps across the input pins. Each input stage is trimmed for offset voltage. A complementary output configuration (Q23 through Q26) is employed to create an

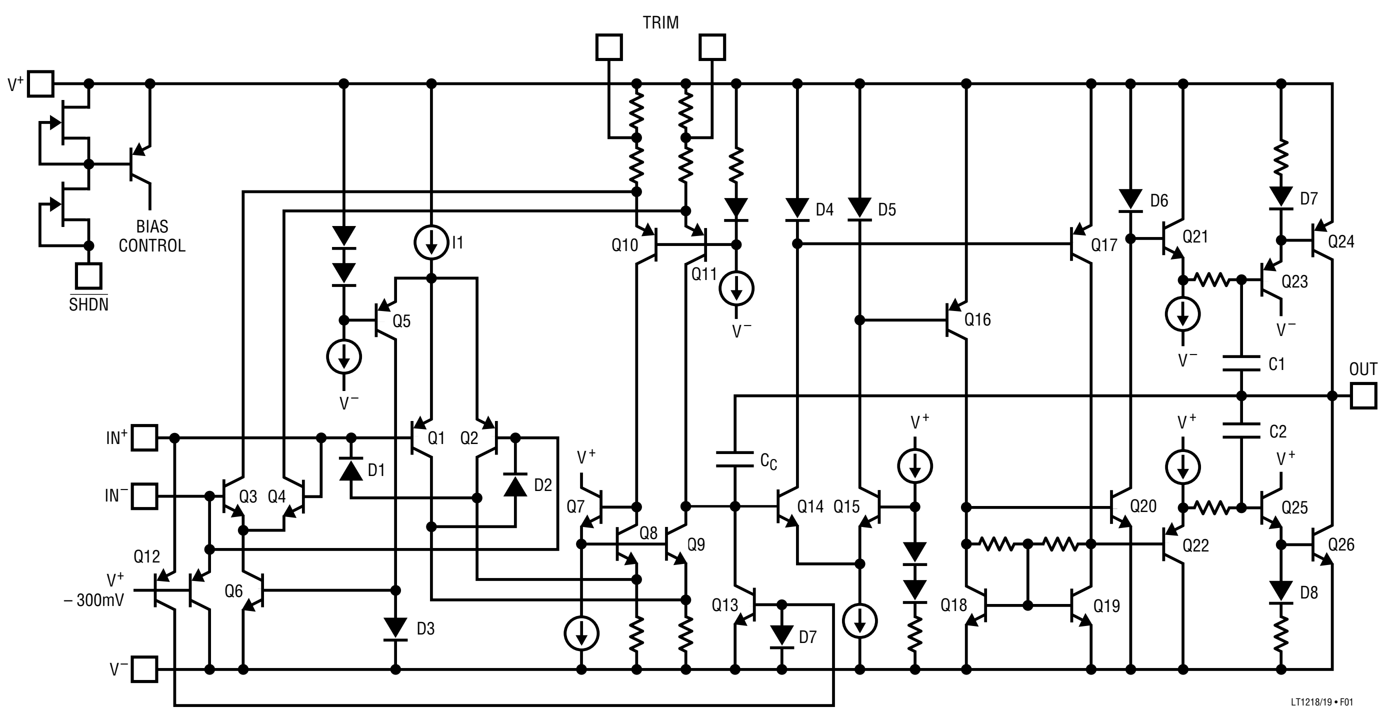


Figure 1. LT1218 Simplified Schematic Diagram

APPLICATIONS INFORMATION

output stage with rail-to-rail swing. The amplifier is fabricated on Linear Technology's proprietary complementary bipolar process, which ensures very similar DC and AC characteristics for the output devices Q24 and Q26.

A simple comparator Q5 steers current from current source I_1 between the two input stages. When the input common mode voltage V_{CM} is near the negative supply, Q5 is reverse biased, and I_1 becomes the tail current for the PNP differential pair Q1/Q2. At the other extreme, when V_{CM} is within about 1.3V from the positive supply, Q5 diverts I_1 to the current mirror D3/Q6, which furnishes the tail current for the NPN differential pair Q3/Q4.

The collector currents of the two input pairs are combined in the second stage, consisting of Q7 through Q11. Most of the voltage gain in the amplifier is contained in this stage. Differential amplifier Q14/Q15 buffers the output of the second stage, converting the output voltage to differential currents. The differential currents pass through current mirrors D4/Q17 and D5/Q16, and are converted to differential voltages by Q18 and Q19. These voltages are also buffered and applied to the output Darlington pairs Q23/Q24 and Q25/Q26. Capacitors C1 and C2 form local feedback loops around the output devices, lowering the output impedance at high frequencies.

Input Offset Voltage

Since the amplifier has two input stages, the input offset voltage changes depending upon which stage is active. The input offsets are random, but bounded voltages. When the amplifier switches between stages, offset voltages may go up, down or remain flat; but will not exceed the guaranteed limits. This behavior is illustrated in three distribution plots of input offset voltage in the Typical Performance Characteristics section.

Overdrive Protection

Two circuits prevent the output from reversing polarity when the input voltage exceeds the common mode range. When the noninverting input exceeds the positive supply by approximately 300mV, the clamp transistor Q12 (Figure 1) turns on, pulling the output of the second stage low, which forces the output high. For input below the negative supply, diodes D1 and D2 turn on, overcoming the saturation of the input pair Q1/Q2.

When overdriven, the amplifier draws input current that exceeds the normal input bias current. Figures 2 and 3 show typical input current as a function of input voltage. The input current must be less than 10mA for the phase reversal protection to work properly. When the amplifier is severely overdriven, an external resistor should be used to limit the overdrive current.

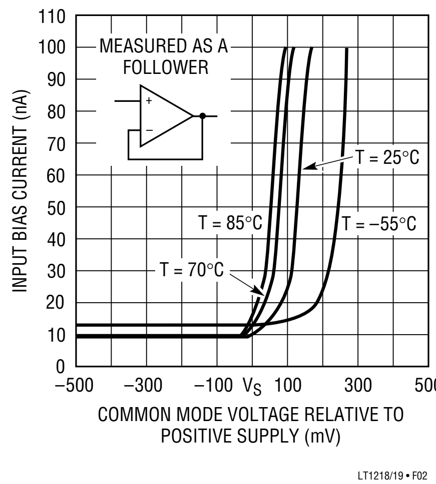


Figure 2. Input Bias Current vs Common Mode Voltage

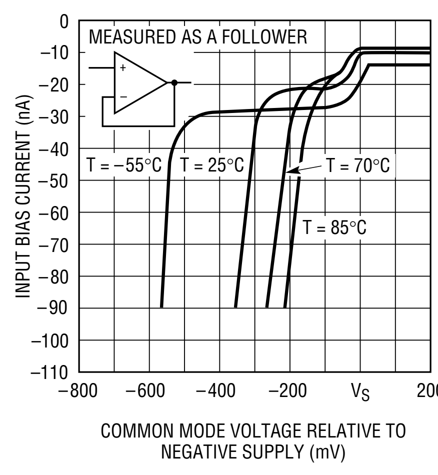


Figure 3. Input Bias Current vs Common Mode Voltage

APPLICATIONS INFORMATION

Shutdown

The biasing of the LT1218/LT1219 is controlled by the $\overline{\text{SHDN}}$ pin. When the $\overline{\text{SHDN}}$ pin is low, the part is shut down. In the shutdown mode, the output looks like a 40pF capacitor and the supply current is less than 30µA. The $\overline{\text{SHDN}}$ pin is referenced to the positive supply through an internal bias circuit (see Figure 1). The $\overline{\text{SHDN}}$ pin current with the pin low is typically 3µA.

The switching time between the shutdown and active states is about 20µs, however, the total time to settle will be greater by the slew time of the amplifier. For example, if the DC voltage at the amplifier output is 0V in shutdown and –2V in the active mode, an additional 20µs is required. Figures 4a and 4b show the switching waveforms for a sinusoidal and a –2V DC input to the LT1218.

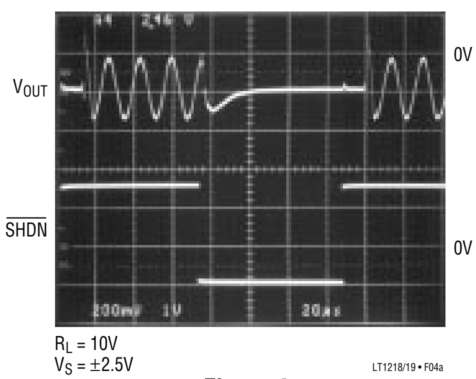


Figure 4a

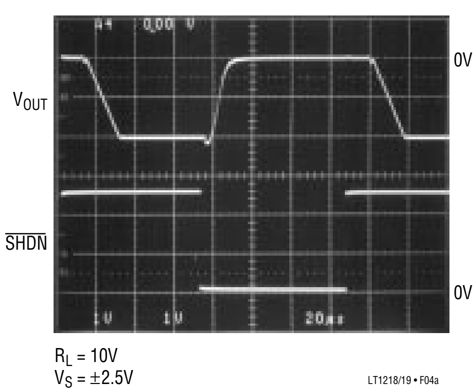


Figure 4b

The $\overline{\text{SHDN}}$ pin can be driven directly from CMOS logic if the logic and the LT1218/LT1219 are operated from the same supplies. For higher supply operation, an interface is required. An easy way to interface between supplies is to use open-drain logic, an example is shown in Figure 5. Because the $\overline{\text{SHDN}}$ pin is referenced to the positive supply, the logic used should have a breakdown voltage greater than the positive supply.

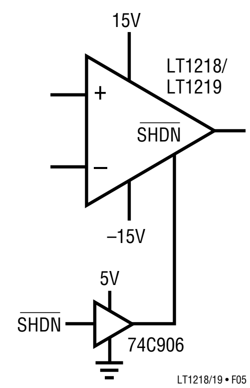


Figure 5. Shutdown Interface

Trim Pins

Trim pins are provided for compatibility with other single op amps. Input offset voltage can be adjusted over a ±2.3mV range with a 10k potentiometer.

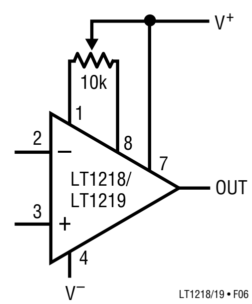


Figure 6. Optional Offset Nulling

Improved Supply Rejection in the LT1219

The LT1219 is a variation of the LT1218 offering greater supply rejection and lower high frequency output impedance. The LT1219 requires a 0.1µF load capacitance for

APPLICATIONS INFORMATION

compensation. The output capacitance forms a filter, which reduces pickup from the supply and lowers the output impedance. This additional filtering is helpful in mixed analog/digital systems with common supplies or systems employing switching supplies. Filtering also reduces high frequency noise, which may be beneficial when driving A/D converters.

Figures 7a and 7b show the outputs of the LT1218/LT1219 perturbed by a 200mV$_{P-P}$ 50kHz square wave added to the positive supply. The LT1219 power supply rejection is about ten times greater than that of the LT1218 at 50kHz. Note the 5-to-1 scale change in the output voltage traces.

The tolerance of the external compensation capacitor is not critical. The plots of Overshoot vs Load Current in the Typical Performance Characteristics section illustrate the effect of a capacitive load.

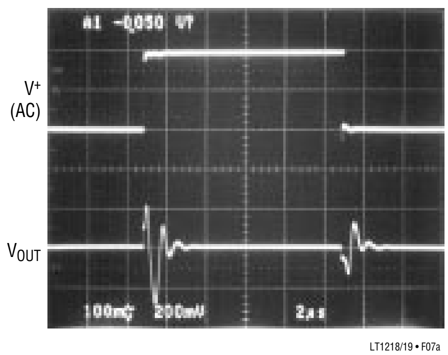


Figure 7a. LT1218 Power Supply Rejection Test

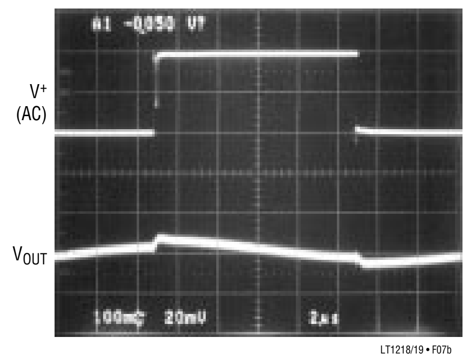
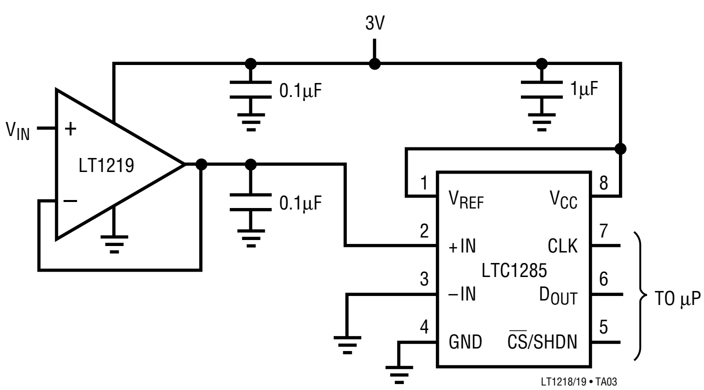


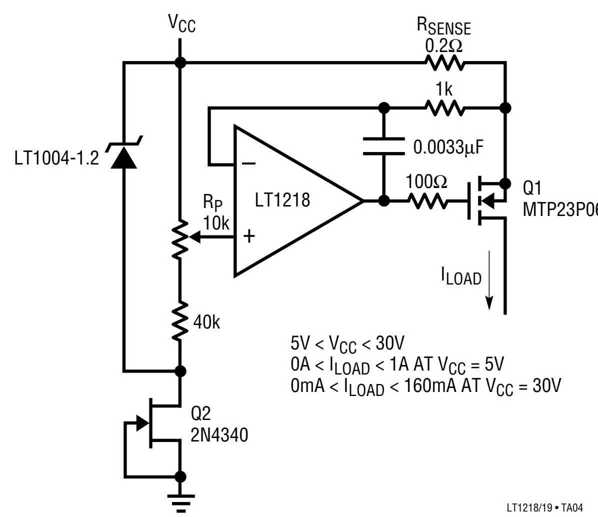
Figure 7b. LT1219 Power Supply Rejection Test

TYPICAL APPLICATIONS

Buffer for 12-Bit A/D Converter

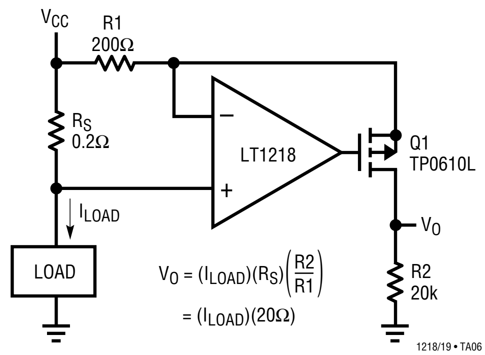


High-Side Current Source



TYPICAL APPLICATIONS

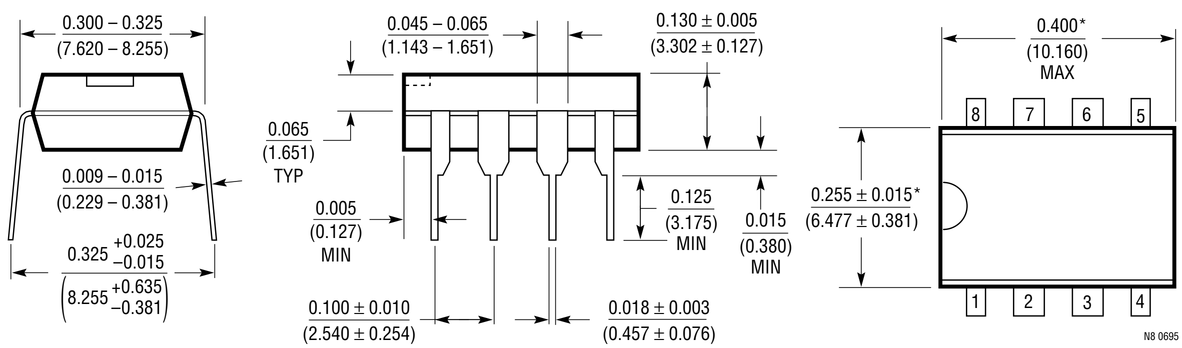
Positive Supply Current Sense



PACKAGE DESCRIPTION

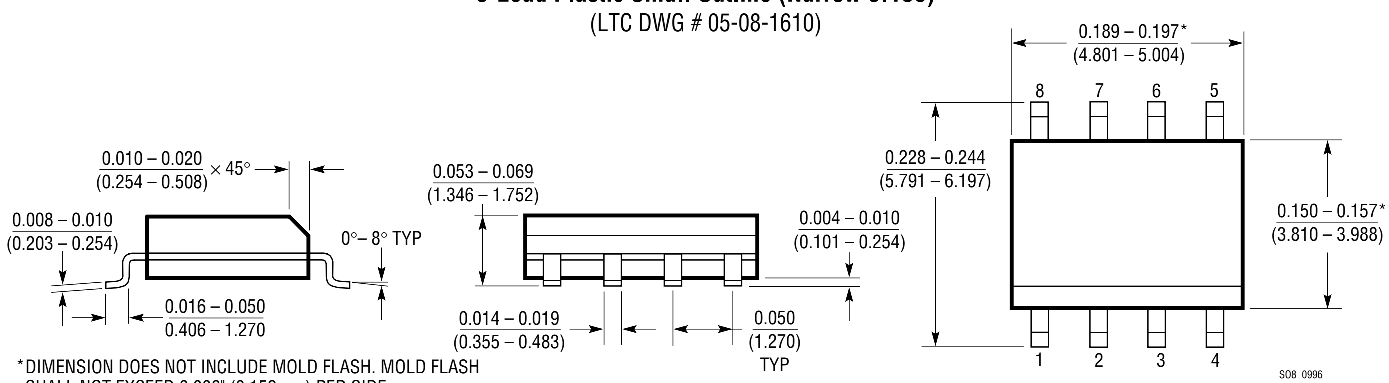
Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

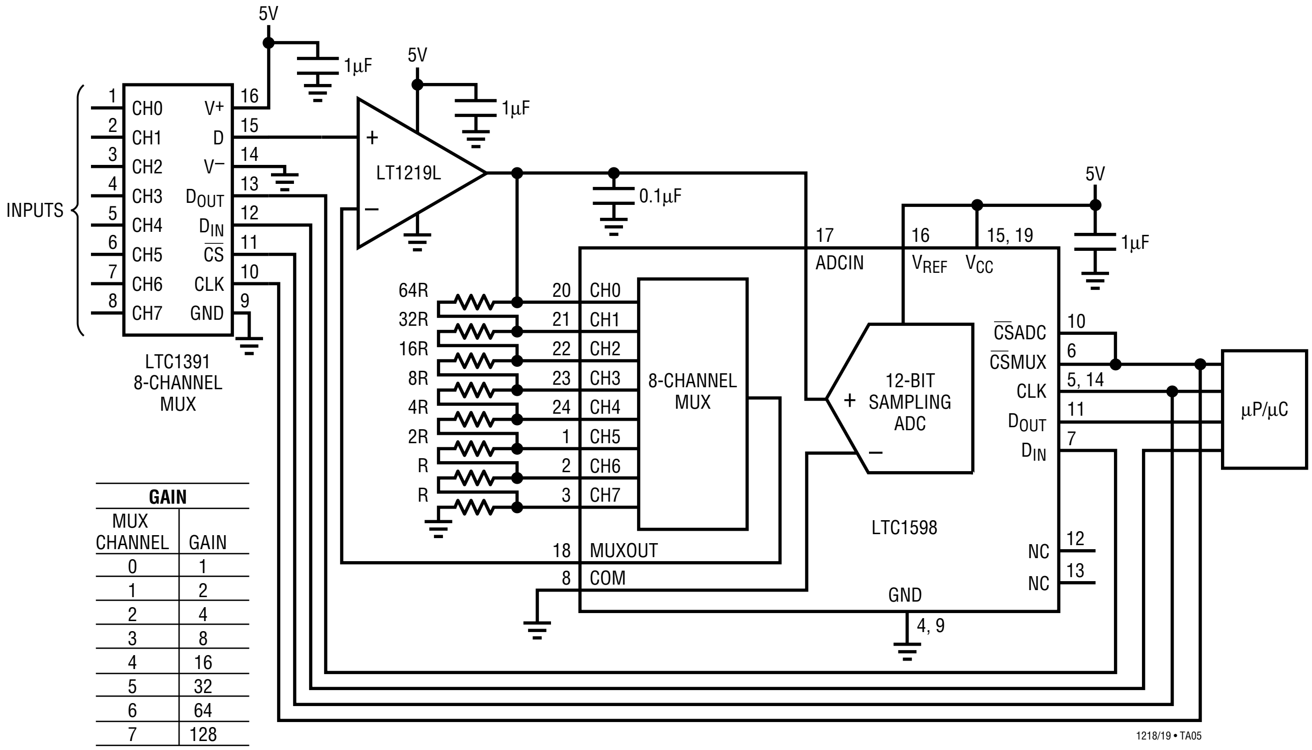


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

8-Channel, 12-Bit Data Acquisition System with Programmable Gain



GAIN	
MUX CHANNEL	GAIN
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC®1152	Rail-to-Rail Input and Output, Zero-Drift Op Amp	High DC Accuracy, 10μV $V_{OS(MAX)}$, 100nV/°C Drift, 0.7MHz GBW, 0.5V/μs Slew Rate, Maximum Supply Current 3mA
LT1366/LT1367	Dual/Quad Precision, Rail-to-Rail Input and Output Op Amps	475μV $V_{OS(MAX)}$, 400kHz GBW, 0.13V/μs Slew Rate, Maximum Supply Current 520μA per Op Amp
LT1466/LT1467	Dual/Quad Micropower, Rail-to-Rail Input and Output Op Amps	Maximum Supply Current 75μA per Op Amp, 390μV $V_{OS(MAX)}$, 120kHz Gain Bandwidth

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