Picoampere Input Current Quad Bipolar Op Amp

AD704

FEATURES

High dc precision
- **150 µV maximum offset voltage**
- **1.5 µV/°C maximum offset voltage drift**
- **270 pA maximum input bias current**
- **0.3 pA/°C typical I_B drift**

Low noise: 0.5 µV p-p
Typical noise: 0.1 Hz to 10 Hz
Low power: 600 µA maximum supply current per amplifier
Dual version: AD706

APPLICATIONS

Industrial/process controls
Weigh scales
ECG/EKG instrumentation
Low frequency active filters

GENERAL DESCRIPTION

The AD704 is a quad, low power bipolar op amp that has the low input bias current of a BiFET amplifier and offers a significantly lower I_B drift over temperature. It uses superbeta bipolar input transistors to achieve picoampere input bias current levels (similar to FET input amplifiers at room temperature), while its I_B typically increases only by 5× at 125°C (unlike a BiFET amp, for which I_B doubles every 10°C, resulting in a 1000× increase at 125°C). In addition, the AD704 achieves 150 µV offset voltage and the low noise characteristics of a precision bipolar input op amp.

Because it has only 1/20 the input bias current of an OP07, the AD704 does not require the commonly used balancing resistor. Furthermore, the current noise is 1/5 that of the OP07, which makes the AD704 usable with much higher source impedances. At 1/6 the supply current (per amplifier) of the OP07, the AD704 is better suited for today's higher density circuit boards and battery-powered applications.

The AD704 is an excellent choice for use in low frequency active filters in 12- and 14-bit data acquisition systems, in precision instrumentation, and as a high quality integrator. The AD704 is internally compensated for unity gain stability. The AD704J is rated over the commercial temperature range of 0°C to 70°C. The AD704A is rated over the industrial temperature of −40°C to +85°C. The AD704S is rated over the military temperature range of −55°C to +125°C, processed to MIL-STD-883B.

CONNECTION DIAGRAMS

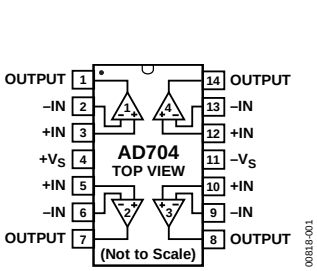

Figure 1. 14-Lead Plastic DIP (N)

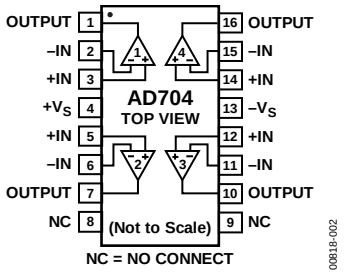

Figure 2. 16-Lead SOIC (R) Package

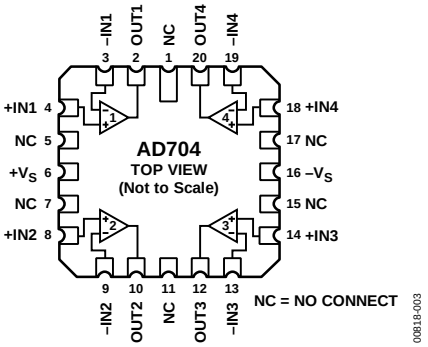

Figure 3. 20-Terminal LCC (E-20-1) Package

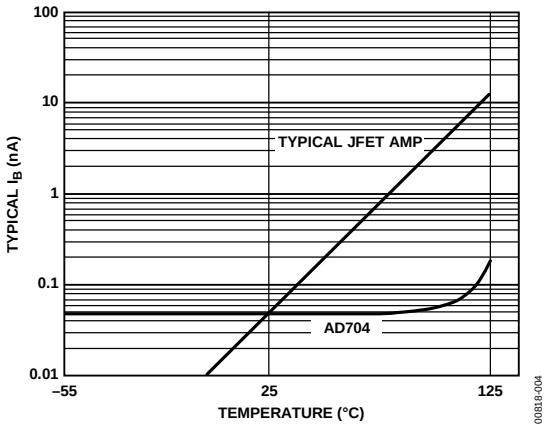

Figure 4. Input Bias Current Over Temperature

Table 1. Low I_B @ 125°C

Model	30V	16V	1.3 to 5V	Next Generation
Single	N/A	AD8663	AD8603	N/A
Dual	AD706	AD8667	AD8607	AD8622
Quad	AD704	AD8669	AD8609	AD8624

Rev. E

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REVISION HISTORY

1/10—Rev. D to Rev. E

Updated Format ..... Universal
Changes to Features and General Description Section, Added Table 1, Renumbered Sequentially 1
Changes to Table 2 3
Changes to Table 3 5
Updated Outline Dimensions 13
Changes to Ordering Guide 14

12/09—Rev. C to Rev. D

Updated Outline Dimensions 10
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11/01—Rev. B to Rev. C

Edits to Features 1
Edits to Product Description 1
Edits to Absolute Maximum Ratings 3
Deleted Metalization Photograph 3
Edits to Ordering Guide 4

SPECIFICATIONS

T_A = 25°C, V_{CM} = 0 V, and V_S =±15 V dc, unless otherwise noted.

Table 2.

Parameters	Conditions	AD704J/A Min	AD704J/A Typ	AD704J/A Max	Unit
INPUT OFFSET VOLTAGE					
Initial Offset			50	150	µV
Offset	T_{MIN} – T_{MAX}		100	250	µV
vs. Temp, Average TC			0.2	1.5	µV/°C
vs. Supply (PSRR)	V_S = ±2 V to ±18 V	100	132		dB
T_{MIN} – T_{MAX}	V_S = ±2.5 V to ±18 V	100	126		dB
Long-Term Stability			0.3		µV/month
INPUT BIAS CURRENT[1]	V_{CM} = 0 V		100	270	pA
	V_{CM} = ±13.5 V			300	pA
vs. Temp, Average TC			0.3		pA/°C
T_{MIN} – T_{MAX}	V_{CM} = 0 V			300	pA
	V_{CM} = ±13.5 V			400	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		80	250	pA
	V_{CM} = ±13.5 V			300	pA
vs. Temp, Average TC			0.6		pA/°C
T_{MIN} – T_{MAX}	V_{CM} = 0 V		100	300	pA
	V_{CM} = ±13.5 V		100	400	pA
MATCHING CHARACTERISTICS					
Offset Voltage				250	µV
	T_{MIN} – T_{MAX}			400	µV
Input Bias Current[2]				500	pA
	T_{MIN} – T_{MAX}			600	pA
Common-Mode Rejection[3]		94			dB
	T_{MIN} – T_{MAX}	94			dB
Power Supply Rejection[4]		94			dB
	T_{MIN} – T_{MAX}	94			dB
Crosstalk[5]	f = 10 Hz				
	R_{LOAD} = 2 kΩ		150		dB
FREQUENCY RESPONSE UNITY GAIN					
Crossover Frequency			0.8		MHz
Slew Rate, Unity Gain	G = –1		0.15		V/µs
Slew Rate	T_{MIN} – T_{MAX}		0.1		V/µs
INPUT IMPEDANCE					
Differential			40||2		MΩ||pF
Common-Mode			300||2		GΩ||pF
INPUT VOLTAGE RANGE					
Common-Mode Voltage		±13.5	±14		V
Common-Mode Rejection Ratio	V_{CM} = ±13.5 V	100	132		dB
	T_{MIN} – T_{MAX}	98	128		dB
INPUT CURRENT NOISE	0.1 Hz to 10 Hz		3		pA p-p
	f = 10 Hz		50		fA/√Hz
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		0.5		µV p-p
	f = 10 Hz		17		nV/√Hz
	f = 1 kHz		15	22	nV/√Hz

Parameters	Conditions	AD704J/A Min	Typ	Max	Unit
OPEN-LOOP GAIN	V_O = ±12 V				
	R_{LOAD} = 10 kΩ	200	2000		V/mV
	T_{MIN} – T_{MAX}	150	1500		V/mV
	V_O = ±10 V				
	R_{LOAD} = 2 kΩ	200	1000		V/mV
	T_{MIN} – T_{MAX}	150	1000		V/mV
OUTPUT CHARACTERISTICS					
Voltage Swing	R_{LOAD} = 10 kΩ				V
	T_{MIN} – T_{MAX}	±13	±14		
Current	Short circuit		±15		mA
CAPACITIVE LOAD					
Drive Capability	Gain = 1		10,000		pF
POWER SUPPLY					
Rated Performance			±15		V
Operating Range		±2.0		±18	V
Quiescent Current			1.5	2.4	mA
	T_{MIN} – T_{MAX}		1.6	2.6	mA
TRANSISTOR COUNT	Number of transistors		180		

[1] Bias current specifications are guaranteed maximum at either input.
[2] Input bias current match is the maximum difference between corresponding inputs of all four amplifiers.
[3] CMRR match is the difference of $\Delta V_{OS}/\Delta V_{CM}$ between any two amplifiers, expressed in dB.
[4] PSRR match is the difference between $\Delta V_{OS}/\Delta V_{SUPPLY}$ for any two amplifiers, expressed in dB.
[5] See Figure 5 for test circuit.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation (25°C)[1]	
Input Voltage	$\pm V_S$
Differential Input Voltage[2]	±0.7 V
Output Short-Circuit Duration (Single Input)	Indefinite
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	
AD704J	0°C to 70°C
AD704A	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] Specification is for the device in free air:
14-lead plastic package: θ_{JA} = 150°C/W.
16-lead SOIC package: θ_{JA} = 100°C/W.
20-terminal LCC package: θ_{JA} = 150°C/W.

[2] The input pins of this amplifier are protected by back-to-back diodes. If the differential voltage exceeds ±0.7 volts, external series protection resistors should be added to limit the input current to less than 25 mA.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

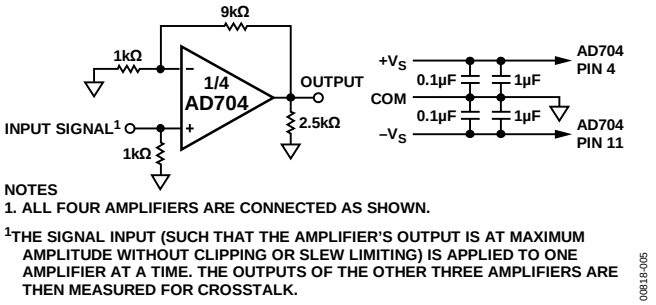


Figure 5. Crosstalk Test Circuit

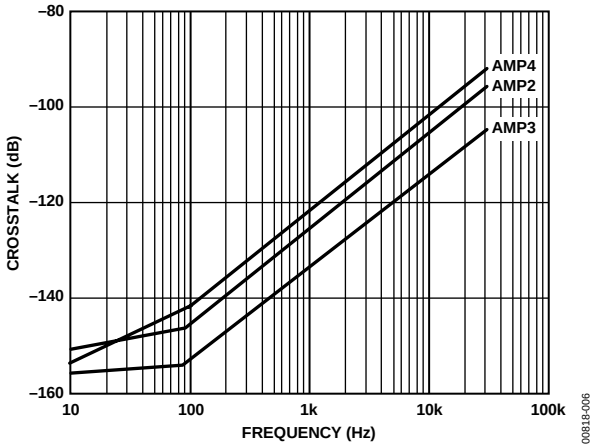


Figure 6. Crosstalk vs. Frequency

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15 V dc, unless otherwise noted.

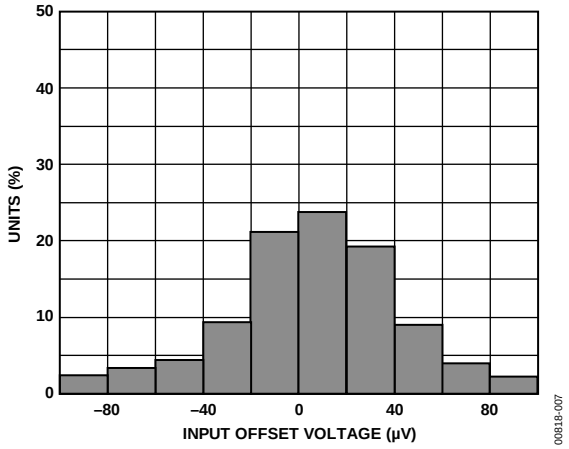


Figure 7. Typical Distribution of Input Offset Voltage

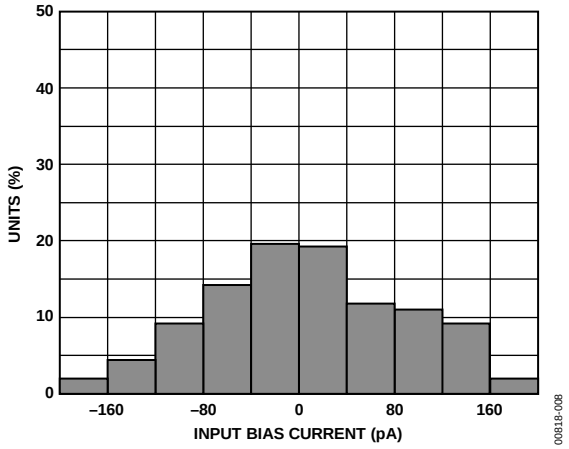


Figure 8. Typical Distribution of Input Bias Current

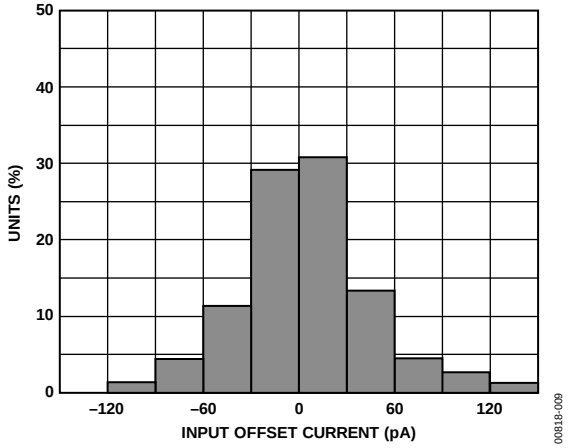


Figure 9. Typical Distribution of Input Offset Current

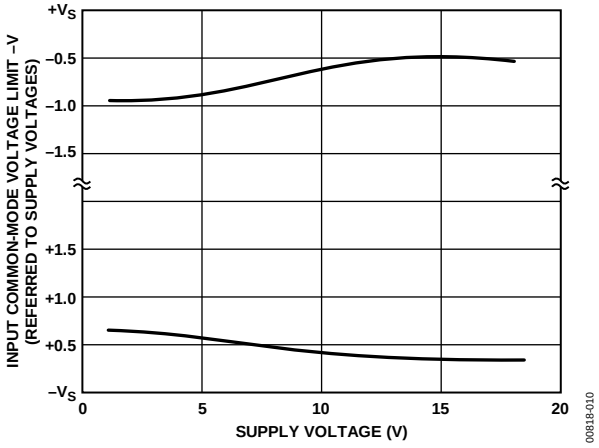


Figure 10. Input Common-Mode Voltage Range vs. Supply Voltage

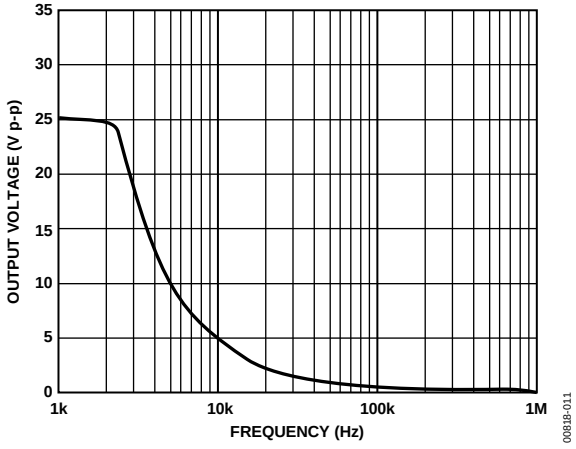


Figure 11. Large Signal Frequency Response

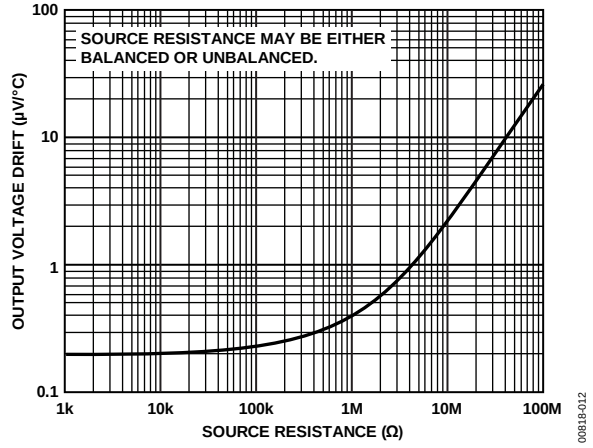


Figure 12. Offset Voltage Drift vs. Source Resistance

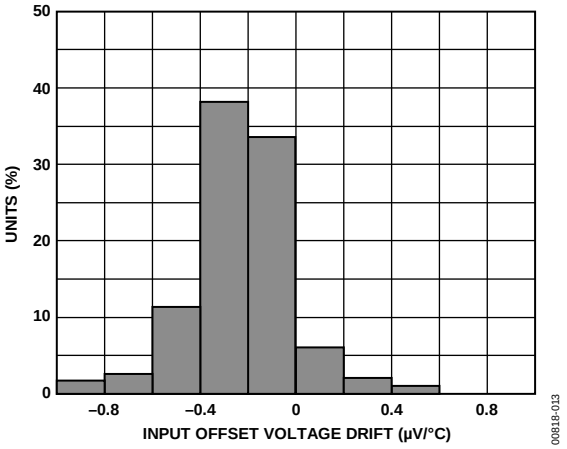


Figure 13. Typical Distribution of Input Offset Voltage Drift

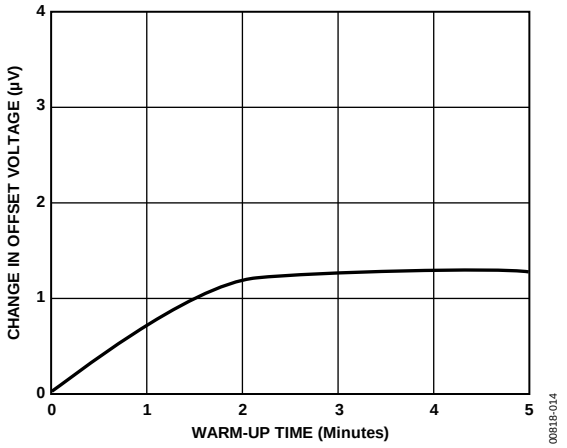


Figure 14. Change in Input Offset Voltage vs. Warm-Up Time

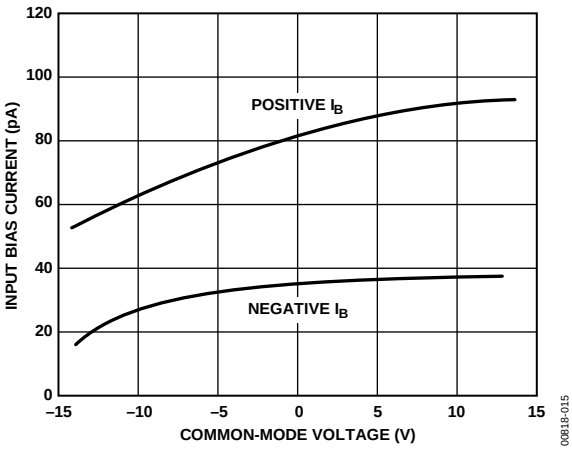


Figure 15. Input Bias Current vs. Common-Mode Voltage

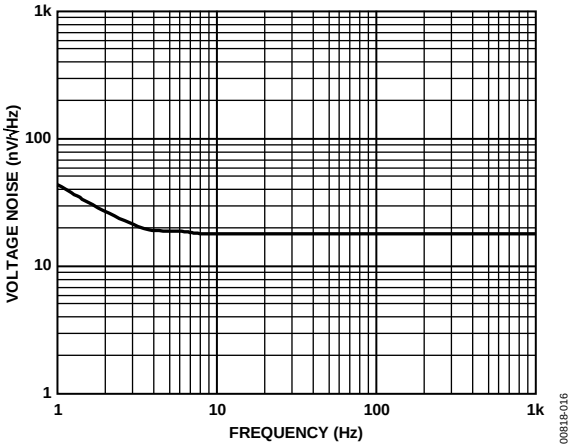


Figure 16. Input Noise Voltage Spectral Density

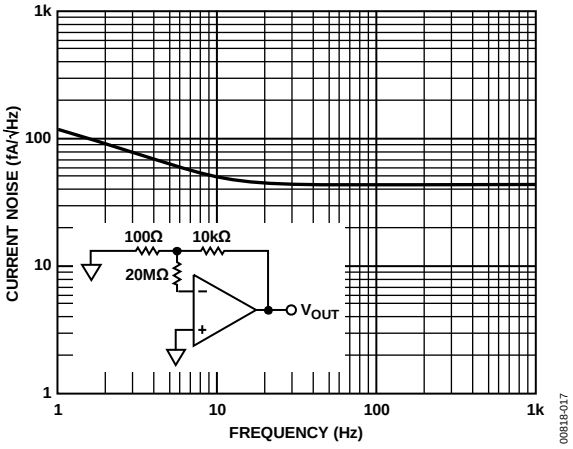


Figure 17. Input Noise Current Spectral Density

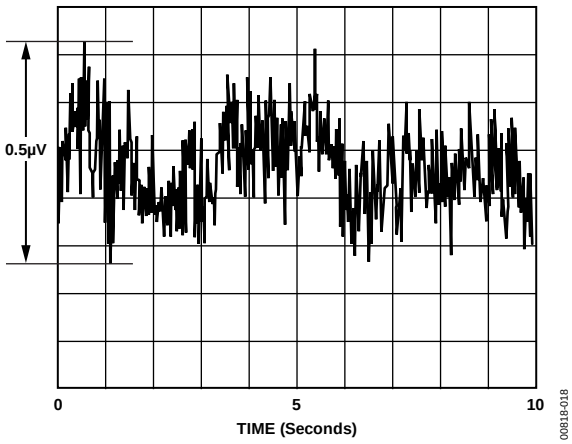


Figure 18. 0.1 Hz to 10 Hz Noise Voltage

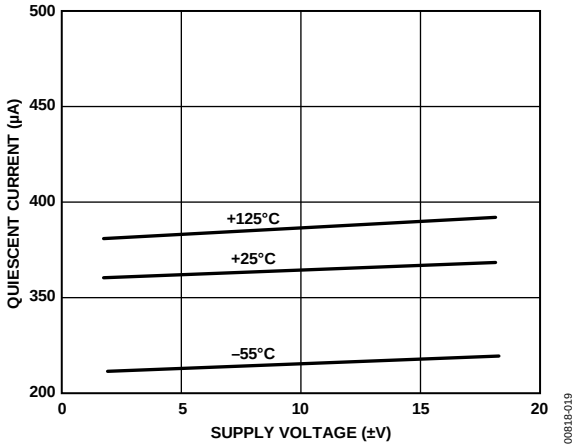


Figure 19. Quiescent Supply Current vs. Supply Voltage (per Amplifier)

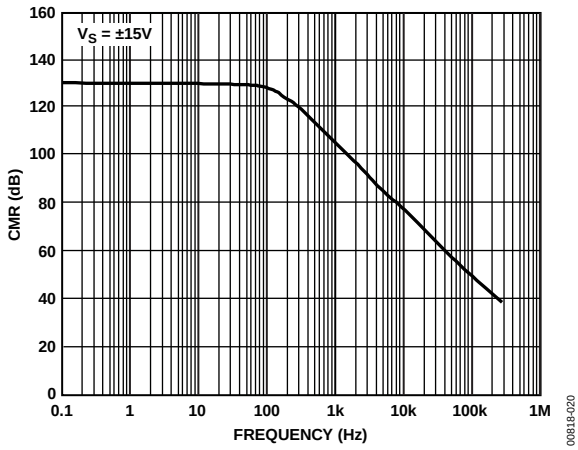


Figure 20. Common-Mode Rejection vs. Frequency

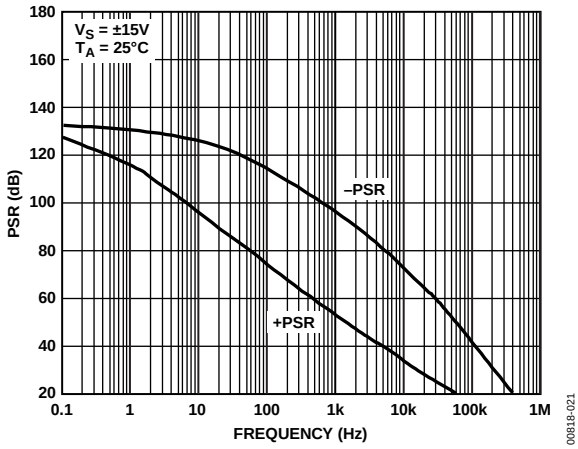


Figure 21. Power Supply Rejection vs. Frequency

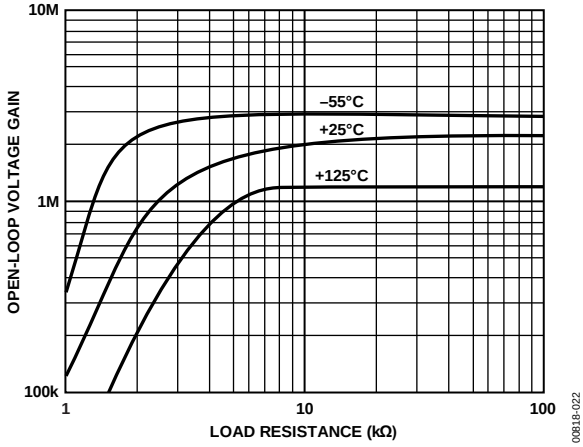


Figure 22. Open-Loop Gain vs. Load Resistance Over Temperature

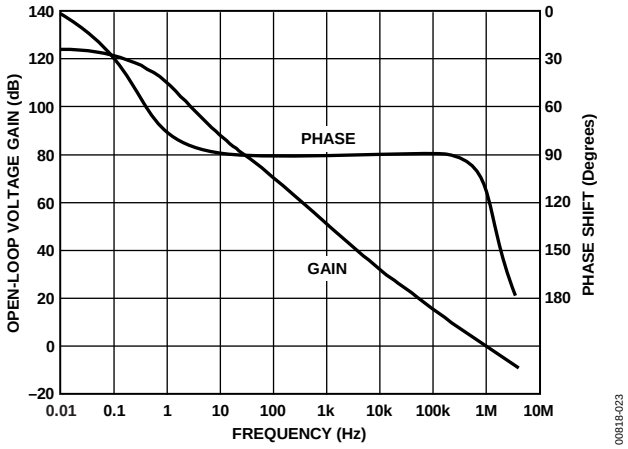


Figure 23. Open-Loop Gain and Phase vs. Frequency

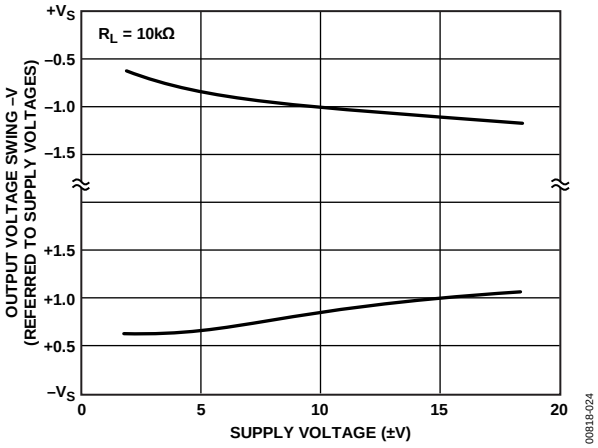


Figure 24. Output Voltage Swing vs. Supply Voltage

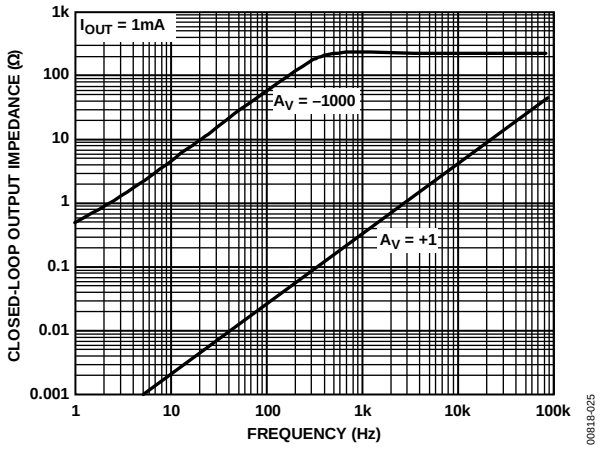


Figure 25. Closed-Loop Output Impedance vs. Frequency

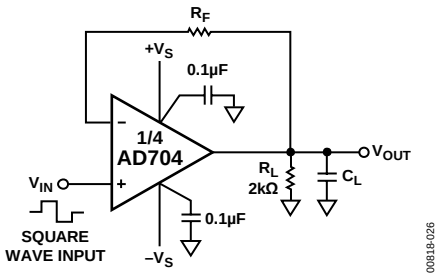


Figure 26. Unity Gain Follower (for Large Signal Applications, Resistor R_F Limits the Current Through the Input Protection Diodes)

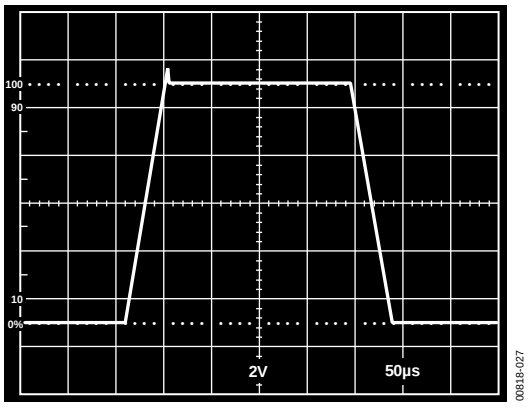


Figure 27. Unity Gain Follower Large Signal Pulse Response R_F = 10 kΩ, C_L = 1000 pF

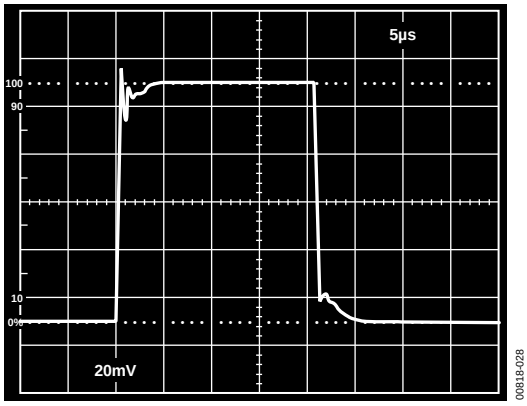


Figure 28. Unity Gain Follower Small Signal Pulse Response R_F = 0 Ω, C_L = 100 pF

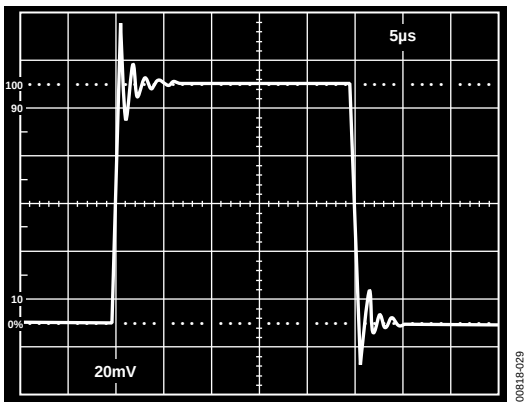


Figure 29. Unity Gain Follower Small Signal Pulse Response R_F = 0 Ω, C_L = 1000 pF

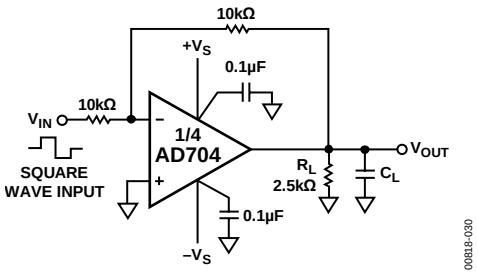


Figure 30. Unity Gain Inverter Connection

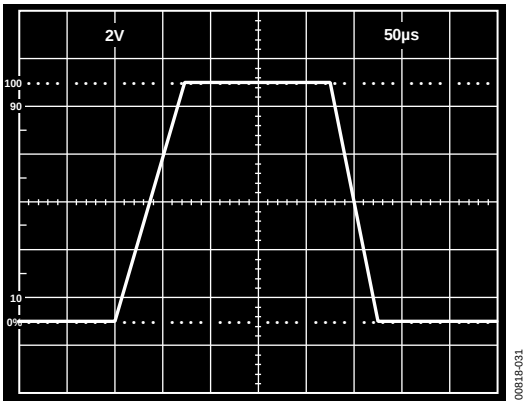


Figure 31. Unity Gain Inverter Large Signal Pulse Response, C_L = 1000 pF

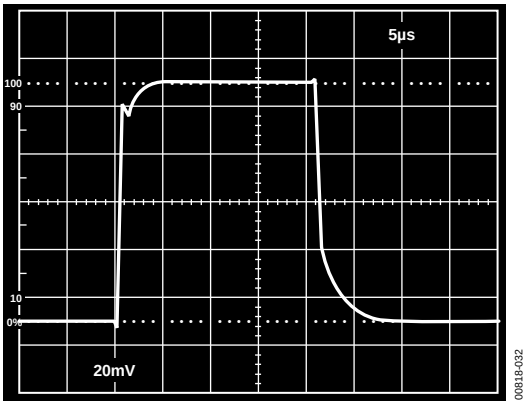


Figure 32. Unity Gain Inverter Small Signal Pulse Response, C_L = 100 pF

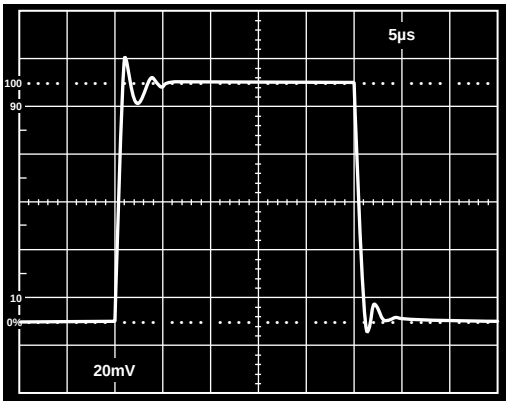
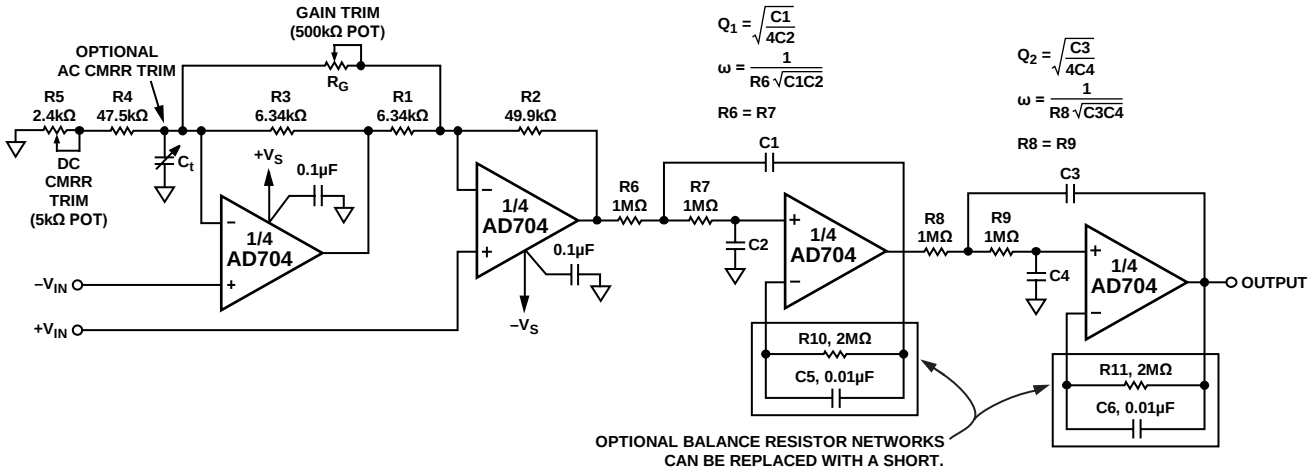


Figure 33. Unity Gain Inverter Small Signal Pulse Response, C_L = 1000 pF

THEORY OF OPERATION



NOTES
1. INSTRUMENTATION AMPLIFIER GAIN = $1 + \frac{R2}{R1} + \frac{2R2}{R_G}$ (FOR R1 = R3, R2 = R4 + R5).
2. CAPACITORS C2 AND C4 ARE SOUTHERN ELECTRONICS MPCC, POLYCARBONATE, ±5%, 50V.
3. ALL RESISTORS METAL FILM, 1%.

00818-034

Figure 34. Gain-of-10 Instrumentation Amplifier with Post Filtering

The instrumentation amplifier with post filtering (see Figure 34) combines two applications that benefit greatly from the AD704. This circuit achieves low power and dc precision over temperature with a minimum of components.

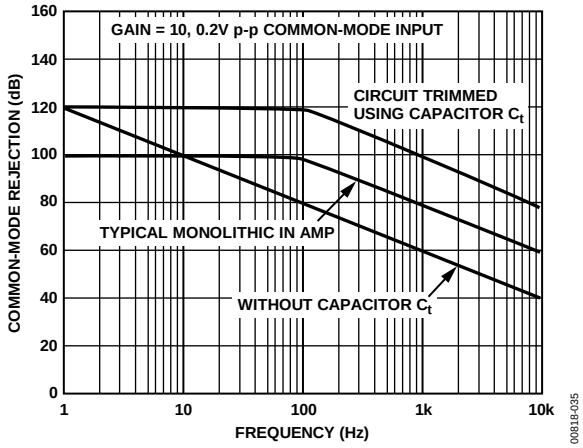
The instrumentation amplifier circuit offers many performance benefits, including BiFET level input bias currents, low input offset voltage drift, and only 1.2 mA quiescent current. It operates for gains that are G ≥ 2 and, at lower gains, it benefits from no output amplifier offset and no noise contribution as encountered in a 3-op-amp design. Good low frequency CMRR is achieved even without the optional ac CMRR trim (see Figure 35). Table 4 provides resistance values for three common circuit gains. For other gains, use the following equations:

$$R2 = R4 + R5 = 49.9\ \text{k}\Omega$$

$$R1 = R3 = \frac{49.9\ \text{k}\Omega}{0.9\,G - 1}$$

$$Max\ Value\ of\ R_G = \frac{99.8\ \text{k}\Omega}{0.06\,G}$$

$$C_t \approx \frac{1}{2\pi\,(R3)\,5 \times 10^5}$$



00818-035

Figure 35. Common-Mode Rejection vs. Frequency with and Without Capacitor C_t

Table 4. Resistance Values for Various Gains

Circuit Gain (G)	R1 and R3	R_G (Max Value of Trim Potentiometer)	Bandwidth (−3 dB), Hz
10	6.34 kΩ	166 kΩ	50 k
100	526 Ω	16.6 kΩ	5k
1000	56.2 Ω	1.66 kΩ	0.5 k

The 1 Hz, four-pole active filter offers dc precision with a minimum of components and cost. The low current noise, I_{OS}, and I_B allow the use of 1 MΩ resistors without sacrificing the 1 µV/°C drift of the AD704. This means that lower capacitor values can be used, reducing cost and space. Furthermore, because the AD704's I_B is as low as its I_{OS}, over most of the MIL temperature range, most applications do not require the use of the normal balancing resistor (with its stability capacitor). Adding the optional balancing resistor enhances performance at high temperatures, as shown in Figure 36. Table 5 gives capacitor values for several common low pass responses.

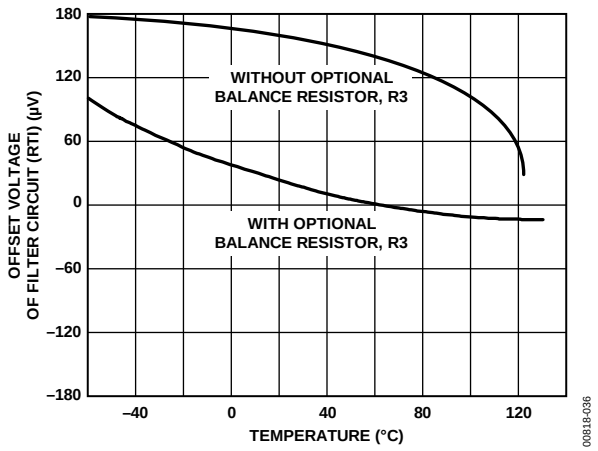


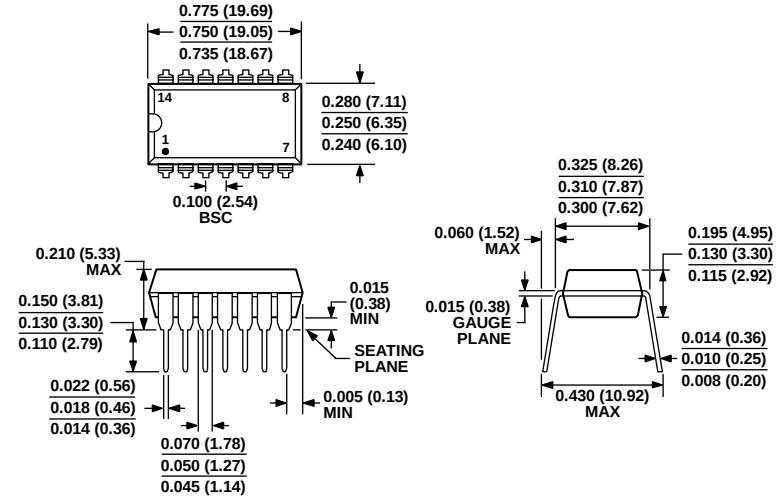
Figure 36. V_{OS} vs. Temperature Performance of the 1 Hz Filter Circuit

Table 5. 1 Hz, Four-Pole Low-Pass Filter Recommended Component Values[1]

Desired Low Pass Response	Section 1 Frequency (Hz)	Q	Section 2 Frequency (Hz)	Q	C1 (µF)	C2 (µF)	C3 (µF)	C4 (µF)
Bessel	1.43	0.522	1.60	0.806	0.116	0.107	0.160	0.0616
Butterworth	1.00	0.541	1.00	1.31	0.172	0.147	0.416	0.0609
0.1 dB Chebychev	0.648	0.619	0.948	2.18	0.304	0.198	0.733	0.0385
0.2 dB Chebychev	0.603	0.646	0.941	2.44	0.341	0.204	0.823	0.0347
0.5 dB Chebychev	0.540	0.705	0.932	2.94	0.416	0.209	1.00	0.0290
1.0 dB Chebychev	0.492	0.785	0.925	3.56	0.508	0.206	1.23	0.0242

[1] Specified values are for a −3 dB point of 1.0 Hz. For other frequencies, simply scale the C1 through C4 capacitors directly; that is, for a 3 Hz Bessel response, C1 = 0.0387 µF, C2 = 0.0357 µF, C3 = 0.0533 µF, and C4 = 0.0205 µF.

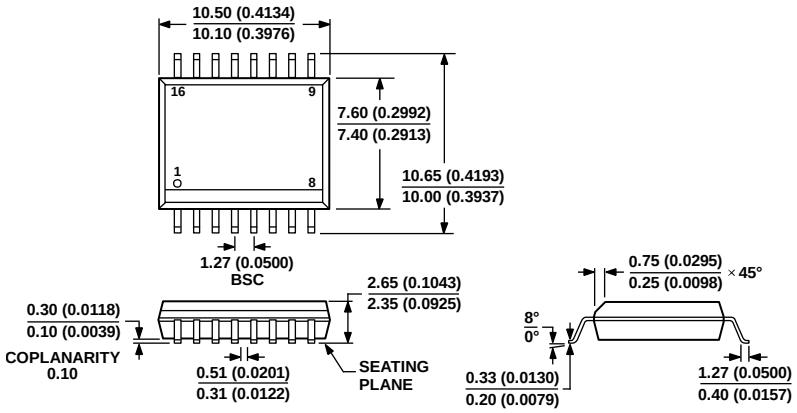
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 37. 14-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body (N-14)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

032707-B

Figure 38. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimensions shown in millimeters and (inches)

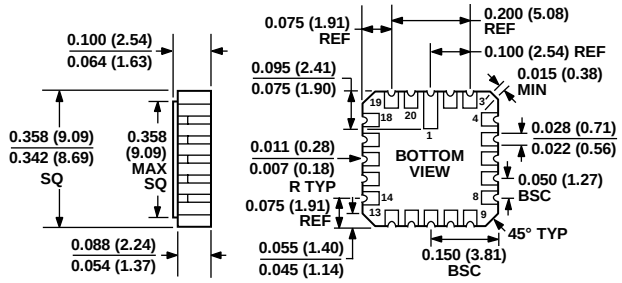


Figure 39. 20-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-20-1)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD704AR-16	−40°C to +85°C	16-Lead SOIC_W	RW -16
AD704AR-16-REEL	−40°C to +85°C	16-Lead SOIC_W	RW -16
AD704ARZ-16	−40°C to +85°C	16-Lead SOIC_W	RW -16
AD704ARZ-16-REEL	−40°C to +85°C	16-Lead SOIC_W	RW -16
AD704JN	0°C to 70°C	14-Lead PDIP	N-14
AD704JNZ	0°C to 70°C	14-Lead PDIP	N-14
AD704JR-16	0°C to 70°C	16-Lead SOIC_W	RW -16
AD704JR-16-REEL	0°C to 70°C	16-Lead SOIC_W	RW -16
AD704JRZ-16	0°C to 70°C	16-Lead SOIC_W	RW -16
AD704JRZ-16-REEL	0°C to 70°C	16-Lead SOIC_W	RW -16
AD704SE/883B	−55°C to +125°C	20-Terminal LCC	E-20-1

[1] Z = RoHS Compliant Part.

NOTES

NOTES

D00818-0-1/10(E)