2-Phase, High Efficiency DC/DC Controller for Intel Mobile CPUs

FEATURES

- **Output Stages Operate Antiphase**
- **±1% Output Voltage Accuracy**
- **6-Bit IMVP-IV VID Code: V_{OUT} = 0.7V to 1.708V**
- **Intel Compatible Power Saving Mode (PSIB)**
- **Stage Shedding Improves Low Current Efficiency**
- **Power Good Output with Adaptive Masking**
- **Lossless Voltage Positioning**
- **Dual Input Supply Capability for Load Sharing**
- Resistor Programmable V_{OUT} at Boot-Up and Deeper Sleep State
- Resistor Programmable Deep Sleep Offset
- Programmable Fixed Frequency: 210kHz to 550kHz
- Adjustable Soft-Start Current Ramping
- Foldback Output Current Limit
- Short-Circuit Shutdown Timer with Defeat Option
- Overvoltage Protection
- Available in 36-Lead SSOP (0.209 Wide) and 38-Lead (5mm × 7mm) Packages

APPLICATIONS

- Mobile and Desktop Computers
- Internet Servers

DESCRIPTION

The LTC®3735 is a 2-phase synchronous step-down switching regulator controller that drives all N-channel power MOSFETs in a constant frequency architecture. The output voltage is programmable by six VID bits during normal operation and by external resistors during initial boot-up and deeper sleep state. The LTC3735 drives its two output stages out-of-phase at frequencies up to 550kHz to minimize the RMS ripple currents in both input and output capacitors. This antiphase technique also doubles the apparent switching frequency, improving the transient response while operating each phase at an optimum frequency for efficiency. Thermal design is further simplified by cycle-by-cycle current sharing between the two phases.

An Intel compatible PSIB input is provided to select between two modes of operation. Fully enhanced synchronous mode achieves a very small output ripple and very fast transient response while power saving mode realizes very high efficiency. OPTI-LOOP® compensation allows the transient response to be optimized for a wide range of output capacitance and ESR values.

TYPICAL APPLICATION

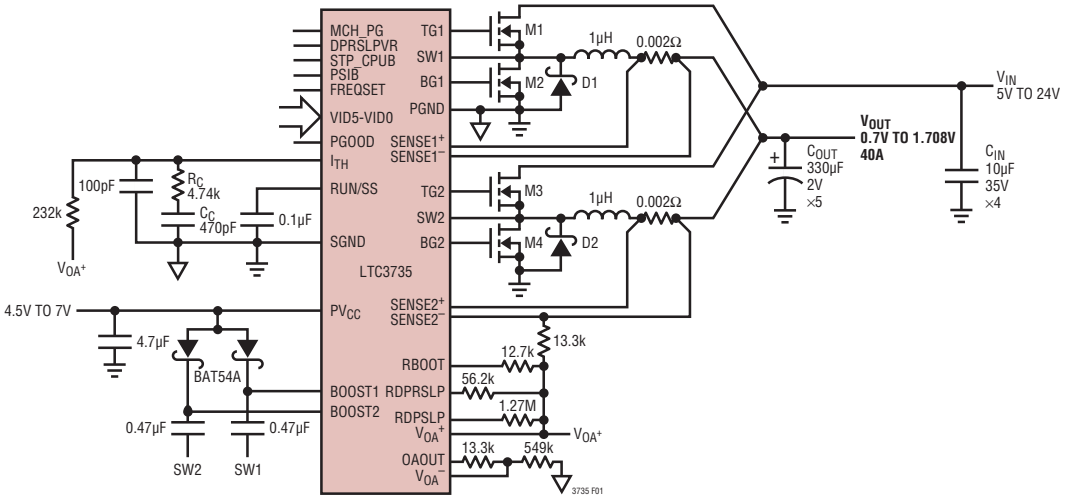


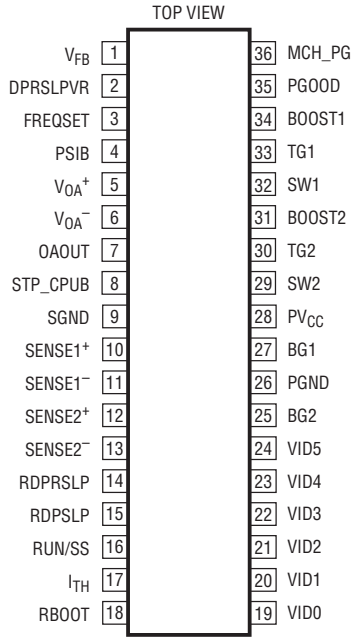
Figure 1. High Current 2-Phase Step-Down Converter

ABSOLUTE MAXIMUM RATINGS (Note 1)

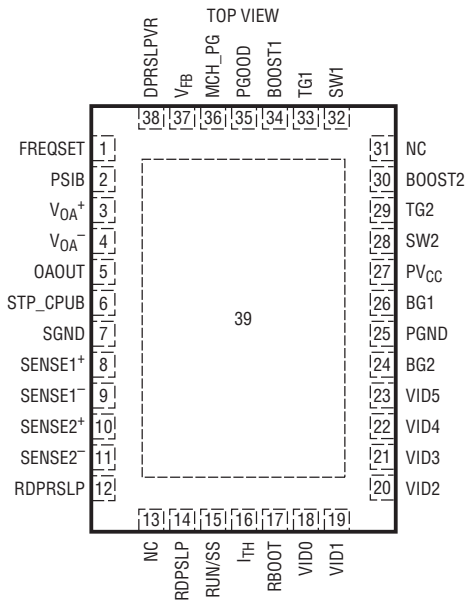
Input Supply Voltage (PV_{CC}) ..... 7V to –0.3V
Topside Driver Voltages (BOOST1,2) ..... 38V to –0.3V
Switch Voltage (SW1, 2) ..... 32V to –5V
Boosted Driver Voltages
(BOOST1-SW1, BOOST2-SW2) ..... 7V to –0.3V
DPRSLPVR, STP_CPUB, MCH_PG, PGOOD,
RDPRSLP, RDPSLP, RBOOT Voltages ..... 5V to –0.3V
RUN/SS, PSIB, FREQSET Voltages .....7V to –0.3V
VID0-VID5 Voltages .....5V to –0.3V
V_{FB}, Voltage ..... 2V to –0.3V
V_{OA}^+, V_{OA}^- ..... 3.6V to –0.3V

Peak Gate Drive Current <1µs
(TG1, TG2, BG1, BG2).....5A
Operating Ambient Temperature Range
(Note 2) ..... –40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range
SSOP ..... –65°C to 150°C
QFN..... –65°C to 125°C
QFN Reflow Peak Body Temperature..... 260°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



G PACKAGE
36-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 85°C/W



UHF PACKAGE
38-LEAD (7mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) IS SIGNAL GROUND, MUST BE CONNECTED TO PCB AND SGND

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3735EG#PBF	LTC3735EG#TRPBF	LTC3735	36-Lead Plastic SSOP	–40°C to 85°C
LTC3735EUHF#PBF	LTC3735EUHF#TRPBF	LTC3735	38-Lead (7mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{PVCC} = 5V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
Reference	Regulated Feedback Voltage	I_{TH} Voltage = 0.5V; Measured at V_{FB} (Note 4)			0.600		V
$V_{SENSEMAX}$	Maximum Current Sense Threshold	I_{TH} Voltage = Max; V_{CM} = 1.7V	●	59	72	85	mV
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop, ΔI_{TH} Voltage: 1.2V to 0.7V Measured in Servo Loop, ΔI_{TH} Voltage: 1.2V to 2V	 ● ●		 0.1 –0.1	 0.5 –0.5	 % %
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{PVCC} = 4.5V to 7V			0.02	0.1	%/V
V_{PSIB}	Forced Continuous Threshold			0.57	0.6	0.63	V
I_{PSIB}	Forced Continuous Current	V_{PSIB} = 0V			–0.5	–1	µA
V_{OVL}	Output Overvoltage Threshold	Measured with Respect to V_{FB} = 0.6V		0.64	0.66	0.68	V
g_m	Transconductance Amplifier g_m	I_{TH} = 1.2V, Sink/Source 25µA (Note 4)	●	4.5	6	7.5	mmho
g_{mOL}	Transconductance Amplifier Gain	I_{TH} = 1.2V, (g_m • Z_L; No Ext Load) (Note 4)			3		V/mV
V_{ACTIVE}	Output Voltage in Active Mode	VID = 010110, I_{TH} = 0.5V (0°C to 85°C) VID = 010110, I_{TH} = 0.5V (Note 2)	 ●	1.342 1.336	1.356 1.356	1.370 1.376	V V
I_Q	Input DC Supply Current Normal Mode Shutdown	(Note 5) $V_{RUN/SS}$ = 0V			 2 20	 3 100	 mA µA
UVR	Undervoltage RUN/SS Reset	PV_{CC} Lowered Until the RUN/SS Pin is Pulled Low		3.2	3.7	4.2	V
$I_{RUN/SS}$	Soft-Start Charge Current	$V_{RUN/SS}$ = 1.9V		–2.3	–1.5	–0.8	µA
VRUN/SS	RUN/SS Pin ON Threshold	$V_{RUN/SS}$ Rising		1.0	1.5	1.9	V
$V_{RUN/SSARM}$	RUN/SS Pin Latchoff Arming	$V_{RUN/SS}$ Rising from 3V			3.9		V
$V_{RUN/SSLO}$	RUN/SS Pin Latchoff Threshold	$V_{RUN/SS}$, Ramping Negative			3.2		V
I_{SCL}	RUN/SS Discharge Current	Soft-Short Condition V_{FB} = 0.375V, $V_{RUN/SS}$ = 4.5V		–5	–1.5		µA
I_{SDLHO}	Shutdown Latch Disable Current	V_{FB} = 0.375V, $V_{RUN/SS}$ = 4.5V			1.5	5	µA
I_{SENSE}	Total Sense Pins Source Current	Each Channel: $V_{SENSE1^-, 2^-}$ = $V_{SENSE1^+, 2^+}$ = 0V		–85	–60		µA
DF_{MAX}	Maximum Duty Factor	In Dropout, $V_{SENSEMAX}$ ≤ 45mV		95	98.5		%
 TG1, 2 t_r TG1, 2 t_f	Top Gate Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 30 40	 90 90	 ns ns
 BG1, 2 t_r BG1, 2 t_f	Bottom Gate Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 60 50	 90 90	 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver (Note 6)			50		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver (Note 6)			60		ns
$t_{ON(MIN)}$	Minimum On-Time	Tested with a Square Wave (Note 7)			100		ns
VID Parameters							
R_{ATTEN}	VID Top Resistance				5.33		kΩ
$ATTEN_{ERR}$	Resistive Divider Error	(Note 8)	●	–0.25		0.25	%
VID_{THLOW}	VID0 to VID5 Logic Threshold Low					0.3	V
VID_{THHIGH}	VID0 to VID5 Logic Threshold High			0.7			V
VID_{LEAK}	VID0 to VID5 Leakage					±1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{PVCC} = 5V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator							
$I_{FREQSET}$	FREQSET Input Current	$V_{FREQSET}$ = 0V			–2	–1	µA
f_{NOM}	Nominal Frequency	$V_{FREQSET}$ = 1.2V		320	355	390	kHz
f_{LOW}	Lowest Frequency	$V_{FREQSET}$ = 0V		190	210	240	kHz
f_{HIGH}	Highest Frequency	$V_{FREQSET}$ ≥ 2.4V		490	550	610	kHz
PGOOD Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
V_{PG}	PGOOD Trip Thresholds	V_{FB} with Respect to Set Output Voltage V_{FB} Ramping Negative V_{FB} Ramping Positive		 –7 7	 –10 11	 –13 13	 % %
t_{MASK}	PGOOD Mask Timer			100	110	120	µs
t_{DELAY}	MCH_PG Delay Time				15		cycles
Operational Amplifier							
I_B	Input Bias Current				15	200	nA
V_{OS}	Input Offset Voltage Magnitude	V_{OA+} = $V_{OA–}$ 1.2V, I_{OUT} = 1mA			0.8	5	mV
CM	Common Mode Input Voltage Range			0		P_{VCC} – 1.4	V
CMRR	Common Mode Rejection Ratio	I_{OUT} = 1mA		46	70		dB
I_{CL}	Output Source Current			10	35		mA
A_{VOL}	Open-Loop DC Gain	I_{OUT} = 1mA			30		V/mV
GBP	Gain-Bandwidth Product	I_{OUT} = 1mA			2		MHz
SR	Slew Rate	R_L = 2k			5		V/µs
$V_{O(MAX)}$	Maximum High Output Voltage	I_{OUT} = 1mA		P_{VCC} – 1.2	P_{VCC} – 0.9		V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3735E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC3735EG: $T_J = T_A + (P_D \bullet 85°C/W)$

LTC3735EUHF: $T_J = T_A + (P_D \bullet 34°C/W)$

Note 4: The LTC3735 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

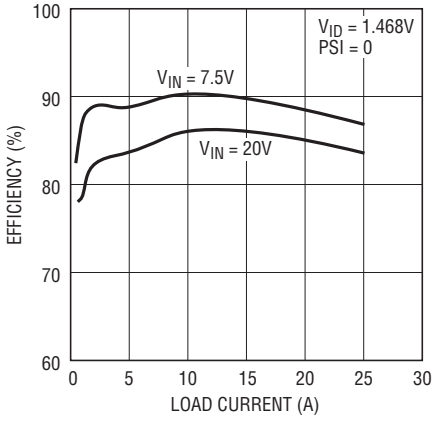
Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 7: The minimum on-time condition corresponds to the on inductor peak-to-peak ripple current ≥40% I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

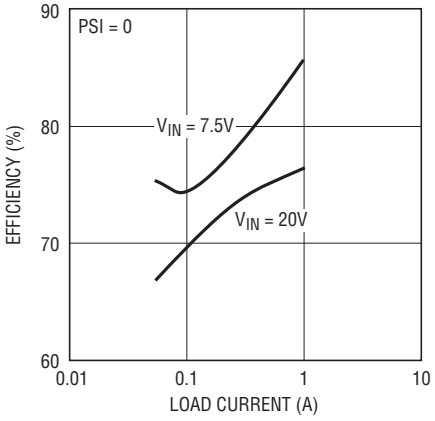
Note 8: The $ATTEN_{ERR}$ specification is in addition to the output voltage accuracy specified at VID code = 010110.

TYPICAL PERFORMANCE CHARACTERISTICS

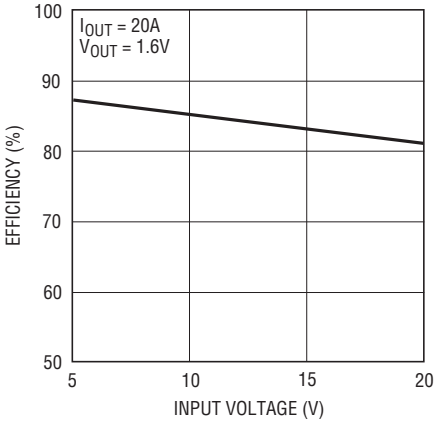
Active Mode Efficiency (Figure 14)



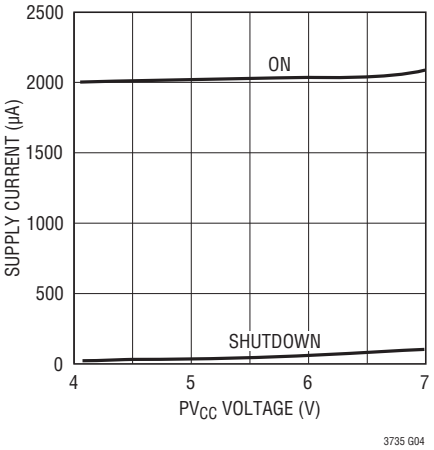
Deeper Sleep Mode Efficiency (Figure 14)



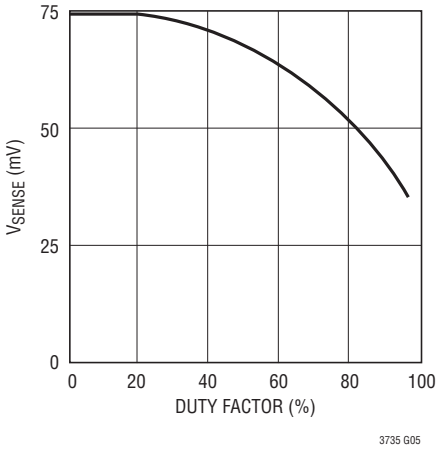
Efficiency vs Input Voltage (Figure 14)



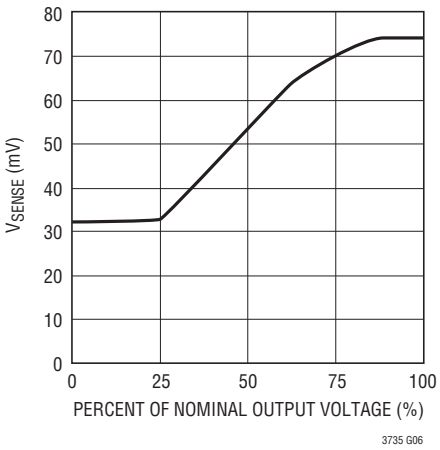
Supply Current vs PV_{CC} Voltage and Mode



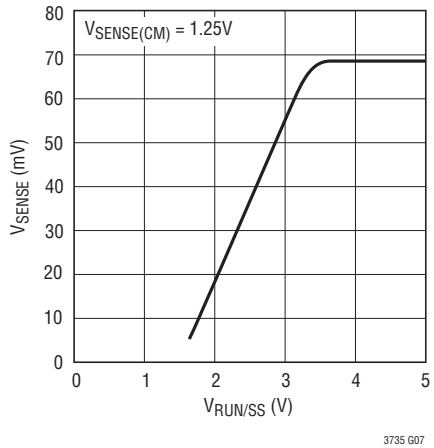
Maximum Current Sense Threshold vs Duty Factor



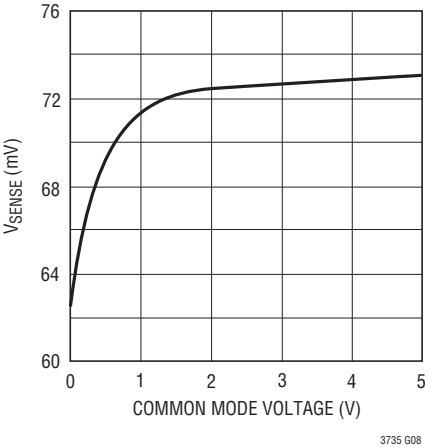
Maximum Current Sense Threshold vs Percent of Nominal Output Voltage (Foldback)



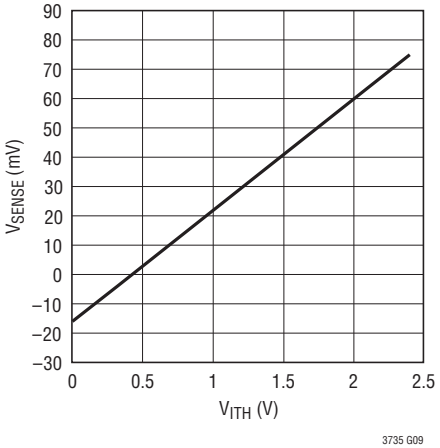
Maximum Current Sense Threshold vs $V_{RUN/SS}$ (Soft-Start)



Maximum Current Sense Threshold vs Sense Common Mode Voltage

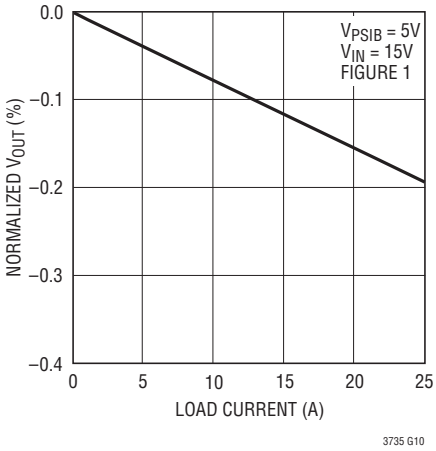


Current Sense Threshold vs I_{TH} Voltage

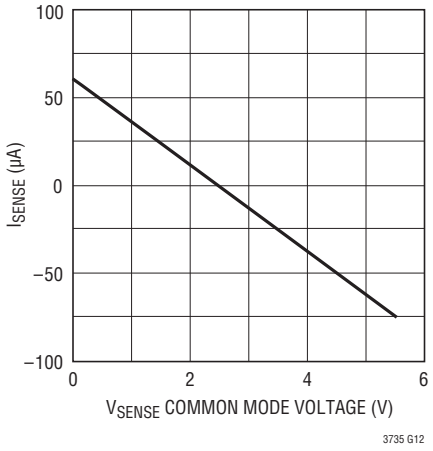


TYPICAL PERFORMANCE CHARACTERISTICS

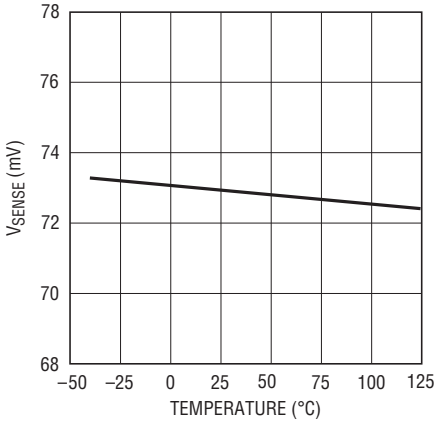
Load Regulation (Without AVP)



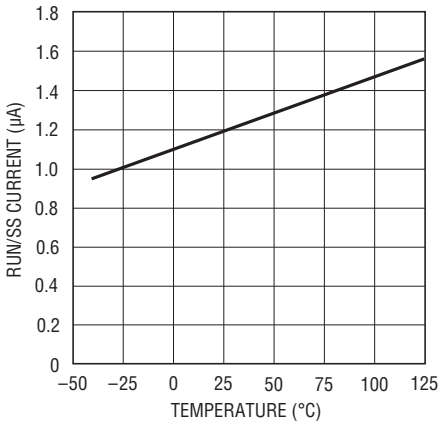
SENSE Pins Total Source Current



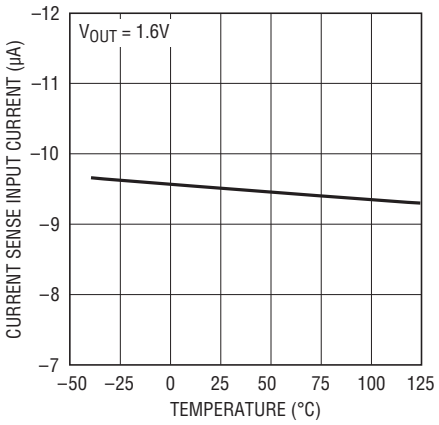
Maximum Current Sense Threshold vs Temperature



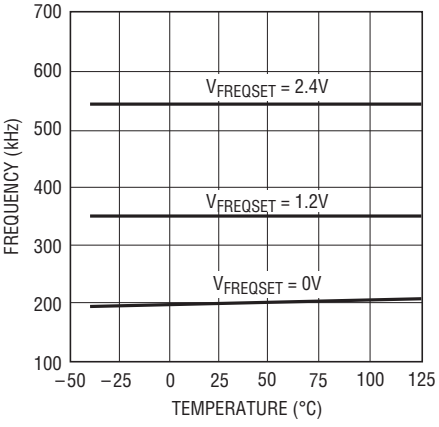
RUN/SS Current vs Temperature



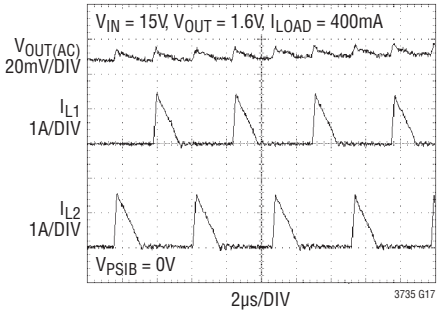
Current Sense Pin Input Current vs Temperature



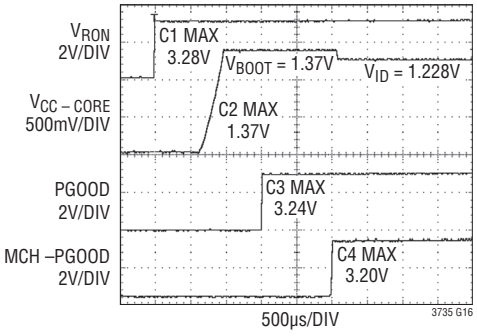
Oscillator Frequency vs Temperature



Constant Frequency Low Current Mode (Figure 14)

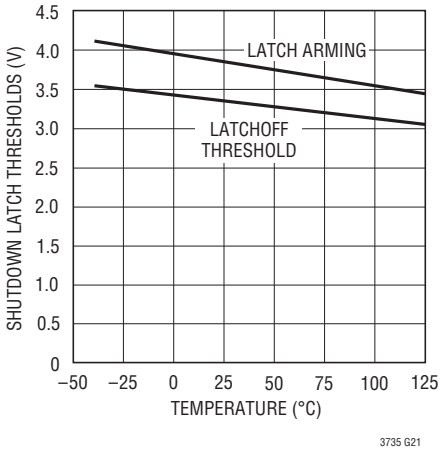


Start-Up Sequence (Figure 14)

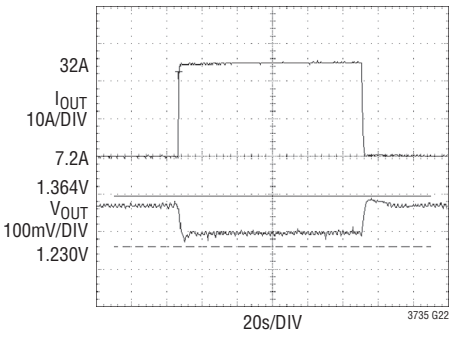


TYPICAL PERFORMANCE CHARACTERISTICS

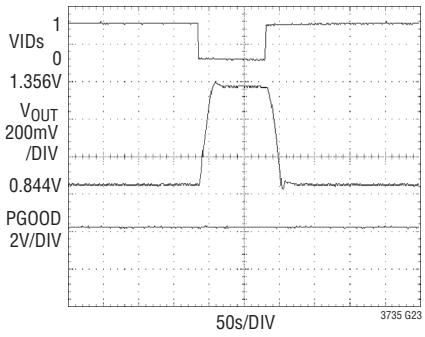
$V_{RUN/SS}$ Shutdown Latch Thresholds vs Temperature



Load Step (Figure 14)



VID Transition (Figure 14)



PIN FUNCTIONS (G/UHF)

V_{FB} (Pin 1/Pin 37): Input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage.

DPRSLPVR (Pin 2/Pin 38): Deeper Sleep State Input. When the signal to this pin is high, the voltage regulator enters deeper sleep state and its output is determined by the parallel resistor value of RDPRSLP and RDPSLP. When the signal is low, the voltage regulator exits deeper sleep state.

FREQSET (Pin 3/Pin 1): Frequency Set Pin. Apply a DC voltage between 0V and 5V to set the operating frequency of the internal oscillator. This frequency is the switching frequency of each phase.

PSIB (Pin 4/Pin 2): Power Status Indicator Input. When the signal to this pin is high, both channels operate in fully synchronous switching mode for fastest transient and lowest ripple. When the signal is low, controller enters power saving mode, providing high efficiency at light load.

V_{OA}^+, V_{OA}^- (Pins 5, 6/Pins 3, 4): Inputs to the Internal Operational Amplifier.

OAOUT (Pin 7/Pin 5): Output of the Internal Operational Amplifier.

STP_CPUB (Pin 8/Pin 6): Deep Sleep State Input. When the signal to this pin is low, the voltage regulator enters deep sleep state and its output voltage is a certain percentage lower than the VID commands. This offset percentage is set by the resistor connected to the RDPSLP pin. When the signal to this pin is high, the voltage regulator exits deep sleep state.

SGND (Pin 9/Pin 7): Signal Ground. This pin is common to both controllers. Route separately to the PGND pin.

SENSE1+, SENSE2+ (Pins 10,12/Pins 8, 9): The (+) Input to Each Differential Current Comparator. The I_{TH} pin voltage and built-in offsets between $SENSE^-$ and $SENSE^+$ pins in conjunction with R_{SENSE} set the current trip threshold.

SENSE1–, SENSE2– (Pins 11,13/Pins 10, 11): The (–) Input to Each Differential Current Comparator.

RDPRSLP (Pin 14/Pin 12): Deeper Sleep State Resistor Pin. Connect a resistor from this pin to V_{OA}^+. This resistor in conjunction with RDPSLP resistor sets the output voltage of the regulator in deeper sleep state.

RDPSLP (Pin 15/Pin 14): Deep Sleep Resistor Pin. Connect a resistor from this pin to V_{OA}^+. This resistor sets the percentage offset of output voltage in deep sleep state.

PIN FUNCTIONS (G/UHF)

RUN/SS (Pin 16/Pin 15): Combination of Soft-Start, Run Control Input and Short-Circuit Detection Timer. A capacitor to ground at this pin sets the ramp time to full current output. Forcing this pin below 1V causes the IC to shut down all internal circuitry. All functions are disabled in shutdown.

I_{TH} (Pin 17/Pin 16): Error Amplifier Output and Switching Regulator Compensation Point. Both current comparator's thresholds increase with this control voltage. The normal voltage range of this pin is from 0V to 2.4V

RBOOT (Pin 18/Pin 17): Boot-Up Resistor Pin. Connect a resistor from this pin to V_{OA}^+. This resistor sets the output voltage during the initial boot-up.

VID0–VID5 (Pins 19, 20, 21, 22, 23, 24/Pins 18, 19, 20, 21, 22, 23): VID Control Logic Input Pins.

BG2, BG1 (Pins 25, 27/Pins 24, 26): High Current Gate Drives for Bottom N-Channel MOSFETs. Voltage swing at these pins is from ground to PV_{CC}.

PGND (Pin 26/Pin 25): Driver Power Ground. Connect to sources of bottom N-channel MOSFETs and the (–) terminals of C_{IN}.

PV_{CC} (Pin 28/Pin 27): Power Supply Pin. The internal control circuits and on-chip gate drivers are powered from this voltage source. Decouple to PGND with a minimum of 4.7µF X5R/X7R ceramic capacitor placed directly adjacent to the IC.

SW2, SW1 (Pins 29, 32/Pins 28, 32): Switch Node Connections to Inductors. Voltage swing at these pins is from a Schottky diode (external) voltage drop below ground to V_{IN}.

TG2, TG1 (Pins 30, 33/Pins 29, 33): High Current Gate Drives for Top N-Channel MOSFETs. These are the outputs of floating drivers with a voltage swing equal to PV_{CC} superimposed on the switch node voltage SW.

BOOST2, BOOST1 (Pins 31, 34/Pins 30, 34): Bootstrapped Supplies to the Topside Floating Drivers. External capacitors are connected between the BOOST and SW pins, and Schottky diodes are connected between the BOOST and PV_{CC} pins.

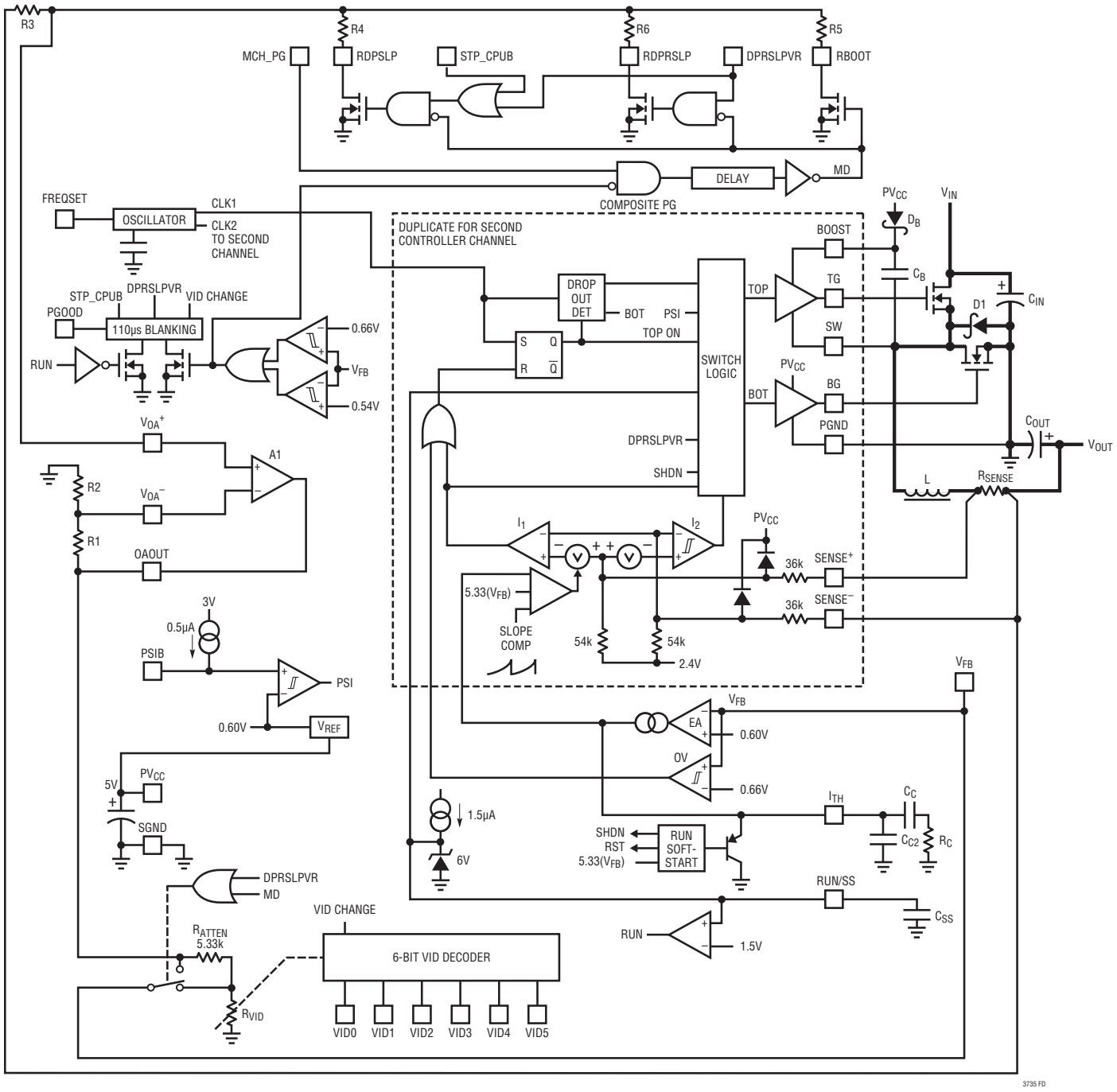
PGOOD (Pin 35/Pin 35): Power Good Indicator Output. This pin is open drain when output is within ±10% of its set point. When output is not within the ±10% window, this pin is pulled to ground. An internal timer watches over VID, state transitions overvoltage or undervoltage conditions, then masks PGOOD from going low for 110µs.

MCH_PG (Pin 36/Pin 36): MCH Power Good Input. Output voltage remains V_{BOOT} for 15 clock cycles after the assertion of MCH_PG. This delay is only sensitive to the rising edge of the MCH_PG logic signal.

SGND (Exposed Pad Pin 39, UHF Only): Signal Ground. Connect to Pins 7 and 25. The Exposed Pad must be soldered to the PCB.

NC (Pins 13, 31, UHF Only): No Connect.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3735 uses a constant frequency, current mode step-down architecture with the two output stages operating 180 degrees out of phase. During normal operation, each top MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the main current comparator, I_1, resets the RS latch. The peak inductor current at which I_1 resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of error amplifier EA. The V_{OA}^+ pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA. When the load current increases, it causes a slight decrease in EA inverting input node relative to the 0.6V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by current comparator I_2, or the beginning of the next cycle.

The top MOSFET drivers are biased from floating bootstrap capacitor C_B, which normally is recharged during each off cycle through an external diode when the top MOSFET turns off. As V_{IN} decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about 500ns every sixth cycle to allow C_B to recharge.

The main control loop is shut down by pulling the RUN/SS pin low. Releasing RUN/SS allows an internal 1.5µA current source to charge soft-start capacitor C_{SS}. When C_{SS} reaches 1.5V, the main control loop is enabled with the internal I_{TH} voltage clamped at approximately 30% of its maximum value. As C_{SS} continues to charge, the internal I_{TH} voltage is gradually released allowing normal, full-current operation.

Frequency Programming and Antiphase Operation

The switching frequency of the LTC3735 is determined by the DC voltage at the FREQSET pin. A DC voltage ranging from 0V to 2.4V moves the internal oscillator frequency from 210kHz to 550kHz.

This frequency is the actual switching frequency of either channel. Because the two channels operate 180°C out of phase, the apparent frequency at both V_{IN} and V_{OUT} is twice the actual switching frequency, minimizing ripple voltages and speeding up transient responses.

Low Current Operation (PSIB)

The PSIB pin selects between two modes of operation. When PSIB is above 0.6V, both channels operate in full synchronous switching mode. Both bottom drivers (BG1, BG2) are kept on once they are turned on until their respective oscillator sets the RS latch. The inductor current can therefore go from output back to input power supply and could potentially boost the input supply to dangerous voltage levels—BEWARE! This mode of operation is also of lower efficiency, given both channels are fully enabled and much current can circulate between input and output. However, this mode provides faster transient response, lower input noise and minimum output ripple.

When PSIB is below 0.6V, the bottom drivers (BG1, BG2) are turned off if the inductor current starts to reverse. This mode of operation prevents current going from output back to input and eliminates the conduction power loss related to circulating current. If the DPRSLPVR signal goes high in this mode, Channel 2 will be shut off and only Channel 1 will be active in supplying load current. This further eliminates power MOSFET gate driving and transition losses of Channel 2. Since DPRSLPVR indicates the entry to deeper sleep state, this “channel shedding” technique optimizes the voltage regulator efficiency at light loads. Table 1 summarizes the operation modes for different pin configurations.

Table 1. Low Current Operation Modes

PSIB	DPRSLPVR	OPERATION MODE
High	High or Low	Both Channels ON, Fully Synchronous Switching, Inductor Current is Allowed to Reverse
Low	Low	Both Channels ON; Reverse Current is Prevented
Low	High	Channel 2 is Shut Off, Reverse Current is Prevented

OPERATION (Refer to Functional Diagram)

Output Voltage at Start-Up and at Deeper Sleep State

Under normal conditions, the output voltage of the regulator is commanded by six VID bits, except at start-up and at deeper sleep state. At start-up, the RUN/SS capacitor starts to charge up and its voltage limits the inrush current from the input power source. This linearly rising current limit provides a controlled output voltage rise. During start-up, the VID command is ignored and the output set point is determined by the value of the resistor connected to the RBOOT pin. The VID bits continue to be ignored for 15 switching cycles after the completion of the following two conditions: 1) output voltage has risen up and has regulated 2) MCH_PG signal has asserted. After 15 switching cycles, output voltage is fully commanded by VID bits.

In deeper sleep state, the VID command and STP_CPUB signal are ignored and the output set point is determined by the parallel value of the resistors at the RDPRSLP pin and RDPSLP pin.

Operational Amplifier and Deep Sleep Offset

The internal operational amplifier provides a programmable output offset at deep sleep state (when the STP_CPUB signal is low). The offset percentage is programmed by the resistor from RDPSLP to V_{OA}^+ and the resistor from output to V_{OA}^+. The amplifier has an output slew rate of 5V/µs and is capable of driving capacitive loads with an output RMS current typically up to 40mA. The open-loop gain of the amplifier is >120dB and the unity-gain bandwidth is 2MHz.

Output Overvoltage Protection

An overvoltage comparator, OV, guards against transient overshoots (>10%) as well as other more serious conditions that may overvoltage the output. In this case, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Power Good

The PGOOD pin is connected to the drain of an internal N-channel MOSFET. The MOSFET turns on when the output voltage is not within ±10% of its nominal set point. When the output voltage is within ±10% of its nominal set point, the MOSFET turns off and PGOOD is high impedance. PGOOD monitors the V_{BOOT} voltage when MCH_PG is not asserted. During VID, deep sleep or deeper sleep transitions, PGOOD is masked from going low for 110µs, preventing the system from resetting during CPU mode changes. When VID bits, STP_CPUB or DPRSLPVR signals change again after a previous transition, but before the timer expires, the internal timer resets.

Short-Circuit Detection

The RUN/SS capacitor is used initially to limit the inrush current from the input power source. Once the controllers have been given time, as determined by the capacitor on the RUN/SS pin, to charge up the output capacitors and provide full-load current, the RUN/SS capacitor is then used as a short-circuit timeout circuit. If the output voltage falls to less than 70% of its nominal output voltage the RUN/SS capacitor begins discharging assuming that the output is in a severe overcurrent and/or short-circuit condition. If the condition lasts for a long enough period as determined by the size of the RUN/SS capacitor, the controller will be shut down until the RUN/SS pin voltage is recycled. This built-in latchoff can be overidden by providing a current >5µA to the RUN/SS pin. This current shortens the soft-start period but also prevents net discharge of the RUN/SS capacitor during a severe overcurrent and/or short-circuit condition. Foldback current limiting is activated when the output voltage falls below 70% of its nominal level whether or not the short-circuit latchoff circuit is enabled.

APPLICATIONS INFORMATION

The basic LTC3735 application circuit is shown in Figure 1 on the first page of this data sheet. External component selection begins with the selection of the inductors based on ripple current requirements and continues with the current sensing resistors using the calculated peak inductor current and/or maximum current limit. Next, the power MOSFETs, D1 and D2 are selected. The operating frequency and the inductor are chosen based mainly on the amount of ripple current. Finally, C_{IN} is selected for its ability to handle the input ripple current (that PolyPhase® operation minimizes) and C_{OUT} is chosen with low enough ESR to meet the output ripple voltage and load step specifications (also minimized with PolyPhase). Current mode architecture provides inherent current sharing between output stages. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 28V (limited by the external MOSFETs). Current mode control allows the ability to connect the two output stages to two *different* input power supply rails. A heavy output load can take some power from *each* input supply according to the selection of the R_{SENSE} resistors.

R_{SENSE} Selection For Output Current

$R_{SENSE1,2}$ are chosen based on the required peak output current. The LTC3735 current comparator has a maximum threshold of 72mV/R_{SENSE} and an input common mode range of SGND to PV_{CC}. The current comparator threshold sets the peak inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L.

Assuming a common input power source for each output stage and allowing a margin for variations in the LTC3735 and external component values yields:

$$R_{SENSE} = 2(40mV/I_{MAX})$$

Operating Frequency

The LTC3735 uses a constant frequency architecture with the frequency determined by an internal capacitor. This capacitor is charged by a fixed current plus an additional current which is proportional to the DC voltage applied to the FREQSET pin. The FREQSET voltage is internally set to 1.2V. It is recommended that this pin is actively biased with a resistor divider to prevent noise getting into the system.

A graph for the voltage applied to the FREQSET pin vs frequency is given in Figure 2. As the operating frequency is increased the gate drive and switching losses will be higher, reducing efficiency (see Efficiency Considerations). The maximum switching frequency is approximately 550kHz.

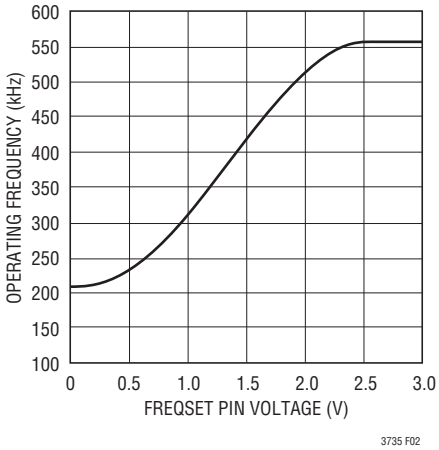


Figure 2. Operating Frequency vs $V_{FREQSET}$

Inductor Value Calculation and Output Ripple Current

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because MOSFET gate charge and transition losses increase directly with frequency. In addition to this basic tradeoff, the effect of inductor value on ripple current and low current operation must also be considered. The PolyPhase approach reduces both input and output ripple currents while optimizing individual output stages to run at a lower fundamental frequency, enhancing efficiency.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L, decreases with higher inductance or frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{V_{OUT}}{fL}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

where f is the individual output stage operating frequency.

APPLICATIONS INFORMATION

In a 2-phase converter, the net ripple current seen by the output capacitor is much smaller than the individual inductor ripple currents due to ripple cancellation. The details on how to calculate the net output ripple current can be found in Linear Technology Application Note 77.

Figure 3 shows the net ripple current seen by the output capacitors for 1- and 2-phase configurations. The output ripple current is plotted for a fixed output voltage as the duty factor is varied between 10% and 90% on the x-axis. The graph can be used in place of tedious calculations, simplifying the design process.

Accepting larger values of ΔI_L allows the use of low inductances, but can result in higher output voltage ripple. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{OUT})/2$, where I_{OUT} is the total load current. Remember, the maximum ΔI_L occurs at the maximum input voltage. The individual inductor ripple currents are determined by the frequency, inductance, input and output voltages.

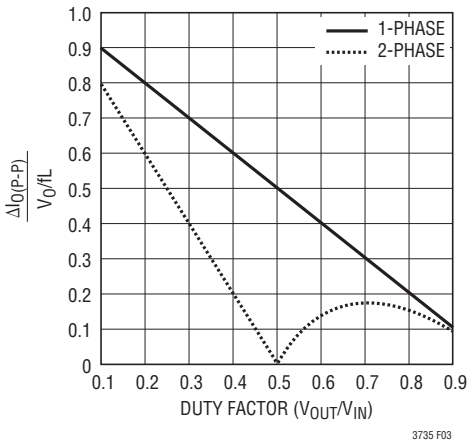


Figure 3. Normalized Output Ripple Current vs Duty Factor [$I_{RMS} \approx 0.3\ (\Delta I_{O(P-P)}$]

Inductor Core Selection

Once the values for L1 and L2 are known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy, or Kool Mμ cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductor type selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. *Do not allow the core to saturate!*

A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Coilcraft, Coiltronics, Toko and Panasonic.

Power MOSFET, D1 and D2 Selection

Two external power MOSFETs must be selected for each output stage with the LTC3735: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the PV_{CC} voltage. This voltage typically ranges from 4.5V to 7V. Consequently, logic-level threshold MOSFETs must be used in most applications. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{DS(ON)}$, gate charge Q_G, reverse transfer capacitance C_{RSS}, breakdown voltage BV_{DSS} and maximum continuous drain current $I_{D(MAX)}$.

When the LTC3735 is operating at continuous mode in a step-down configuration, the duty cycles for the top and bottom MOSFETs of each power stage are approximately:

$$\text{Top MOSFET Duty Cycle} = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$\text{Bottom MOSFET Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \quad (2)$$

APPLICATIONS INFORMATION

The conduction losses of the top and bottom MOSFETs are therefore:

$$P_{CONTOP} = \frac{V_{OUT}}{V_{IN}} \bullet \left(\frac{I_{OUT}}{2}\right)^2 \bullet (1+\delta \bullet \Delta T) \bullet R_{DS(ON)} \quad (3)$$

$$P_{CONBOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet \left(\frac{I_{OUT}}{2}\right)^2 \bullet (1+\delta \bullet \Delta T) \bullet R_{DS(ON)} \quad (4)$$

where I_{OUT} is the total output current at full load, ΔT is the difference between MOSFET operating temperature and room temperature, and δ is the temperature dependency of $R_{DS(ON)}$. δ is roughly 0.004/°C ~ 0.006/°C for low voltage MOSFETs.

The power losses of driving the top and bottom MOSFETs are simply:

$$P_{DRTOP} = Q_G \bullet PV_{CC} \bullet f \quad (5)$$

$$P_{DRBOT} = Q_G \bullet PV_{CC} \bullet f \quad (6)$$

Use Q_G data at $V_{GS} = PV_{CC}$ in MOSFET data sheets. f is the switching frequency as described previously. Please notice that the above gate driving losses are usually not dissipated by the MOSFETs. Instead they are mainly dissipated on the internal drivers of the LTC3735, if there are no resistors connected between the drive pins (TG, BG) and the gates of the MOSFETs.

The calculation of MOSFET switching loss is complicated by several factors including the wide distribution of power MOSFET threshold voltage, the nonlinearity of current rising/falling characteristic and the Miller Effect. Given the data in a typical power MOSFET data sheet, the switching losses of the top and bottom MOSFETs can only be estimated as follows:

$$P_{SWTOP} \text{ per Phase} = \frac{V_{IN}^2 \bullet I_{OUT}}{4} \bullet f \bullet C_{RSS} \bullet R_{DR} \bullet \left(\frac{1}{V_{DR} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right) \quad (7)$$

$$P_{SWBOT} \approx 0 \quad (8)$$

where R_{DR} is the effective driver resistance (of approximately 2Ω), V_{DR} is the driving voltage (= PV_{CC}) and $V_{TH(MIN)}$ is the minimum gate threshold voltage of the MOSFET. Please notice that the switching loss of the bottom MOSFET is effectively negligible because the current conduction of the antiparalleling diode. This effect is often referred as zero-voltage-transition (ZVT). Similarly when the LTC3735 converter works under fully synchronous mode at light load, the reverse inductor current can also go through the body diode of the top MOSFET and make the turn-on loss to be negligible. However, equations 7 and 8 have to be used in calculating the worst-case power loss, which happens at highest load level.

The selection criteria of power MOSFETs start with the stress check:

$V_{IN} < BV_{DSS}$

$I_{MAX} < I_{D(MAX)}$

and

$P_{CONTOP} + P_{SWTOP}$ < top MOSFET maximum power dissipation specification

$P_{CONBOT} + P_{SWBOT}$ < bottom MOSFET maximum power dissipation specification

The maximum power dissipation allowed for each MOSFET depends heavily on MOSFET manufacturing and packaging, PCB layout and power supply cooling method. Maximum power dissipation data are usually specified in MOSFET data sheets under different PCB mounting conditions.

The next step of selecting power MOSFETs is to minimize the overall power loss:

$$P_{OVL} = P_{TOP} + P_{BOT}$$

$$= (P_{CONTOP} + P_{DRTOP} + P_{SWTOP}) + (P_{CONBOT} + P_{DRBOT} + P_{SWBOT})$$

For typical mobile CPU applications where the ratio between input and output voltages is higher than 2:1, the bottom MOSFET conducts load current most of the time while the main losses of the top MOSFET are for switching and driving. Therefore a low $R_{DS(ON)}$ part (or multiple parts in parallel) would minimize the conduction loss of the bottom

APPLICATIONS INFORMATION

MOSFET while a higher $R_{DS(ON)}$ but lower Q_G and C_{RSS} part would be desirable for the top MOSFET.

The Schottky diodes, D1 and D2 in Figure 1 conduct during the dead-time between the conduction of the top and bottom MOSFETs. This helps reduce the current flowing through the body diode of the bottom MOSFET. A body diode usually has a forward conduction voltage higher than that of a Schottky and is thus detrimental to efficiency. The charge storage and reverse recovery of a body diode also cause high frequency rings at the switching nodes (the conjunction nodes between the top and bottom MOSFETs), which are again not desired for efficiency or EMI. Some power MOSFET manufacturers integrate a Schottky diode with a power MOSFET, eliminating the need to parallel an external Schottky. These integrated Schottky-MOSFETs, however, have smaller MOSFET die sizes than conventional parts and are thus not suitable for high current applications.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of each top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. A low ESR input capacitor sized for the maximum RMS current must be used. The details of a closed form equation can be found in Linear Technology Application Note 77. Figure 4 shows the input capacitor ripple current for a 2-phase configuration with the output voltage fixed and input voltage varied. The input ripple current is normalized against the DC output current. The graph can be used in place of tedious calculations. The minimum input ripple current can be achieved when the input voltage is twice the output voltage.

In the graph of Figure 4, the 2-phase local maximum input RMS capacitor currents are reached when:

$$\frac{V_{OUT}}{V_{IN}} = \frac{2k-1}{4}$$

where k = 1, 2

These worst-case conditions are commonly used for design, considering input/output variations and long term reliability. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the capacitor manufacturer if there is any question.

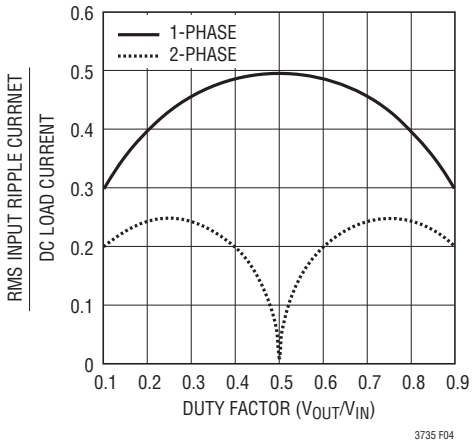


Figure 4. Normalized RMS Input Ripple Current vs Duty Factor for 1 and 2 Output Stages

It is important to note that the efficiency loss is proportional to the input RMS current *squared* and therefore a 2-phase implementation results in 75% less power loss when compared to a single phase design. Battery/input protection fuse resistance (if used), PC board trace and connector resistance losses are also reduced by the reduction of the input ripple current in a 2-phase system. The required amount of input capacitance is further reduced by the factor, 2, due to the reduction in input RMS current.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically once the ESR requirement has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirements. The steady state output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_{RIPPLE}\left(ESR + \frac{1}{16 \bullet f \bullet C_{OUT}}\right)$$

where f = operating frequency of each stage, C_{OUT} = output capacitance and ΔI_{RIPPLE} = interleaved inductor ripple currents.

ΔI_{RIPPLE} can be calculated from the duty factor and the ΔI_L of each stage. A closed form equation can be found in

APPLICATIONS INFORMATION

Linear Technology Application Note 77. Assuming inductors are selected to have same ripple percentage for both 1-phase and 2-phase configurations, Figure 5 shows the reduction of output ripple current by 2-phase operation. Not only the ripple amplitude is more than halved, but the ripple frequency is also doubled. Compared with the output voltage ripple for 1-phase:

$$\Delta V_{OUT} \approx \Delta I_{RIPPLE}\left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}}\right)$$

ΔV_{OUT} of 2-phase is less than 50% of that of 1-phase, given the same output capacitor ESRs. Or, to have same ΔV_{OUT} 2-phase only need half the number of output capacitors that are needed in 1-phase.

The output ripple varies with input voltage since ΔI_L is a function of input voltage. The output ripple will be less than ±25mV at max V_{IN} with $\Delta I_L = 0.4 I_{OUT(MAX)}/2$ assuming:

C_{OUT} required ESR < $4(R_{SENSE})$ and

$C_{OUT} > 1/(16f)(R_{SENSE})$

The LTC3735 employs OPTI-LOOP technique to compensate the switching regulator loop with external components (through I_{TH} pin). OPTI-LOOP compensation speeds up regulator's transient response, minimizes output capacitance and effectively removes constraints on output capacitor ESR. It opens a much wider selection of output capacitor types and a variety of capacitor manufactures are available for high current, low voltage switching regulators.

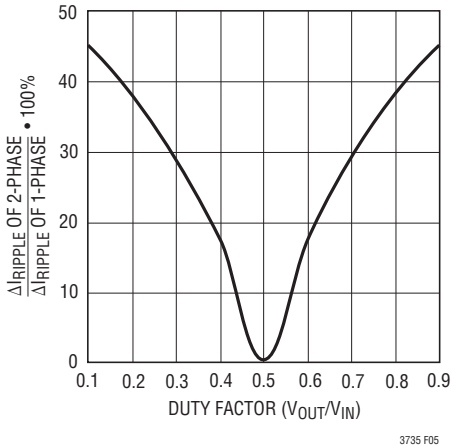


Figure 5. Output Ripple Current Reduction of 2-Phase Over Single Phase

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest (ESR)(size) product of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON type capacitors is recommended to reduce the inductance effects.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer (SP) surface mount capacitors from Panasonic offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent choices are the AVX TPS, AVX TPSV or the KEMET T510 series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, POSCAPs, Kemet AO-CAPs, Nichicon PL series and Sprague 595D series. Consult the manufacturer for other specific recommendations. A combination of capacitors will often result in maximizing performance and minimizing overall cost and size.

PV_{CC} Decoupling

The PV_{CC} pin supplies power to the top and bottom gate drivers and therefore must be bypassed to power ground with a minimum of 4.7µF ceramic or tantalum capacitor. Since the gate driving currents are of high amplitude and high slew rate, this bypassing capacitor should be placed very close to the PV_{CC} and PGND pins to minimize the parasitic inductance. Do NOT apply greater than 7V to the PV_{CC} pin.

The PV_{CC} pin also supplies current to the internal control circuitry of the LTC3735. This supply current is much lower than that of the current for the external MOSFET gate drive. Ceramic capacitors are very good for high frequency filtering and a 0.1µF ~ 1µF ceramic capacitor should be placed adjacent to the PV_{CC} and SGND pins.

APPLICATIONS INFORMATION

Topside MOSFET Driver Supply (C_B, D_B) (Refer to Functional Diagram)

External bootstrap capacitors C_{B1} and C_{B2} connected to the BOOST1 and BOOST2 pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged though diode D_B from PV_{CC} when the SW pin is low. When the topside MOSFET turns on, the driver places the C_B voltage across the gate-source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin rises to V_{IN} + PV_{CC}. The value of the boost capacitor C_B needs to be 30 to 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of D_B must be greater than $PV_{CC(MAX)}$.

VID Output Voltage Programming

After 27µs ~ 71µs t_{BOOT} delay, the output voltage of the regulator is digitally programmed as defined in Table 2 using the VID0 to VID5 logic input pins. The VID logic inputs program a precision, 0.25% internal feedback resistive divider. The LTC3735 has an output voltage range of 0.700V to 1.708V in 16mV steps.

Refering to the Functional Diagram, there is a resistor, R_{VID}, from V_{FB} to ground. The value of R_{VID} is controlled by the six VID input pins. Another internal resistor, 5.33k (R_{ATTEN}), completes the resistive divider. The output voltage is thus set by the ratio of (R_{VID} + 5.33k) to R_{VID}.

Each VID digital pin is a high impedance input. Therefore they must be actively pulled high or pulled low. The logic low threshold of the VID pins is 0.3V; the logic high threshold is 0.7V.

Soft-Start/Run Function

The RUN/SS pin provides three functions: 1) run/shutdown, 2) soft-start and 3) an optional short-circuit latchoff timer. Soft-start reduces the input power sources' surge currents by gradually increasing the controller's current limit. The latchoff timer prevents very short, extreme load transients from tripping the overcurrent latch. A small pull-up current (>5µA) supplied to the RUN/SS pin will prevent the overcurrent latch from operating. The following paragraph describes how the functions operate.

An internal 1.5µA current source charges up the soft-start capacitor, C_{SS}. When the voltage on RUN/SS reaches 1.5V, the controller is permitted to start operating. As the voltage on RUN/SS increases from 1.5V to 3.0V, the internal current limit is increased from 25mV/R_{SENSE} to 72mV/R_{SENSE}. The output current thus ramps up slowly, eliminating the starting surge current required from the input power supply. If RUN/SS has been pulled all the way to ground there is a delay before starting of approximately:

$$t_{DELAY} = \frac{1.5V}{1.5\mu A} C_{SS} = (1s/\mu F) C_{SS}$$

The time for the output current to ramp up is then:

$$t_{IRAMP} = \frac{3V - 1.5V}{1.5\mu A} C_{SS} = (1s/\mu F) C_{SS}$$

By pulling the RUN/SS pin below 1V the LTC3735 is put into low current shutdown (I_Q < 100µA). The RUN/SS pin can be driven directly from logic as shown in Figure 6. Diode D1 in Figure 6 reduces the start delay but allows C_{SS} to ramp up slowly providing the soft-start function. The RUN/SS pin has an internal 6V zener clamp (see Functional Diagram).

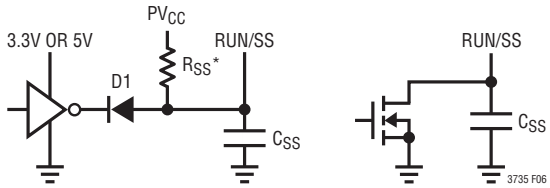


Figure 6. RUN/SS Pin Interfacing

Start-Up Sequence (Refer to the Functional Diagram)

After soft-start, the output voltage of the regulator settles at a voltage level equal to V_{BOOT}.

$$V_{BOOT} = 0.6V \bullet \frac{R2 \bullet (R3 + R5)}{R5 \bullet (R1 + R2)}$$

By using different R5 resistors, V_{BOOT} can be programmed.

APPLICATIONS INFORMATION

Table 2. VID Output Voltage Programming

VID5	VID4	VID3	VID2	VID1	VID0	LTC3735
0	0	0	0	0	0	1.708V
0	0	0	0	0	1	1.692V
0	0	0	0	1	0	1.676V
0	0	0	0	1	1	1.660V
0	0	0	1	0	0	1.644V
0	0	0	1	0	1	1.628V
0	0	0	1	1	0	1.612V
0	0	0	1	1	1	1.596V
0	0	1	0	0	0	1.580V
0	0	1	0	0	1	1.564V
0	0	1	0	1	0	1.548V
0	0	1	0	1	1	1.532V
0	0	1	1	0	0	1.516V
0	0	1	1	0	1	1.500V
0	0	1	1	1	0	1.484V
0	0	1	1	1	1	1.468V
0	1	0	0	0	0	1.452V
0	1	0	0	0	1	1.436V
0	1	0	0	1	0	1.420V
0	1	0	0	1	1	1.404V
0	1	0	1	0	0	1.388V
0	1	0	1	0	1	1.372V
0	1	0	1	1	0	1.356V
0	1	0	1	1	1	1.340V
0	1	1	0	0	0	1.324V
0	1	1	0	0	1	1.308V
0	1	1	0	1	0	1.292V
0	1	1	0	1	1	1.276V
0	1	1	1	0	0	1.260V
0	1	1	1	0	1	1.244V
0	1	1	1	1	0	1.228V
0	1	1	1	1	1	1.212V

VID5	VID4	VID3	VID2	VID1	VID0	LTC3735
1	0	0	0	0	0	1.196V
1	0	0	0	0	1	1.180V
1	0	0	0	1	0	1.164V
1	0	0	0	1	1	1.148V
1	0	0	1	0	0	1.132V
1	0	0	1	0	1	1.116V
1	0	0	1	1	0	1.100V
1	0	0	1	1	1	1.084V
1	0	1	0	0	0	1.068V
1	0	1	0	0	1	1.052V
1	0	1	0	1	0	1.036V
1	0	1	0	1	1	1.020V
1	0	1	1	0	0	1.004V
1	0	1	1	0	1	0.988V
1	0	1	1	1	0	0.972V
1	0	1	1	1	1	0.956V
1	1	0	0	0	0	0.940V
1	1	0	0	0	1	0.924V
1	1	0	0	1	0	0.908V
1	1	0	0	1	1	0.892V
1	1	0	1	0	0	0.876V
1	1	0	1	0	1	0.860V
1	1	0	1	1	0	0.844V
1	1	0	1	1	1	0.828V
1	1	1	0	0	0	0.812V
1	1	1	0	0	1	0.796V
1	1	1	0	1	0	0.780V
1	1	1	0	1	1	0.764V
1	1	1	1	0	0	0.748V
1	1	1	1	0	1	0.732V
1	1	1	1	1	0	0.716V
1	1	1	1	1	1	0.700V

APPLICATIONS INFORMATION

After the output voltage enters the ±10% regulation window centered at V_{BOOT}, the internal power good comparator issues a logic high signal. Refer to the timing diagram in Figure 7. This signal then enters a logic AND gate, with MCH_PG being the other input, and the output of the gate is PG shown in Figure 7. This composite PG signal is then delayed by t_{BOOT} amount of time and then becomes MD. As soon as MD is asserted, the output voltage changes from V_{BOOT} to V_{VID}, a voltage level totally controlled by the six VID bits. In the LTC3735, the time t_{BOOT} is set to be 15 switching cycles:

$$t_{BOOT} = 15\frac{1}{f_S}$$

If f_S is set at 210kHz, t_{BOOT} = 71µs

If f_S is set at 550kHz, t_{BOOT} = 27µs

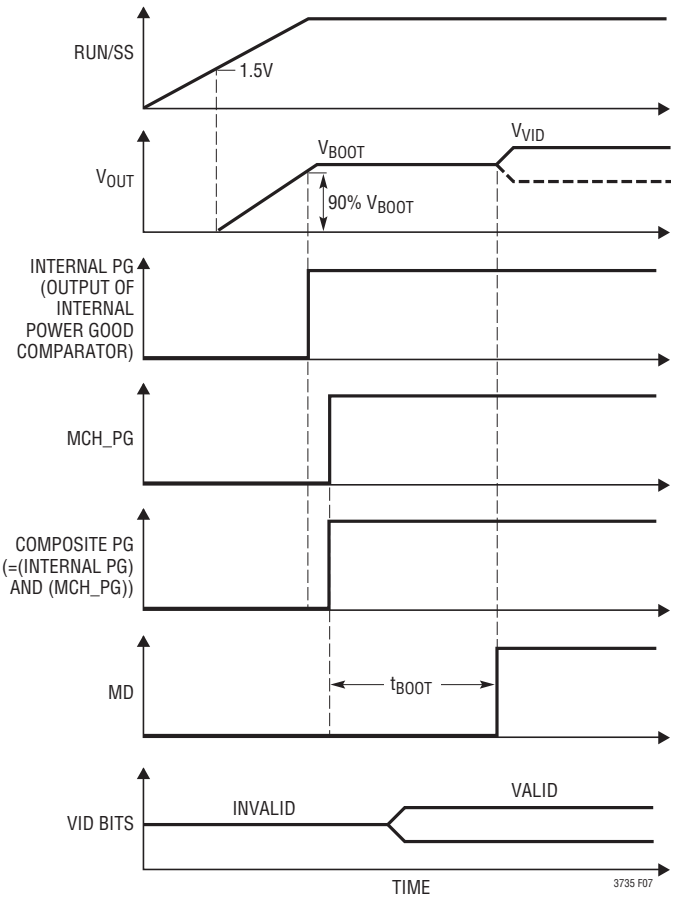


Figure 7. Start-Up Timing Diagram

Output Voltage Set in Deep Sleep and Deeper Sleep States (Refer to the Functional Diagram)

The output voltage can be offset by the STP_CPUB signal. When STP_CPUB becomes low, the output voltage will be a certain percentage lower than that set by the VID bits in Table 2. This state is defined to be the deep sleep state. Referring to the Functional Diagram, we can caluculate the STP_CPUB offset to be:

$$STP\% = -\frac{R3}{R3+R4} \bullet 100\%$$

By using different R4 resistors, STP_CPUB offset can be programmed.

The output voltage could also be set by external resistors R6 and R4 when DPRSLPVR input is high. This state is defined to be the deeper sleep state. The output voltage is set to $V_{DPRSLPVR}$, regardless of the VID setting:

$$V_{DPRSLPVR} = 0.6V \bullet \frac{R2 \bullet (R3 + R6||R4)}{(R6||R4) \bullet (R1+R2)}$$

By using different value R6 resistors, $V_{DPRSLPVR}$ can be programmed.

(The digital input threshold voltage is set to 1.8V for STP_CPUB, DPRSLPVR and MCH_PG inputs.)

Power Good Masking

The PGOOD output monitors V_{OUT}. When V_{OUT} is not within ±10% of the set point, PGOOD is pulled low with an internal MOSFET. When V_{OUT} is within the regulation window, PGOOD is high impedance. PGOOD should be pulled up by an external resistor.

During VID changes, deep sleep and deeper sleep transitions, the output voltage can initially be out of the ±10% window of the newly set regulation point. To avoid nuisance indications from PGOOD, a timer masks PGOOD for 110µs. If V_{OUT} is still out of regulation after this blanking time, PGOOD goes low. Any overvoltage or undervoltage condition is also masked for 110µs before it is reported by PGOOD.

APPLICATIONS INFORMATION

The masking circuitry also adaptively tracks VID and state changes. If a new change in VID or state happens before the 110µs masking timer expires, the timer resets and starts a fresh count of 110µs. This prevents the system from rebooting under frequent output voltage transitions. Refer to Figure 8 for the PGOOD timing diagram.

During start-up, PGOOD is actively pulled low until the RUN/SS pin voltage reaches its arming voltage, which is 4.2V typically, only then is the PGOOD pull-low signal released. When RUN/SS goes low, PGOOD goes low simultaneously.

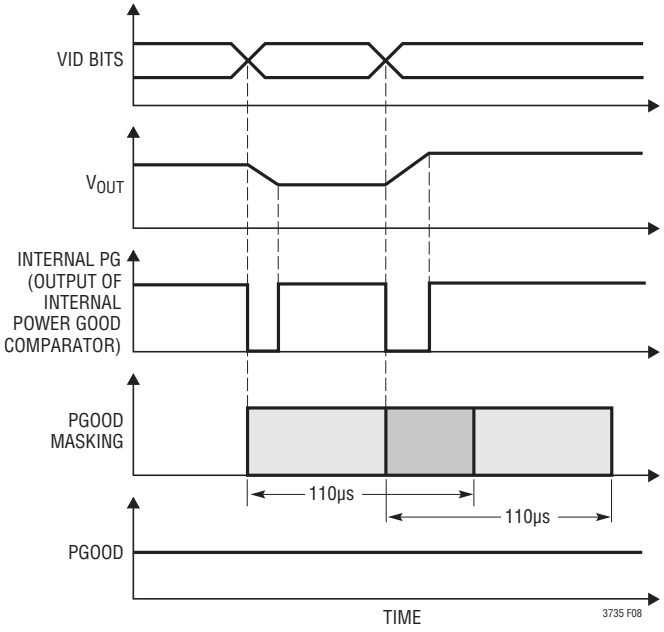


Figure 8. PGOOD Timing Diagram

Fault Conditions: Overcurrent Latchoff

The RUN/SS pin also provides the ability to latch off the controller when an overcurrent condition is detected. The RUN/SS capacitor, C_{SS}, is used initially to limit the inrush current. After the controller has been started and been given adequate time to charge up the output capacitors and provide full load current, the RUN/SS capacitor is used for a short-circuit timer. If the output voltage falls to less than 70% of its nominal value after C_{SS} reaches 4.2V, C_{SS} begins discharging on the assumption that the output is in an overcurrent condition. If the condition lasts for a long enough period as determined by the size of the C_{SS}, the controller will be shut down until the RUN/SS pin voltage is recycled. If the overload occurs during start-up, the time can be approximated by:

$$t_{LO1} \approx (C_{SS} \bullet 0.7V)/(1.5\mu A) = 4.6 \bullet 10^5 (C_{SS})$$

If the overload occurs after start-up, the voltage on C_{SS} will continue charging and will provide additional time before latching off:

$$t_{LO2} \approx (C_{SS} \bullet 2V)/(1.5\mu A) = 1.3 \bullet 10^6 (C_{SS})$$

This built-in overcurrent latchoff can be overridden by providing a pull-up resistor, R_{SS}, to the RUN/SS pin as shown in Figure 6. This resistance shortens the soft-start period and prevents the discharge of the RUN/SS capacitor during a severe overcurrent and/or short-circuit condition. When deriving the 5µA current from PV_{CC} as in the figure, current latchoff is always defeated.

Why should you defeat current latchoff? During the prototyping stage of a design, there may be a problem with noise pickup or poor layout causing the protection circuit to latch off the controller. Defeating this feature allows troubleshooting of the circuit and PC layout. The internal short-circuit and foldback current limiting still remains active, thereby protecting the power supply system from failure. A decision can be made after the design is complete whether to rely solely on foldback current limiting or to enable the latchoff feature by removing the pull-up resistor.

The value of the soft-start capacitor C_{SS} may need to be scaled with output voltage, output capacitance and load current characteristics. The minimum soft-start capacitance is given by:

$$C_{SS} > (C_{OUT})(V_{OUT})(10^{-4})(R_{SENSE})$$

A recommended soft-start capacitor of C_{SS} = 0.1µF will be sufficient for most applications.

APPLICATIONS INFORMATION

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3735 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC3735 will begin to skip cycles resulting in variable frequency operation. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase.

The minimum on-time for the LTC3735 is generally less than 150ns. However, as the peak sense voltage decreases, the minimum on-time gradually increases. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger ripple current and ripple voltage.

If an application can operate close to the minimum on-time limit, an inductor must be chosen that has a low enough inductance to provide sufficient ripple amplitude to meet the minimum on-time requirement. *As a general rule, keep the inductor ripple current of each phase equal to or greater than 15% of $I_{OUT(MAX)}$ at $V_{IN(MAX)}$.*

Active Voltage Positioning

Active voltage positioning can be used to minimize peak-to-peak output voltage excursion under worst-case transient loading conditions. The open-loop DC gain of the control loop is reduced depending upon the maximum load step specifications. Active voltage positioning can easily be added to the LTC3735. Figure 9 shows the equivalent circuit for implementing AVP. The load line slope is estimated to be:

$$AVP \cong -35.5 \bullet \frac{R_{SENSE}}{m} \bullet \frac{R3}{R_{AVP}}, \quad \text{if } g_m \bullet R3 > 10 \bullet \frac{V_{OUT}}{0.6V} \tag{9}$$

where R_{SENSE} is the current sense resistor, m is the number of phases, (m = 2 for LTC3735) R3 and R_{AVP} are defined in Figure 9. g_m is the transconductance gain for the error amplifier, it is about 4.5mmho for LTC3735. Rewriting Equation 9 we can estimate the AVP resistor to be:

$$R_{AVP} \cong \frac{35.5 \bullet R3 \bullet R_{SENSE}}{m \bullet |AVP|} \tag{10}$$

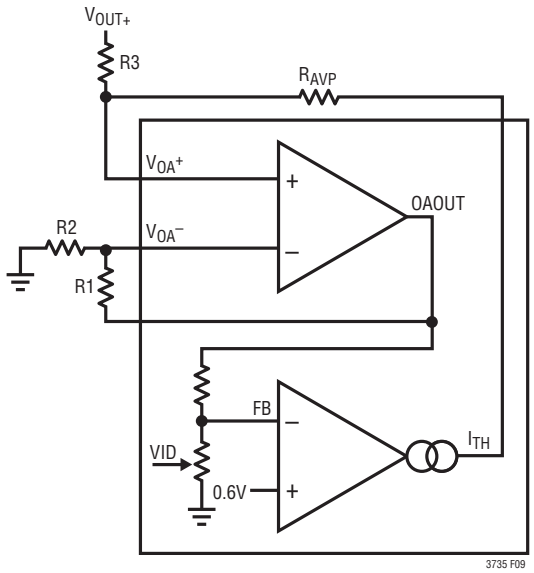


Figure 9. Simplified Schematic Diagram for AVP Design in LTC3735

We also adopt the current sense resistors as part of voltage positioning slopes. So the total load line slope is estimated to be:

$$AVP \cong -35.5 \bullet \frac{R_{SENSE}}{m} \bullet \frac{R3}{R_{AVP}} - \frac{R_{SENSE}}{m}, \quad \text{if } g_m \bullet R3 >> \frac{V_{OUT}}{0.6V} \tag{11}$$

APPLICATIONS INFORMATION

Rewriting this equation, we can estimate the R_{AVP} value to be:

$$R_{AVP} \cong \frac{35.5 \bullet R3}{\frac{m \bullet |AVP|}{R_{SENSE}} - 1} \quad (12)$$

Typically the calculation results based on these equations have ±10% tolerance. So the resistor values need to be fine tuned.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3735 circuits: 1) I^2R losses, 2) Topside MOSFET transition losses, 3) PV_{CC} supply current and 4) C_{IN} loss.

1) I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, and current sense resistor. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 10mΩ, R_L = 10mΩ, and R_{SENSE} = 5mΩ, then the total resistance is 25mΩ. This results in losses ranging from 2% to 8% as the output current increases from 3A to 15A per output stage for a 5V output, or a 3% to 12% loss per output stage for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

2) Transition losses apply only to the topside MOSFET(s), and are significant only when operating at high input voltages (typically 12V or greater). Transition losses can be estimated from:

$$\text{Transition Loss per Phase} = \frac{V_{IN}^2 \bullet I_{OUT}}{4} \bullet f \bullet C_{RSS} \bullet R_{DR} \bullet \left(\frac{1}{V_{DR} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}} \right)$$

3) PV_{CC} drives both top and bottom MOSFETs. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from PV_{CC} to ground. The resulting dQ/dt is a current out of PV_{CC} that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = (Q_T + Q_B)f$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs and f is the switching frequency.

4) The input capacitor has the difficult job of filtering the large RMS input current to the regulator. It must have a very low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries. The LTC3735 2-phase architecture typically halves the input and output capacitor requirements over 1-phase solutions.

Other losses, including C_{OUT} ESR loss, Schottky diode conduction loss during dead time, inductor core loss and internal control circuitry supply current generally account for less than 2% additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive)

APPLICATIONS INFORMATION

load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD}(ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. *The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time, and settling at this test point truly reflects the closed loop response.* Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in the Figure 1 circuit will provide an adequate starting point for most applications.

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.2 to 5 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be decided upon first because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of <1µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

Automotive Considerations: Plugging into the Cigarette Lighter

As battery-powered devices go mobile, there is a natural interest in plugging into the cigarette lighter in order to conserve or even recharge battery packs during operation. But before you connect, be advised: you are plugging into the supply from hell. The main battery line in an automobile is the source of a number of nasty potential transients, including load-dump, reverse-battery and double-battery.

Load-dump is the result of a loose battery cable. When the cable breaks connection, the field collapse in the alternator can cause a positive spike as high as 60V which takes several hundred milliseconds to decay. Reverse-battery is just what it says, while double-battery is a consequence of tow truck operators finding that a 24V jump start cranks cold engines faster than 12V.

The network shown in Figure 10 is the most straightforward approach to protect a DC/DC converter from the ravages of an automotive power line. The series diode prevents current from flowing during reverse-battery, while the transient suppressor clamps the input voltage during load-dump. Note that the transient suppressor should not conduct during double-battery operation, but must still clamp the input voltage below breakdown of the converter. Although the LT3735 has a maximum input voltage of 32V, most applications will be limited to 30V by the MOSFET BV_{DSS}.

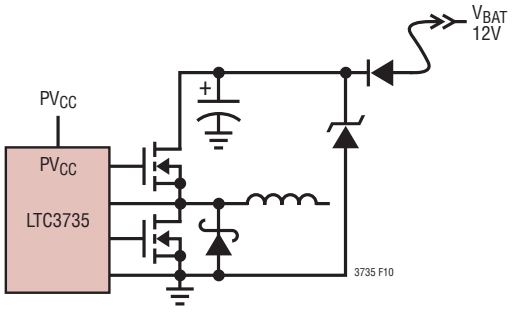


Figure 10. Automotive Application Protection

APPLICATIONS INFORMATION

Design Example

As a design example, assume V_{IN} = 12V (nominal), V_{IN} = 21V (max), V_{OUT} = 1.5V, I_{MAX} = 35A, and f = 350kHz (each phase).

The inductance value is chosen first based on a 40% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. The minimum inductance for 40% ripple current is:

$$L \geq \frac{V_{OUT}}{f \bullet \Delta I} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right) = \frac{1.5V}{350kHz \bullet (40\% \bullet 17.5A)} \bullet \left(1 - \frac{1.5V}{21V}\right) = 0.57\mu H$$

Using L = 0.6µH, a common "off-the-shelf" value results in 38%ripple current. The peak inductor current will be the maximum DC current plus one half of the ripple current, or 21A.

Tie the FREQSET pin to 1.2V, resistively divided down from PV_{CC} to have 350kHz operation for each phase.

The minimum on-time also occurs at maximum input voltage:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN} \bullet f} = \frac{1.5V}{21V \bullet 350kHz} = 204ns$$

which is larger than 150ns, the typical minimum on time of the LTC3735.

R_{SENSE1} and R_{SENSE2} can be calculated by using a conservative maximum sense voltage threshold of 40mV and taking into account of the peak current:

$$R_{SENSE} = \frac{40mV}{21A} = 0.002\Omega$$

The power loss dissipated by the top MOSFET can be calculated with equations 3 and 7. Using a Fairchild FDS7760 as an example: $R_{DS(ON)}$ = 8mΩ, Q_G = 55nC at 5V V_{GS}, C_{RSS} = 307pF, $V_{TH(MIN)}$ = 1V. At maximum input voltage with T_J(estimated) = 85°C at an elevated ambient temperature:

$$P_{TOP} = \frac{1.5V}{21V} \bullet \left(\frac{35A}{2}\right)^2 \bullet (1 + 0.005 \bullet (85°C - 25°C)) \bullet 0.008\Omega + \frac{21V^2 \bullet 17.5A}{2} \bullet 350kHz \bullet 307pF \bullet 2\Omega \bullet \left(\frac{1}{5V - 1V} + \frac{1}{1V}\right) = 1.26W$$

Equation 4 gives the worst-case power loss dissipated by the bottom MOSFET (assuming FDS7760 and T_J = 85°C again):

$$P_{BOT} = \frac{21V - 1.5V}{21V} \bullet \left(\frac{35A}{2}\right)^2 \bullet (1 + 0.005 \bullet (85°C - 25°C)) \bullet 0.008\Omega = 2.95W$$

Therefore it is necessary to have two FDS7760s in parallel to split the power loss.

A short-circuit to ground will result in a folded back current of about:

$$I_{SC} = \frac{25mV}{0.002\Omega} + \frac{1}{2} \bullet \left(\frac{200ns \bullet 21V}{0.6\mu H}\right) = 16A$$

The worst-case power dissipation by the bottom MOSFET under short-circuit conditions is:

$$P_{BOT} = \frac{\frac{1}{350kHz} - 200ns}{\frac{1}{350kHz}} \bullet (16A)^2 \bullet (1 + 0.005 \bullet (85°C - 25°C)) \bullet 0.008\Omega = 2.48W$$

which is less than normal, full load conditions.

The nominal duty cycle of this application is equation 1:

$$DC = \frac{1.5V}{12V} = 12.5\%$$

APPLICATIONS INFORMATION

Using Figure 4, the RMS input ripple current will be:

$$I_{INRMS} = 35A \bullet 0.22 = 7.7A$$

An input capacitor(s) with a 8A RMS current rating is required.

The output capacitor ripple current is calculated by using the inductor ripple current and multiplying by the factor obtained from Figure 3. The output ripple will be highest at the maximum input voltage since the duty cycle is less than 50%. The maximum output current ripple is:

$$\Delta I_{OUT(MAX)} = \frac{1.5V}{350kHz \bullet 0.6\mu H} \bullet 0.77 = 5.5A_{P-P}$$

Assuming the ESR of output capacitor(s) is 5mΩ, the output ripple voltage is:

$$\Delta V_{OUT} \approx 5.5A_{P-P}\left(5m\Omega + \frac{1}{16 \bullet 350kHz \bullet (4 \bullet 270\mu F)}\right)$$

$$= 28.4mV_{P-P}$$

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3735. Check the following in your layout:

1) Are the signal and power grounds segregated? Keep the SGND at one end of a PC board to prevent MOSFET currents from traveling under the IC. The IC signal ground pin should be used to hook up all control circuitry on one side of the IC, routing the copper through SGND, under the IC covering the "shadow" of the package, connecting to the PGND pin and then continuing on to the (–) plate of C_{OUT}.

2) Is the PV_{CC} decoupling capacitor connected immediately adjacent to the PV_{CC} and PGND pins? A 1µF ceramic capacitor of the X7R or X5R material is small enough to fit very close to the IC to minimize the ill effects of the large current pulses drawn to drive the power MOSFETs. An additional 4.7µF ~ 10µF of ceramic, tantalum or other low ESR capacitor is recommended in order to keep PV_{CC} stable. The power ground returns to the sources of the bottom N-channel MOSFETs, anodes of the Schottky diodes, and (–) plates of C_{IN}, which should have the shortest trace length possible.

3) Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitors between $SENSE^+$ and $SENSE^-$ pin pairs should be as close as possible to the LTC3735. Ensure accurate current sensing with Kelvin connections at the current sense resistor. See Figure 11.

4) Does the (+) plate of C_{IN} connect to the drains of the topside MOSFETs as closely as possible? This capacitor provides the AC current to the MOSFETs. Keep the input current path formed by the input capacitor, top and bottom MOSFETs, and the Schottky diode on the same side of the PC board in a tight loop to minimize conducted and radiated EMI.

5) Keep the "noisy" nodes, SW, BOOST, TG and BG away from sensitive small-signal nodes. Ideally the switch nodes should be placed at the furthest point from the LTC3735.

The diagram in Figure 12 illustrates all branch currents in a 2-phase switching regulator. It becomes very clear after studying the current waveforms why it is critical to keep the high-switching-current paths to a small physical size. High electric and magnetic fields will radiate from these "loops" just as radio stations transmit signals. The output capacitor ground should return to the negative terminal of the input capacitor and not share a common ground path with any switched current paths. The left half of the circuit gives rise to the "noise" generated by a switching regulator.

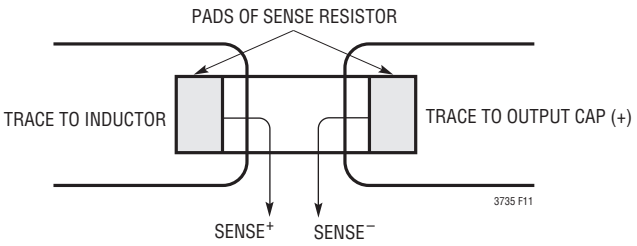


Figure 11. Proper Current Sense Connections

APPLICATIONS INFORMATION

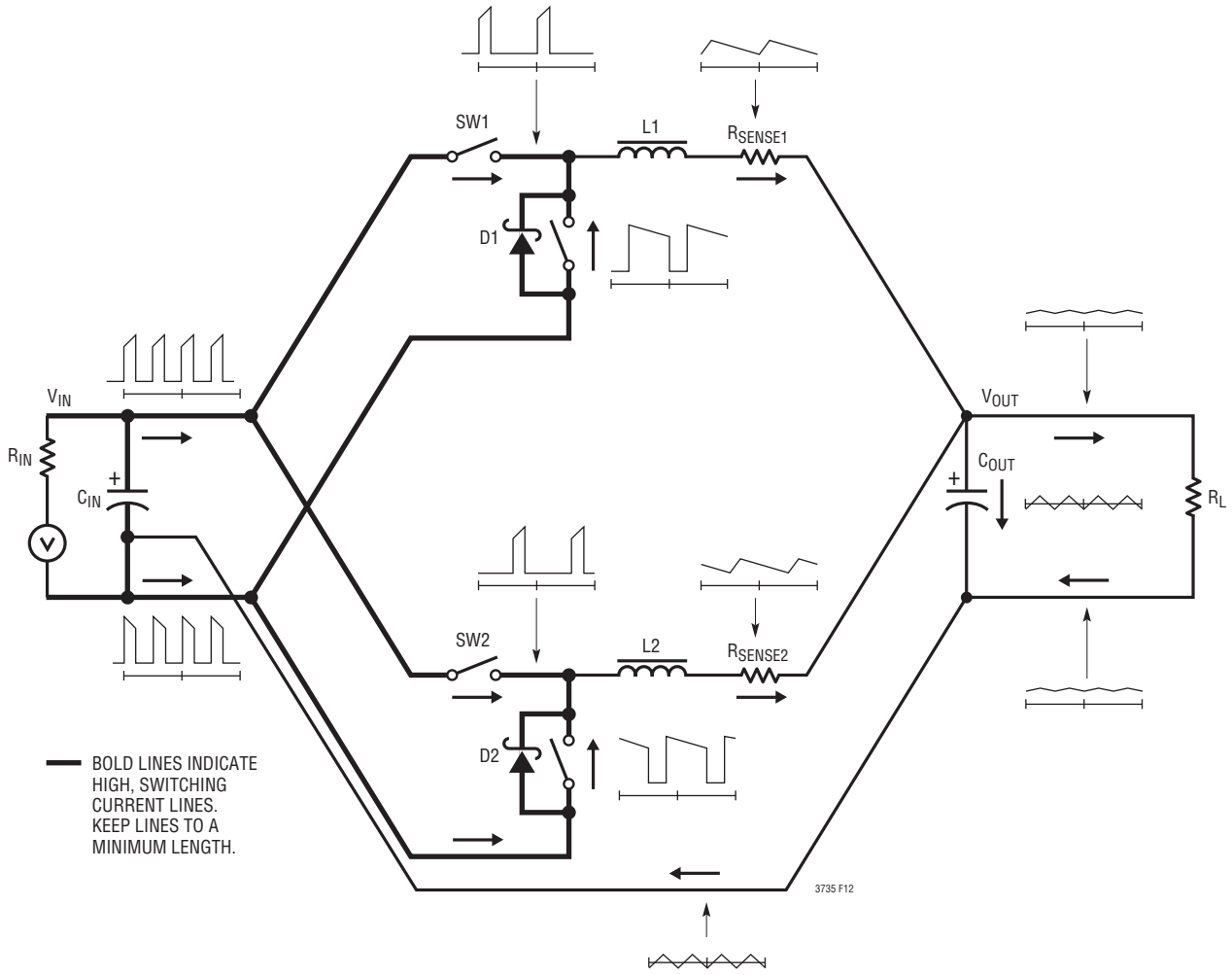


Figure 12. Instantaneous Current Path Flow in a Multiple Phase Switching Regulator

The ground terminations of the sychronous MOSFETs and Schottky diodes should return to the negative plate(s) of the input capacitor(s) with a short isolated PC trace since very high switched currents are present. A separate isolated path from the negative plate(s) of the input capacitor(s) should be used to tie in the IC power ground pin (PGND) and the signal ground pin (SGND). This technique keeps inherent signals generated by high current pulses from taking alternate current paths that have finite impedances during the total period of the switching regulator. External OPTI-LOOP compensation allows overcompensation for PC layouts which are not optimized but this is not the recommended design procedure.

Simplified Visual Explanation of How a 2-Phase Controller Reduces Both Input and Output RMS Ripple Current

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is divided by, and the effective ripple frequency is multiplied up by the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by, and the effective ripple frequency is increased by the number of phases used. Figure 13 graphically illustrates the principle.

APPLICATIONS INFORMATION

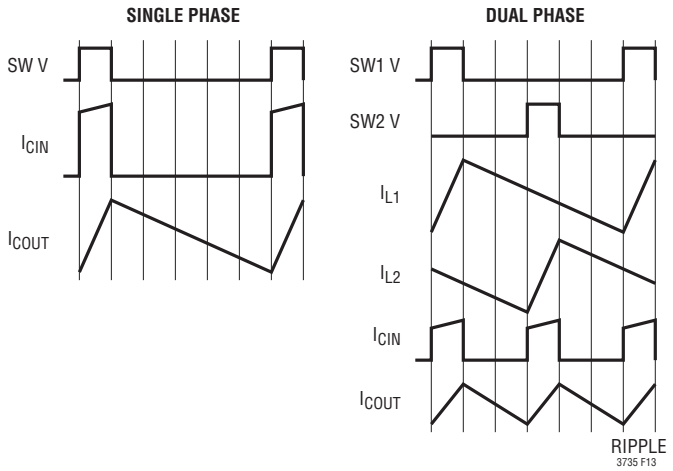


Figure 13. Single and 2-Phase Current Waveforms

The worst-case RMS ripple current for a single stage design peaks at an input voltage of twice the output voltage. The worst-case RMS ripple current for a two stage design results in peak outputs of 1/4 and 3/4 of input voltage. When the RMS current is calculated, higher effective duty factor results and the peak current levels are divided as long as the currents in each stage are balanced. Refer to Linear Technology Application Note 19 for a detailed description of how to calculate RMS current for the single stage switching regulator. Figures 3 and 4 illustrate how the input and output currents are reduced by using an additional phase. The input current peaks drop in half and the frequency is doubled for this 2-phase converter. The input capacity requirement is thus reduced theoretically by a factor of four! Ceramic input capacitors with their low ESR characteristics can be used.

Figure 4 illustrates the RMS input current drawn from the input capacitance vs the duty cycle as determined by the ratio of input and output voltage. The peak input RMS current level of the single phase system is reduced by 50% in a 2-phase solution due to the current splitting between the two stages.

An interesting result of the 2-phase solution is that the V_{IN} which produces worst-case ripple current for the input capacitor, $V_{OUT} = V_{IN}/2$, in the single phase design produces zero input current ripple in the 2-phase design.

The output ripple current is reduced significantly when compared to the single phase solution using the same inductance value because the V_{OUT}/L discharge current term from the stage that has its bottom MOSFET on subtracts current from the $(V_{IN} – V_{OUT})/L$ charging current resulting from the stage which has its top MOSFET on. The output ripple current is:

$$\Delta I_{RIPPLE} = \frac{2V_{OUT}}{fL}\left[\frac{|1-2D|(1-D)}{|1-2D|+1}\right]$$

where D is duty factor.

The input and output ripple frequency is increased by the number of stages used, reducing the output capacity requirements. When V_{IN} is approximately equal to $2(V_{OUT})$ as illustrated in Figures 3 and 4, very low input and output ripple currents result.

TYPICAL APPLICATION

Figure 14 shows a typical application using the LTC3735 to power the mobile CPU core. The input can vary from 5V to 24V; the output voltage can be programmed from 0.7V to 1.708V with a maximum current of 32A. By only modifying the external MOSFET and inductor selection, higher load current capability (up to 40A) can be achieved.

The power supply in Figure 14 receives a VRON signal for ON/OFF control. After soft-start, the output voltage is set at 1.2V until the assertion of the MCH_PG signal. After about a 50µs delay, the VID5-VID0 bits gain the control over the output voltage and program it between 0.7V and 1.708V. When the STP_CPUB signal is low, a deep sleep state is indicated and the output voltage is decreased by about 1.04%. When the DPRSLPVR signal is high, a deeper sleep state is indicated and the output voltage becomes 0.748V regardless of the states of the VID bits. Active voltage positioning is accomplished with a resistor from the I_{TH} to the V_{OA}^+ pin. Lower resistance yields a steeper AVP slope while higher resistance provides a flatter slope. Finally, the PGOOD output is masked for 110µs during VID change or state transition.

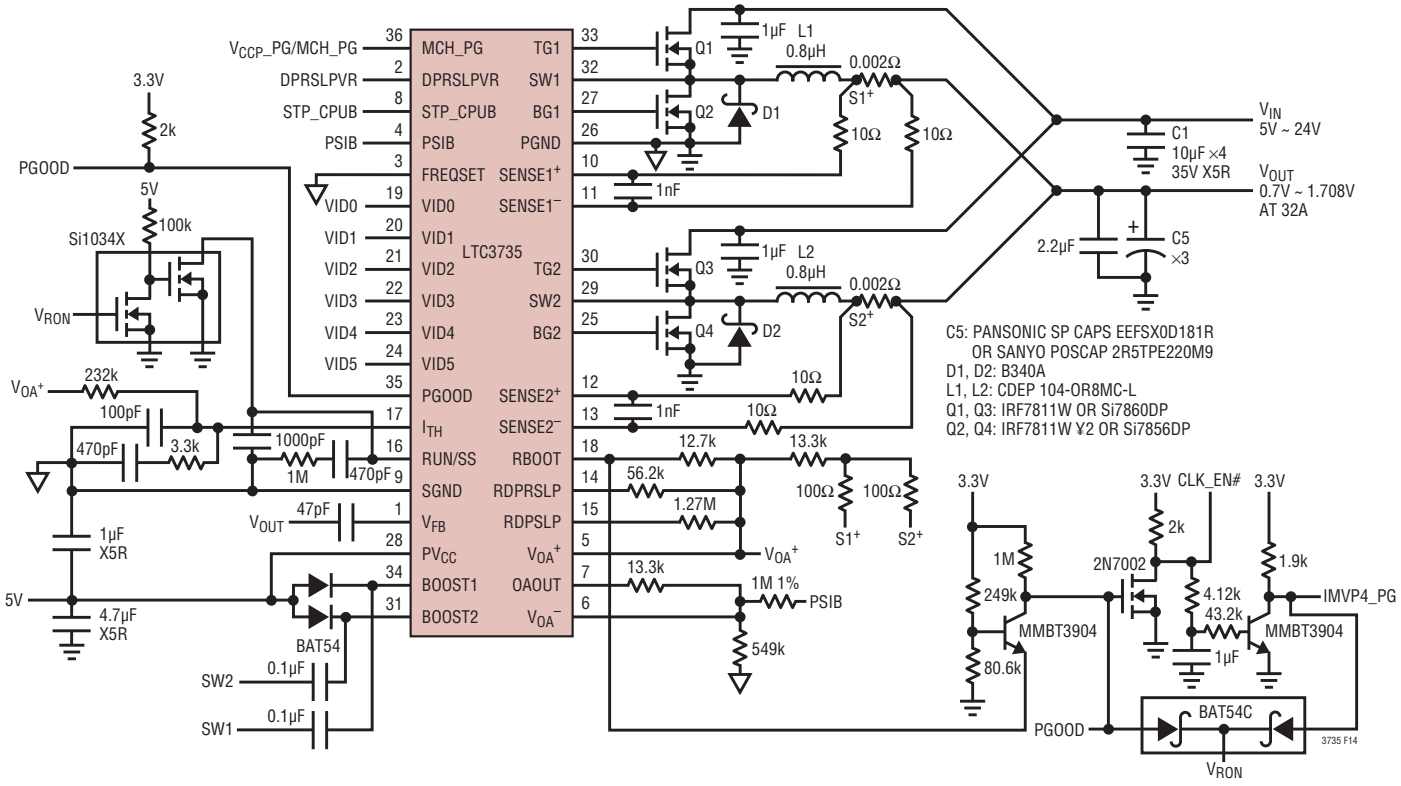
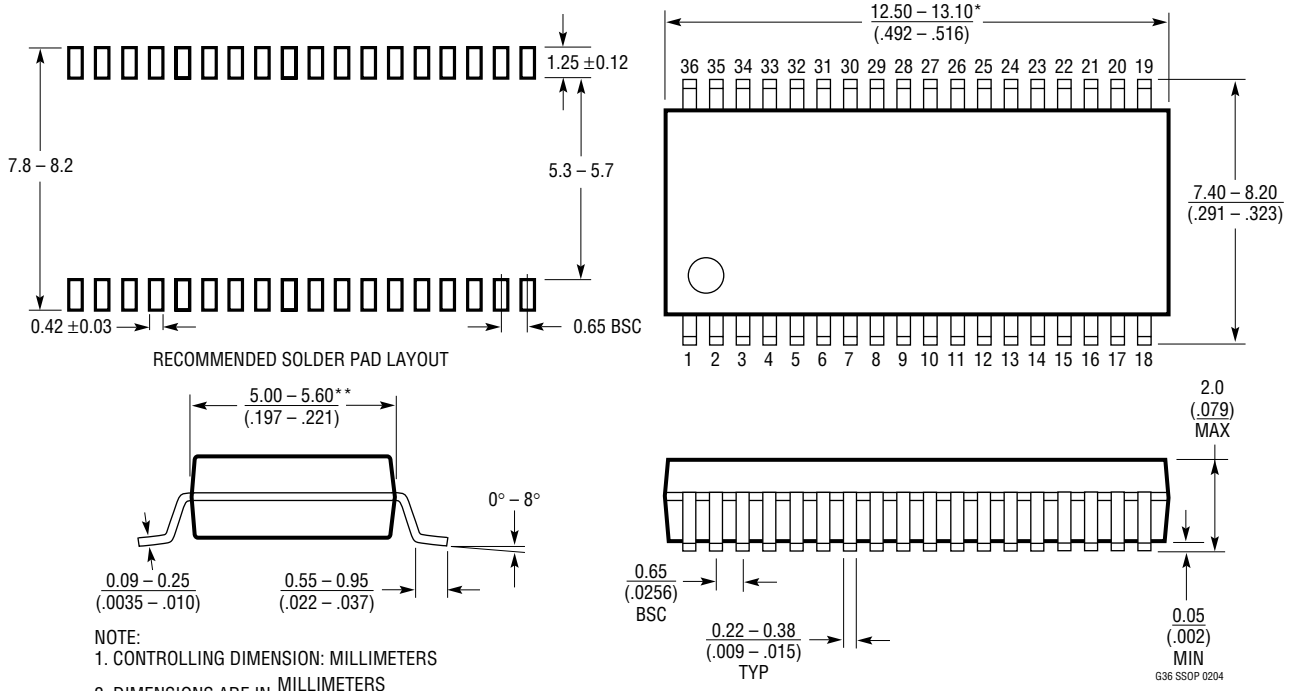


Figure 14. 5V to 24V Input, 0.7V to 1.708V Output, 32A IMVP-IV Compatible Power Supply

PACKAGE DESCRIPTION

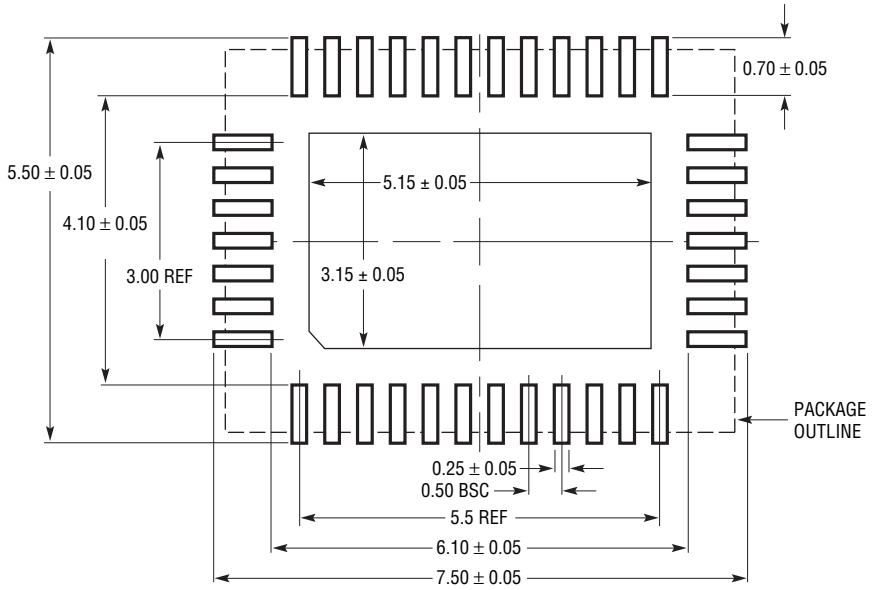
G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



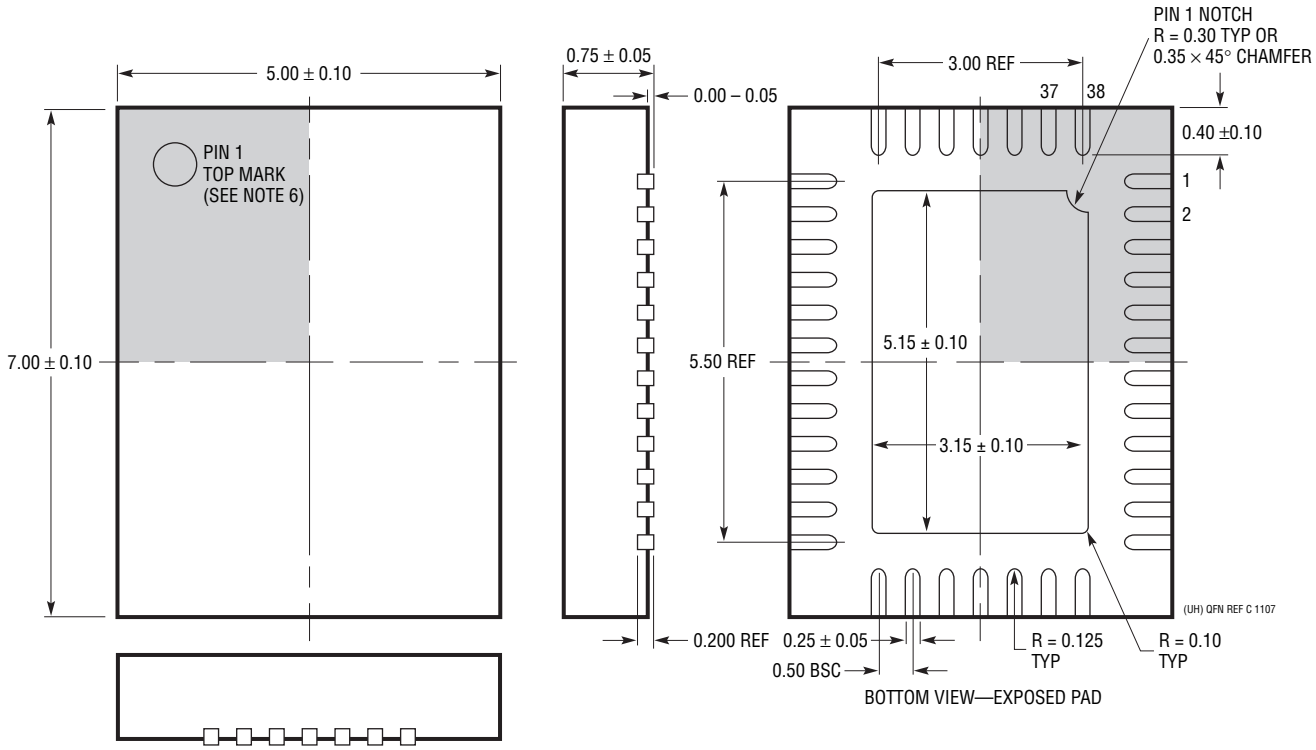
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

PACKAGE DESCRIPTION

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701 Rev C)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	4/11	Updated Figure 14	28
		Updated Related Parts	32

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3816	Single Phase DC/DC Controller for Intel IMVP-6/6+/6.5 CPUs	7-Bit IMVP-6 VID: 0.00V ≤ V_{OUT} ≤ 1.50V, 4.5V ≤ V_{IN} ≤ 36V, Very Low Duty Cycle Capable
LTC3732	3-Phase, 5-Bit VID, 600kHz, Synchronous Controller	5-Bit VRM 9/9.1: 1.10V ≤ V_{OUT} ≤ 1.85V
LTC3734	Single Phase DC/DC Controller for IMVP-4	6-Bit IMVP-4 VID: 0.70V ≤ V_{OUT} ≤ 1.708V, 4.5V ≤ V_{IN} ≤ 30V, Lossless Voltage Positioning
LTC3869/LTC3869-2	Dual, 2-Phase Synchronous Step-Down DC/DC Controllers with Excellent Current Share when Paralleled	Phase-Lockable Fixed 250kHz to 780kHz Frequency, 4V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 12.5V
LTC3856	2-Phase, Single Output Synchronous Step-Down DC/DC Controller with Diff Amp and DCR Temperature Compensation	Phase-Lockable Fixed 250kHz to 770kHz Frequency, 4.5V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 5V
LTC3850/LTC3850-1 LTC3850-2	Dual 2-Phase, High Efficiency Synchronous Step-Down DC/DC Controller, R_{SENSE} or DCR Current Sensing and Tracking	Phase-Lockable Fixed 250kHz to 780kHz Frequency, 4V ≤ V_{IN} ≤ 30V, 0.8V ≤ V_{OUT} ≤ 5.25V
LTC3860	Dual, Multiphase, Synchronous Step-Down DC/DC Controller with Diff Amp and Three-State Output Drive	Operates with Power Blocks, DRMOS Devices or External Drivers/MOSFETs, 3V ≤ V_{IN} ≤ 24V, $t_{ON(MIN)}$ = 20ns
LTC3855	Dual, Multiphase, Synchronous Step-Down DC/DC Controller with Diff Amp and DCR Temperature Compensation	Phase-Lockable Fixed Frequency 250kHz to 770kHz, 4.5V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 12V
LTC3829	3-Phase, Single Output Synchronous Step-Down Controller with Diff Amp and DCR Temperature Compensation	Phase-Lockable Fixed 250kHz to 770kHz Frequency, 4.5V ≤ V_{IN} ≤ 38V, 0.8V≤ V_{OUT} ≤ 5V
LTC3853	Triple Output, Multiphase Synchronous Step-Down DC/DC Controller, R_{SENSE} or DCR Current Sensing and Tracking	Phase-Lockable Fixed 250kHz to 750kHz Frequency, 4V ≤ V_{IN} ≤ 24V, V_{OUT3} Up to 13.5V

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