InvenSense

ADMP441

Omnidirectional Microphone with Bottom Port and I²S Digital Output

GENERAL DESCRIPTION

The ADMP441 is a high-performance, low power, digital-output, omnidirectional MEMS microphone with a bottom port. The complete ADMP441 solution consists of a MEMS sensor, signal conditioning, an analog-to-digital converter, anti-aliasing filters, power management, and an industry-standard 24-bit I²S interface. The I²S interface allows the ADMP441 to connect directly to digital processors, such as DSPs and microcontrollers, without the need for an audio codec in the system.

The ADMP441 has a high SNR, making it an excellent choice for near field applications. The ADMP441 has a flat wideband frequency response, resulting in natural sound with high intelligibility.

The ADMP441 is available in a thin 4.72 × 3.76 × 1 mm surface-mount package. It is reflow- solder compatible with no sensitivity degradation. The ADMP441 is halide free.

**Protected by U.S. Patents 7,449,356; 7,825,484; 7,885,423; and 7,961,897. Other patents are pending.*

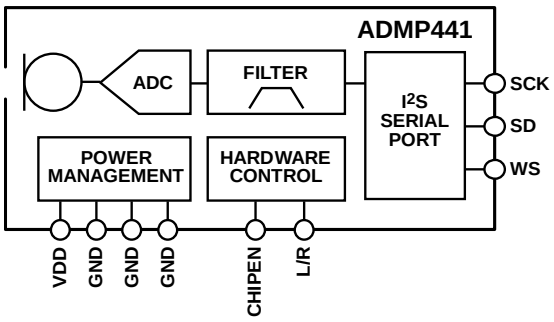
APPLICATIONS

- Teleconferencing Systems
- Remote Controls
- Gaming Consoles
- Mobile Devices
- Laptops
- Tablets
- Security Systems

FEATURES

- Digital I²S Interface with High-Precision 24-Bit Data
- High SNR of 61 dBA
- High Sensitivity of -26 dBFS
- Flat Frequency Response from 60 Hz to 15 kHz
- Low Current Consumption of 1.4 mA
- High PSR of -75 dBFS
- Small 4.72 × 3.76 × 1 mm Surface-Mount Package
- Compatible with Sn/Pb and Pb-Free Solder Processes
- RoHS/WEEE Compliant

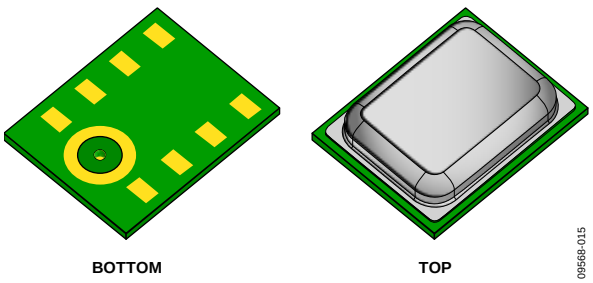
FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
ADMP441ACEZ-RL	−40°C to +85°C*	CE-9-1
ADMP441ACEZ-RL7	−40°C to +85°C†	CE-9-1
EVAL-ADMP441Z	—	—
EVAL-ADMP441Z-FLEX	—	—

* – 13” Tape and Reel † – 7” Tape and Reel



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SPECIFICATIONS

TABLE 1. ELECTRICAL CHARACTERISTICS

(T_A = −40 to 85°C, V_{DD} = 1.8 to 3.3 V, CLK = 2.4 MHz, C_{LOAD} = 30 pF, unless otherwise noted. All minimum and maximum specifications are guaranteed across temperature, voltage, and clock frequency specified in Table 1, Table 2, Table 3, unless otherwise noted. Typical specifications are not guaranteed.)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
PERFORMANCE							
Directionality				Omni			
Sensitivity		1 kHz, 94 dB SPL	−29	−26	−23	dBFS	1
Signal-to-Noise Ratio (SNR)		20 Hz to 20 kHz, A-weighted		61		dBA	
Equivalent Input Noise (EIN)		20 Hz to 20 kHz, A-weighted		33		dBA SPL	
Dynamic Range		Derived from EIN and maximum acoustic input		87		dB	
Frequency Response		Low frequency −3 dB point		60		Hz	2
		High frequency −3 dB point		15		kHz	
Total Harmonic Distortion (THD)		105 dB SPL			3	%	
Power-Supply Rejection (PSR)		217 Hz, 100 mVp-p square wave superimposed on V_{DD} = 1.8 V		−75		dBFS	
Maximum Acoustic Input		Peak		120		dB SPL	
Noise Floor		20 Hz to 20 kHz, A-weighted, RMS		−87		dBFS	
POWER SUPPLY							
Supply Voltage (V_{DD})			1.62		3.63	V	
Supply Current (I_S)							
V_{DD} = 1.8 V	Normal Mode			1.4	1.6	mA	
	Standby				0.8	mA	
	Power Down				2	µA	
V_{DD} = 3.3 V	Normal Mode			2.2	2.5	mA	
	Standby				0.8	mA	
	Power Down				4.5	µA	
DIGITAL FILTER							
Group Delay					17.2/fS	sec	
		f_S = 48 kHz			359	µs	
		f_S = 16 kHz			1078	µs	
Pass-Band Ripple					±0.04	dB	
Stop-Band Attenuation				60		dB	
Pass Band		0.423 × f_S		20.3		kHz	

Note 1: The peak-to-peak amplitude relative to peak-to-peak amplitude of (2^{24} − 1.) The stimulus is a 104 dB SPL sinusoid having RMS amplitude of 3.1623 Pa. Sensitivity is relative to 1 Pa.

Note 2: See Figure 4 and Figure 5

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TABLE 2. I²S DIGITAL INPUT/OUTPUT CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
DIGITAL INPUT						
Input Voltage High (V_{IH})	L/R, WS, SCK	0.7 x V_{DD}		V_{DD}	V	1
Input Voltage Low (V_{IL})	L/R, WS, SCK	0		0.25 x V_{DD}	V	1
SD DIGITAL INPUT						
Voltage Output Low (VOL)	VDD = 1.8 V, I_{SINK} = 0.25 mA			0.1 × V_{DD}	V	1
Voltage Output Low (VOL)	VDD = 1.8 V, I_{SINK} = 0.7 mA			0.3 × V_{DD}	V	1
Voltage Output High (VOH)	VDD = 1.8 V, I_{SINK} = 0.7 mA	0.7 × V_{DD}			V	1
Voltage Output High (VOH)	VDD = 1.8 V, I_{SINK} = 0.25 mA	0.9 × V_{DD}			V	1
Voltage Output Low (VOL)	VDD = 3.3 V, I_{SINK} = 0.5 mA			0.1 × V_{DD}	V	1
Voltage Output Low (VOL)	VDD = 3.3 V, $_{ISINK}$ = 1.7 mA			0.3 × V_{DD}	V	1
Voltage Output High (VOH)	VDD = 3.3 V, I_{SINK} = 1.7 mA	0.7 × V_{DD}			V	1
Voltage Output High (VOH)	VDD = 3.3 V, I_{SINK} = 0.5 mA	0.9 × V_{DD}			V	1

Note 1: Limits based on characterization results; not production tested..

TABLE 3. SERIAL DATA PORT TIMING SPECIFICATIONS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
t_{SCH}	SCK high	50			ns	
t_{SCL}	SCK low	50			ns	
t_{SCP}	SCK period	312			ns	
f_{SCK}	SCK frequency	0.5		3.2	MHz	
t_{WSS}	WS setup	0			ns	
t_{WSH}	WS hold	20			ns	
f_{WS}	WS frequency	7.8		50	kHz	

TIMING DIAGRAM

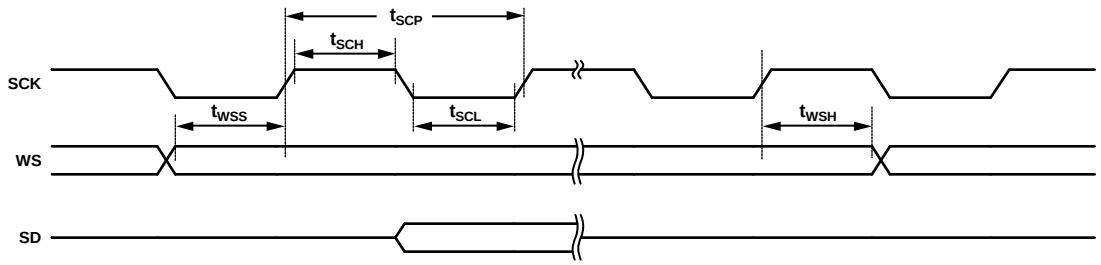

Figure 1. Serial Data Port Timing

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ABSOLUTE MAXIMUM RATINGS

Stress above those listed as Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

TABLE 4. ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Supply Voltage (V_{DD})	−0.3 V to +3.63 V
Digital Pin Input Voltage	−0.3 V to V_{DD} + 0.3 V or 3.63 V, whichever is less
Sound Pressure Level	160 dB
Mechanical Shock	10,000 *g*
Vibration	Per MIL-STD-883 Method 2007, Test Condition B
Temperature Range	
Biased	−40°C to +85°C
Storage	−55°C to +150°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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SOLDERING PROFILE

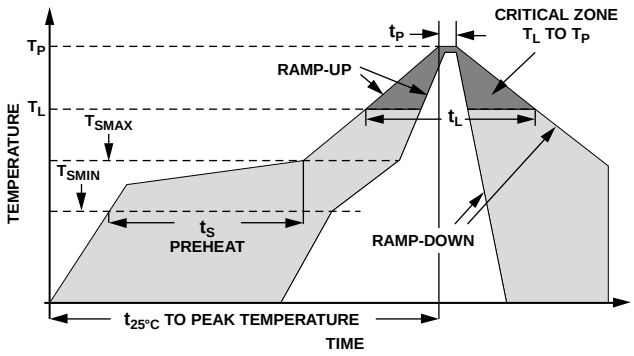

Figure 2. Recommended Soldering Profile Limits

TABLE 5. RECOMMENDED SOLDERING PROFILE

PROFILE FEATURE		Sn63/Pb37	Pb-Free
Average Ramp Rate (T_L to T_P)		1.25°C/sec max	1.25°C/sec max
Preheat	Minimum Temperature (T_{SMIN})	100°C	100°C
	Minimum Temperature (T_{SMIN})	150°C	200°C
	Time (T_{SMIN} to T_{SMAX}), t_S	60 sec to 75 sec	60 sec to 75 sec
Ramp-Up Rate (T_{SMAX} to T_L)		1.25°C/sec	1.25°C/sec
Time Maintained Above Liquidous (t_L)		45 sec to 75 sec	~50 sec
Liquidous Temperature (T_L)		183°C	217°C
Peak Temperature (T_P)		215°C +3°C/−3°C	260°C +0°C/−5°C
Time Within +5°C of Actual Peak Temperature (t_P)		20 sec to 30 sec	20 sec to 30 sec
Ramp-Down Rate		3°C/sec max	3°C/sec max
Time +25°C ($t_{25°C}$) to Peak Temperature		5 min max	5 min max

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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

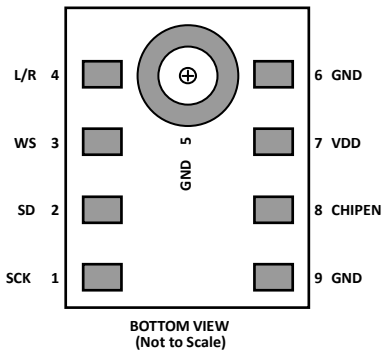

Figure 3. Pin Configuration

TABLE 6. PIN FUNCTION DESCRIPTIONS

PIN	NAME	FUNCTION
1	SCK	Serial-Data Clock for I²S Interface
2	SD	Serial-Data Output for I²S Interface. This pin tri-states when not actively driving the appropriate output channel. The SD trace should have a 100 kΩ pulldown resistor to discharge the line during the time that all microphones on the bus have tri-stated their outputs.
3	WS	Serial Data-Word Select for I²S Interface
4	L/R	Left/Right Channel Select. When set low, the microphone outputs its signal in the left channel of the I²S frame. When set high, the microphone outputs its signal in the right channel.
5	GND	Ground. Connect to ground on the PCB.
6	GND	Ground. Connect to ground on the PCB.
7	VDD	Power, 1.8 V to 3.3 V. This pin should be decoupled to Pin 6 with a 0.1 µF capacitor.
8	CHIPEN	Microphone Enable. When set low (ground), the microphone is disabled and put in power-down mode. When set high (VDD), the microphone is enabled.
9	GND	Ground. Connect to ground on the PCB.

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TYPICAL PERFORMANCE CHARACTERISTICS

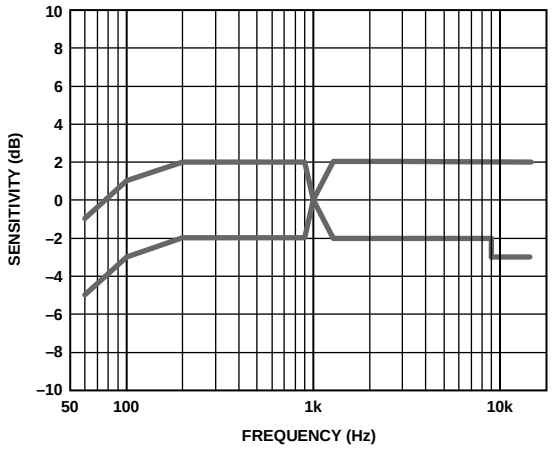

Figure 4. Frequency Response Mask

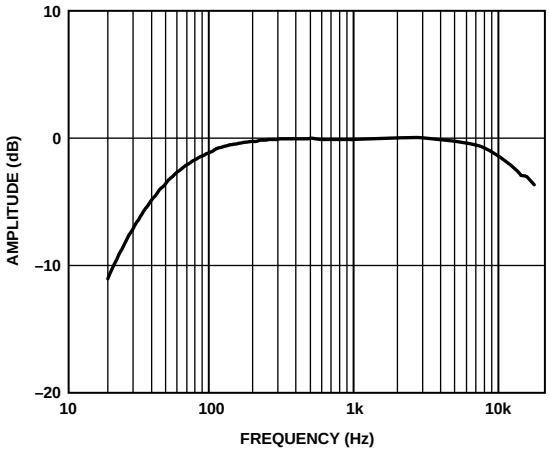

Figure 5. Typical Frequency Response (Measured)

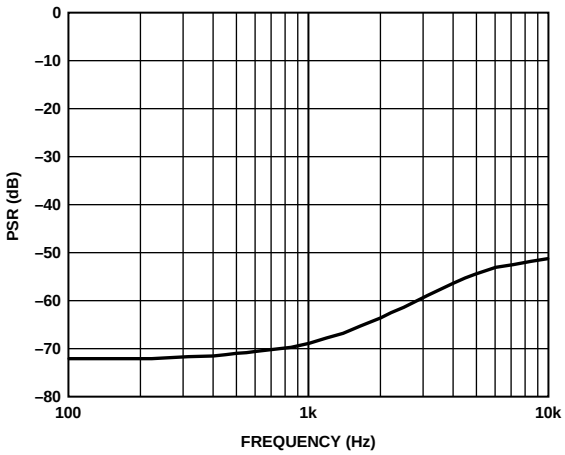

Figure 6. Power-Supply Rejection (PSR) vs. Frequency

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THEORY OF OPERATION

The ADMP441 is a high-performance, low-power, digital-output, omni-directional MEMS microphone with a bottom port. The complete ADMP441 solution consists of a MEMS sensor, signal conditioning, an analog-to-digital converter, anti-aliasing filters, power management, and an industry-standard 24-bit I²S interface.

The ADMP441 complies with the TIA-920 *Telecommunications Telephone Terminal Equipment Transmission Requirements for Wideband Digital Wireline Telephones* standard.

UNDERSTANDING SENSITIVITY

The casual user of digital microphones may have difficulty understanding the sensitivity specification. Unlike an analog microphone (whose specification is easily confirmed with an oscilloscope), the digital microphone output has no obvious unit of measure.

The ADMP441 has a nominal sensitivity of −26 dBFS at 1 kHz with an applied sound pressure level of 94 dB. The units are in decibels referred to full scale. The ADMP441 default full-scale peak output word is $2^{23} - 1$ (integer representation), and −26 dBFS of that scale is $(2^{23} - 1) \times 10^{(-26/20)}$ = 420,426. A pure acoustic tone at 1 kHz having a 1Pa RMS amplitude results in an output digital signal whose peak amplitude is 420,426.

Although the industry uses a standard specification of 94 dB SPL, the ADMP441 test method applies a 104 dB SPL signal. The higher sound pressure level reduces noise and improves repeatability. The ADMP441 has excellent gain linearity, and the sensitivity test result at 94 dB is derived with very high confidence from the test data.

POWER MANAGEMENT

The ADMP441 has three different power states: normal operation, standby mode, and power-down mode.

Normal Operation

The microphone becomes operational 2^{18} clock cycles (85 ms with SCK at 3.072 MHz) after initial power-up. The CHIPEN pin then controls the power modes. The part is in normal operation mode when SCK is active and the CHIPEN pin is high.

Standby Mode

The microphone enters standby mode when the serial-data clock SCK stops and CHIPEN is high. Normal operation resumes 2^{14} clock cycles (5 ms with SCK at 3.072 MHz) after SCK restarts.

The ADMP441 should not be transitioned from standby to power-down mode, or vice versa. Standby mode is only intended to be entered from the normal operation state.

Power-Down Mode

The microphone enters power-down mode when CHIPEN is low, regardless of the SCK operation. Normal mode operation resumes 2^{17} SCK clock cycles (43 ms with SCK at 3.072 MHz) after CHIPEN returns high while SCK is active.

It always takes 2^{17} clock cycles to restart the ADMP441 after V_{DD} is applied.

It is not recommended to supply active clocks (WS and SCK) to the ADMP441 while there is no power supplied to VDD. Doing this continuously turns on ESD protection diodes, which may affect long-term reliability of the microphone.

Startup

The microphones have zero output for the first 2^{18} SCK clock cycles (85ms with SCK at 3.072 MHz) following power-up.

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I²S DATA INTERFACE

The slave serial-data port's format is I²S, 24-bit, twos complement. There must be 64 SCK cycles in each WS stereo frame, or 32 SCK cycles per data-word. The L/R control pin determines whether the ADMP441 outputs data in the left or right channel. For a stereo application, the SD pins of the left and right ADMP441 microphones should be tied together as shown in Figure 9. The format of a stereo I²S data stream is shown in Figure 10. Figures 11 and 12 show the formats of a mono-microphone data stream for left and right microphones, respectively.

Data Output Mode

The output data pin (SD) is tri-stated when it is not actively driving I²S output data. SD immediately tri-states after the LSB is output so that another microphone can drive the common data line.

The SD trace should have a pull-down resistor to discharge the line during the time that all microphones on the bus have tri-stated their outputs. A 100 kΩ resistor is sufficient for this, as shown in Figure 9 .

Data-Word Length

The output data-word length is 24 bits per channel. The ADMP441 must always have 64 clock cycles for every stereo data-word ($f_{SCK} = 64 \times f_{WS}$).

Data-Word Format

The default data format is I²S (twos complement), MSB-first. In this format, the MSB of each word is delayed by one SCK cycle from the start of each half-frame.

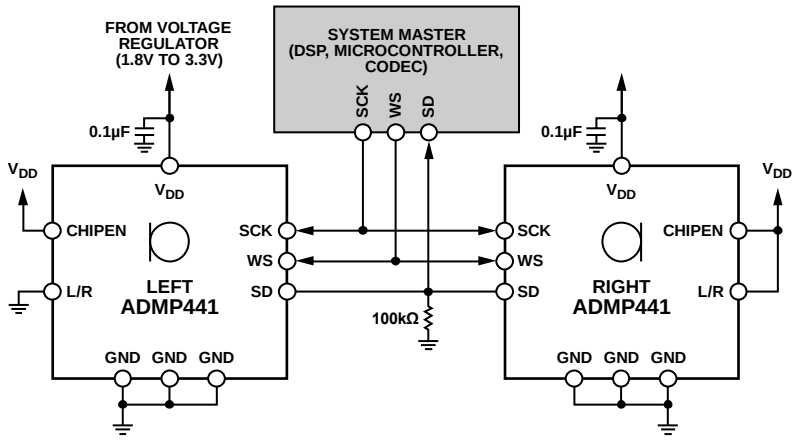

Figure 9. System Block Diagram

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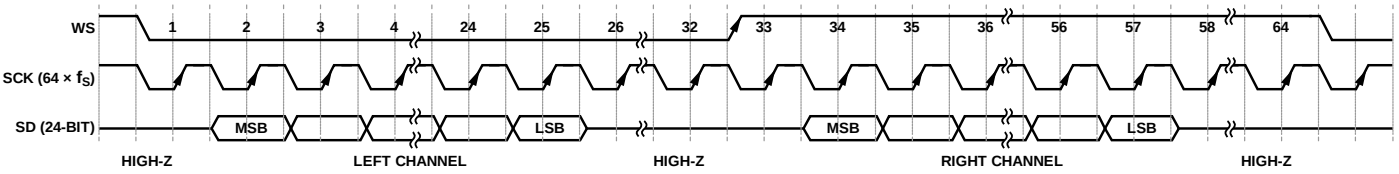

Figure 10. Stereo-Output I²S Format

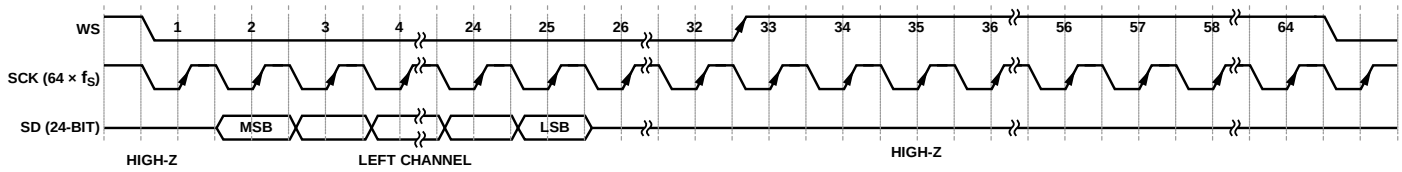

Figure 11. Mono-Output I²S Format Left Channel (L/R = 0)

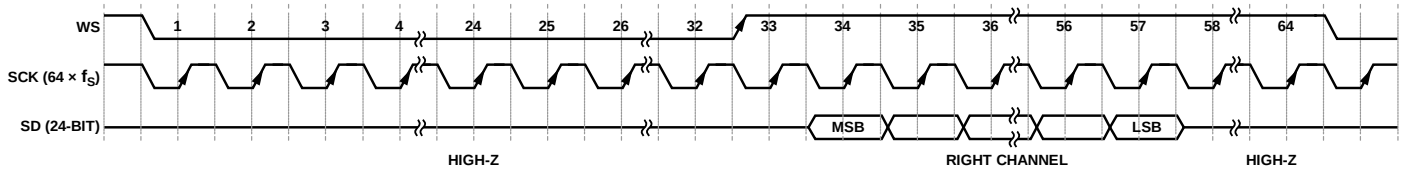

Figure 12. Mono-Output I²S Format Right Channel (L/R = 1)

DIGITAL MICROPHONE SENSITIVITY

The sensitivity of a PDM output microphone is specified in units of dBFS (decibels relative to a full-scale digital output). A 0 dBFS sine wave is defined as a signal whose peak just touches the full-scale code of the digital word (see Figure 7). This measurement convention means that signals with a different crest factor may have an RMS level higher than 0dBFS. For example, a full-scale square wave has an RMS level of 3dBFS.

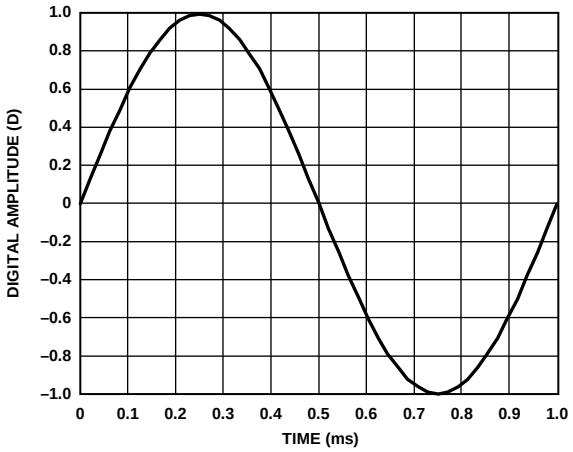

Figure 7. 1 kHz, 0 dBFS Sine Wave

The definition of a 0 dBFS signal must be understood when measuring the sensitivity of the ADMP441. An acoustic input signal of a 1 kHz sine wave at 94 dB SPL applied to the ADMP441 results in an output signal with a −26 dBFS level. This means that the output digital word peaks at −26 dB below the digital full-scale level. A common misunderstanding is that the output has an RMS level of −29 dBFS; however, this is not the case because of the definition of a 0 dBFS sine wave.

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There is no commonly accepted unit of measurement to express the instantaneous level of a digital signal output from the microphone, as opposed to the RMS level of the signal. Some measurement systems express the instantaneous level of an individual sample in units of D, where 1.0 D is digital full scale (see Figure 7). In this case, a −26 dBFS sine wave has peaks at 0.05 D.

For more information about digital microphone sensitivity, see the AN-1112 Application Note, *Microphone Specifications Explained*.

SYNCHRONIZING MICROPHONES

Stereo ADMP441 microphones are synchronized by the WS signal, so audio captured from two microphones sharing the same clock will be in sync. If the mics are enabled separately, this synchronization may take up to 0.35 ms after the enable signal is asserted while internal data paths are flushed.

DIGITAL FILTER CHARACTERISTICS

The ADMP441 has an internal digital band-pass filter. A high-pass filter eliminates unwanted low-frequency signals. A low-pass filter allows the user to scale the pass band with the sampling frequency, as well as perform required noise reduction.

HIGH-PASS FILTER

The ADMP441 incorporates a high-pass filter to remove unwanted DC and very low frequency components. This shows the high-pass characteristics for a nominal sampling rate of 48 kHz. The cutoff frequency scales with changes in sampling rate.

TABLE 7. HIGH PASS FILTER CHARACTERISTICS

FREQUENCY	ATTENTUATION
3.7 Hz	−3 dB
10.4 Hz	−0.5 dB
21.6 Hz	−0.1 dB

This digital filter response is in addition to the natural high-pass response of the ADMP441 MEMS acoustic transducer that has a -3 dB cutoff of 60 Hz.

LOW-PASS FILTER

The analog-to-digital converter in the ADMP441 is a single-bit, high-order, sigma-delta (Σ-Δ) running at a high oversampling ratio. The noise shaping of the converter pushes the majority of the noise well above the audio band and gives the microphone a wide dynamic range. However, it does require a good quality low-pass filter to eliminate the high-frequency noise.

Figure 13 shows the response of this digital low-pass filter included in the microphone. The pass band of the filter extends to 0.423 × f_S and, in that band, has an unnoticeable 0.04 dB of ripple. The high-frequency cutoff of −6 dB occurs at 0.5 × f_S. A 48 kHz sampling rate results in a pass band of 20.3 kHz and a half amplitude corner at 24 kHz. The stop-band attenuation of the filter is greater than 60 dB. Note that these filter specifications scale with sampling frequency.

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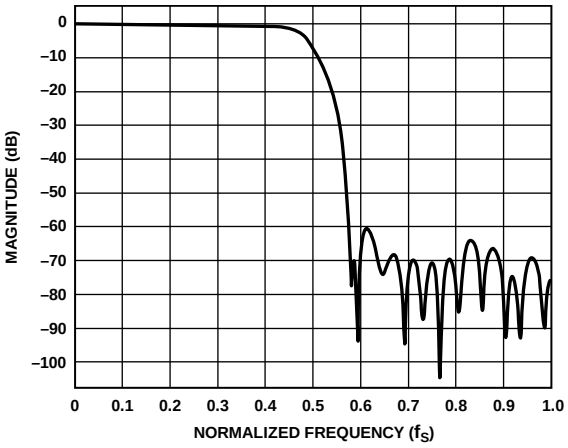

Figure 13. Digital Low-Pass Filter Magnitude Response

APPLICATIONS INFORMATION

POWER-SUPPLY DECOUPLING

For best performance and to avoid potential parasitic artifacts, placing a 0.1 µF ceramic type X7R or better capacitor between Pin 7 (VDD) and ground is strongly recommended. The capacitor should be placed as close to Pin 7 as possible.

The connections to each side of the capacitor should be as short as possible, and the trace should stay on a single layer with no vias. For maximum effectiveness, locate the capacitor equidistant from the power and ground pins, or if equidistant placement is not possible, slightly closer to the power pin. Thermal connections to the ground planes should be made on the far side of the capacitor, as shown in Figure 14.

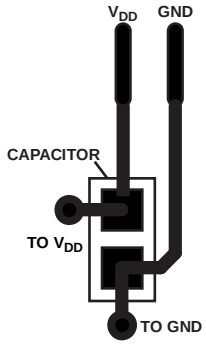

Figure 14. Recommended Power-Supply Bypass Capacitor Layout

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SUPPORTING DOCUMENTS

For additional information, see the following documents.

EVALUATION BOARD USER GUIDE

UG-303, EVAL-ADMP441Z-FLEX: Bottom Port I^{2}S Output MEMS Microphone Evaluation Board
UG-362, EVAL-ADMP441Z SDP Daughter Board for the ADMP441 I^{2}S MEMS Microphone

CIRCUIT NOTE

CN-0208, High Performance Digital MEMS Microphone's Simple Interface to SigmaDSP Audio Processor
CN-0266, High Performance Digital MEMS Microphone Standard Digital Audio Interface to Blackfin DSP

APPLICATION NOTES

AN-1003, Recommendations for Mounting and Connecting the Invensense, Inc., Bottom-Ported MEMS Microphones
AN-1068, Reflow Soldering of the MEMS Microphone
AN-1112, Microphone Specifications Explained
AN-1124, Recommendations for Sealing Invensense, Inc., Bottom-Port MEMS Microphones from Dust and Liquid Ingress
AN-1140, Microphone Array Beamforming

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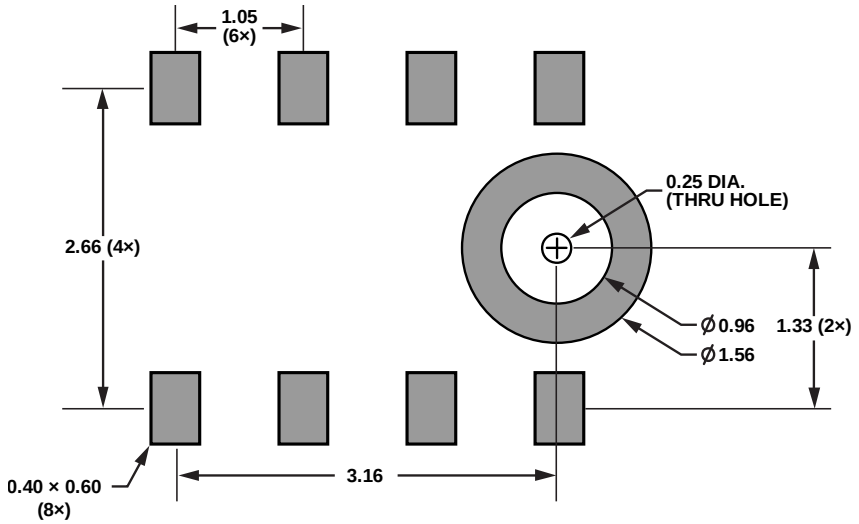
PCB DESIGN AND LAND PATTERN LAYOUT

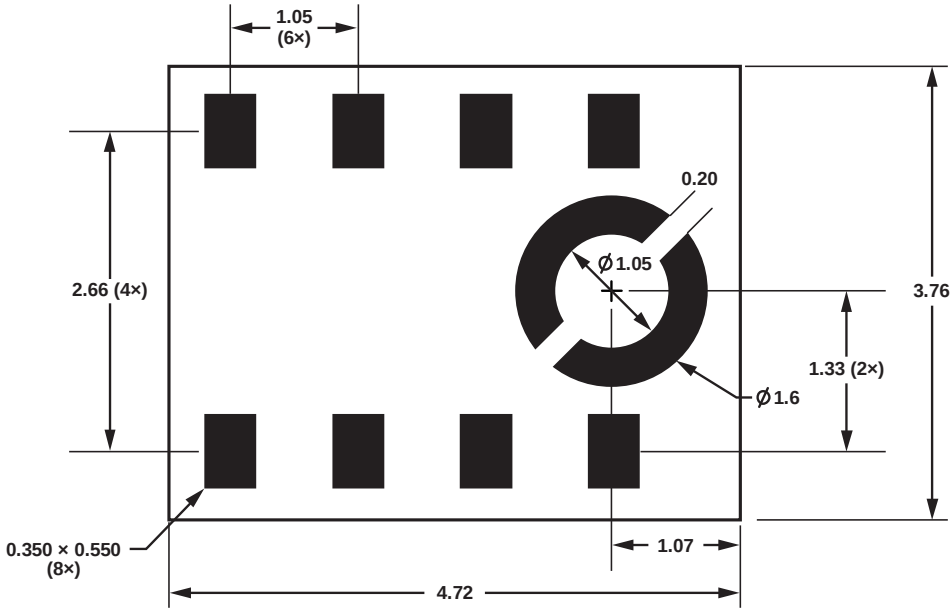
Lay out the PCB land pattern for the ADMP441 at a 1:1 ratio to the solder pads on the microphone package (see Figure 8.) Take care to avoid applying solder paste to the sound hole in the PCB. Figure 9 shows a suggested solder paste stencil pattern layout.
The response of the ADMP441 is not affected by the PCB hole size, as long as the hole is not smaller than the sound port of the microphone (0.25 mm, or 0.010 inch, in diameter). A 0.5 mm to 1 mm (0.020 inch to 0.040 inch) diameter for the hole is recommended.

Align the hole in the microphone package with the hole in the PCB. The exact degree of the alignment does not affect the performance of the microphone as long as the holes are not partially or completely blocked.



DIMENSIONS SHOWN IN MILLIMETERS

Figure 8. Suggested PCB Land Pattern Layout



DIMENSIONS SHOWN IN MILLIMETERS

Figure 9. Suggested Solder Paste Stencil Pattern Layout

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PCB MATERIAL AND THICKNESS

The performance of the ADMP441 is not affected by PCB thickness. The ADMP441 can be mounted on either a rigid or flexible PCB. A flexible PCB with the microphone can be attached directly to the device housing with an adhesive layer. This mounting method offers a reliable seal around the sound port while providing the shortest acoustic path for good sound quality.

HANDLING INSTRUCTIONS

PICK AND PLACE EQUIPMENT

The MEMS microphone can be handled using standard pick-and-place and chip shooting equipment. Take care to avoid damage to the MEMS microphone structure as follows:

- Use a standard pickup tool to handle the microphone. Because the microphone hole is on the bottom of the package, the pickup tool can make contact with any part of the lid surface.
- Do not pick up the microphone with a vacuum tool that makes contact with the bottom side of the microphone. Do not pull air out of or blow air into the microphone port.
- Do not use excessive force to place the microphone on the PCB.

REFLOW SOLDER

For best results, the soldering profile must be in accordance with the recommendations of the manufacturer of the solder paste used to attach the MEMS microphone to the PCB. It is recommended that the solder reflow profile not exceed the limit conditions specified in Figure 2 and Table 5.

BOARD WASH

When washing the PCB, ensure that water does not make contact with the microphone port. Do not use blow-off procedures or ultrasonic cleaning.

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OUTLINE DIMENSIONS

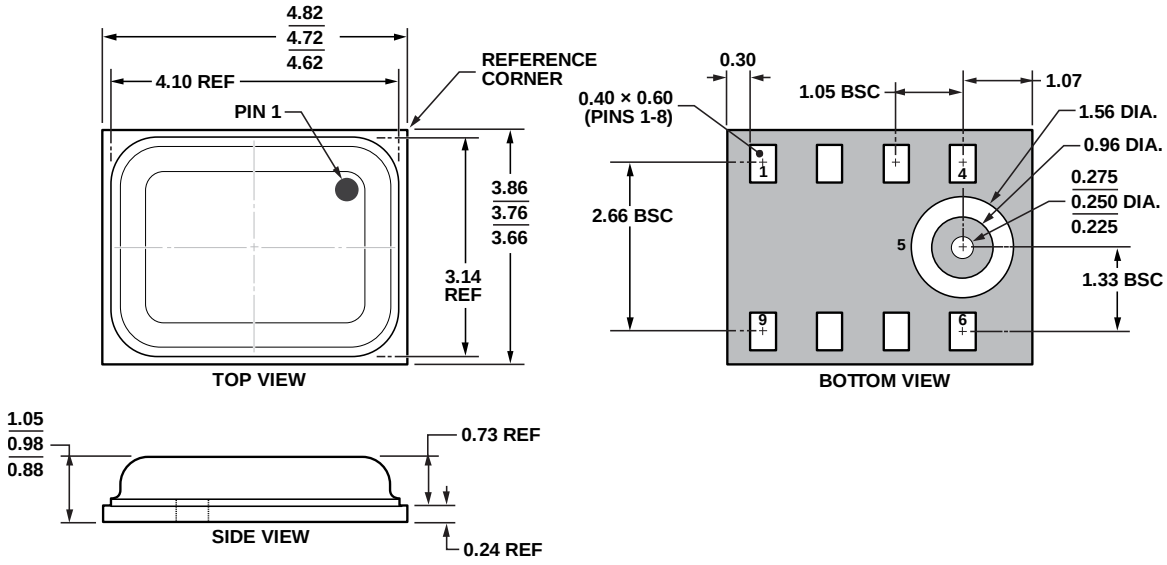

Figure 10. 9-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]
4.72 mm × 3.76 mm × 1.00 mm Body
(CE-9-1)
Dimensions shown in millimeters

ORDERING GUIDE

PART	TEMP RANGE	PACKAGE	PACKAGE OPTION	QUANTITY
ADMP441ACEZ-RL	−40°C to +85°C	9-Terminal LGA_CAV*	CE-9-1	4,500
ADMP441ACEZ-RL7	−40°C to +85°C	9-Terminal LGA_CAV†	CE-9-1	1,000
EVAL-ADMP441Z-FLEX	—	Flexible Evaluation Board	—	—
EVAL-ADMP441Z	—	Evaluation Board	—	—

* – 13” Tape and Reel
† – 7” Tape and Reel

REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
11/25/2013	1.0	Initial Release

Document Number: DS-ADMP441-00
Revision: 1.0.

Compliance Declaration Disclaimer:

InvenSense believes this compliance information to be correct but cannot guarantee accuracy or completeness. Conformity documents for the above component constitutes are on file. InvenSense subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by InvenSense

Environmental Declaration Disclaimer:

InvenSense believes this environmental information to be correct but cannot guarantee accuracy or completeness. Conformity documents for the above component constitutes are on file. InvenSense subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by InvenSense

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