LTM2892-S
SPI/Digital µModule Isolator

DESCRIPTION

Demonstration circuit 1957A is a serial peripheral interface bus (SPI) or digital µModule isolator featuring the LTM2892-S. The demo circuit operates from external supply voltages on V_{CC1}, V_{L1}, V_{CC2}, and V_{L2}. It communicates all necessary signaling across the isolation barrier through LTC's Isolator™ µModule® technology.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC1}, V_{CC2}	Input Supply Range		3.0		5.5	V
V_{L1}, V_{L2}	Logic Supply Range		1.62		5.5	V
f_{MAX}	Maximum Data Rate	INx → OUTx, C_L = 15pF	20			MHz
		SPI Bidirectional Communication SPI Unidirectional Communication	4 8			MHz MHz
V_{IORM}	Maximum Working Insulation Voltage	GND1 to GND2	850			V_{DC}
			600			V_{RMS}
	Common Mode Transient Immunity		50			kV/µs

OPERATING PRINCIPLES

The LTM2892-S requires two to four external power supplies for operation, one for power and one for the signal interface, on each side of the isolation barrier. The logic supplies may be tied to the input supplies. Isolation is maintained by the separation of GND1 and GND2 where significant operating voltages and transients can exist without affecting the operation of the LTM2892-S. The ON1 and/or ON2 pins enable or shut down the LTM2892-S, both must be driven to their respective logic supply voltage for proper operation. All SPI or Digital signals are referenced to the logic supply pins V_{L1} or V_{L2}.

SPI signaling is typically configured by defining the digital pins as follows:

Logic Side: IN1 = SCK(IN), IN2 = SDI(IN), IN3 = $\overline{CS}$(IN) = $\overline{SDOE}$, and OUTD = SDO(OUT).

Isolated Side: OUT1 = SCK(OUT), OUT2 = SDI(OUT), OUT3 = $\overline{CS}$(OUT), and IND = SDO(IN).

Reference Figure 1 for schematic representation.

No special precautions are required for low RF emissions. EMI performance is shown in Figure 2, measured using a gigahertz transverse electromagnetic (GTEM) cell and method detailed in IEC 61000-4-20, Testing and Measurement Techniques – Emission and Immunity Testing in Transverse Electromagnetic Waveguides.

OPERATING PRINCIPLES

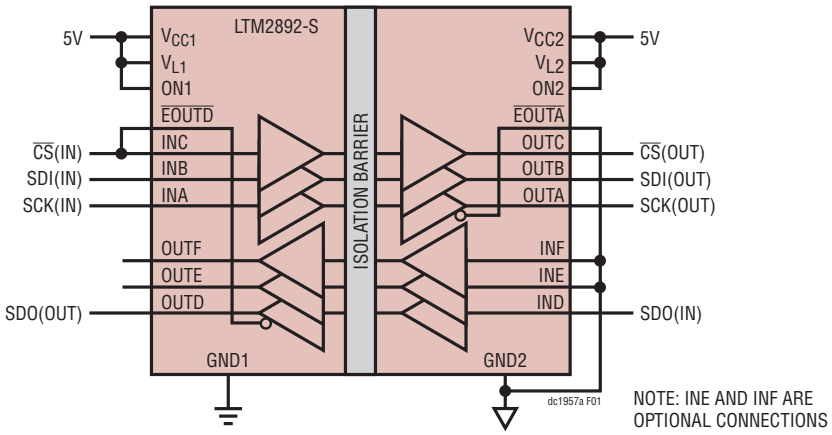


Figure 1. SPI Pin Definition

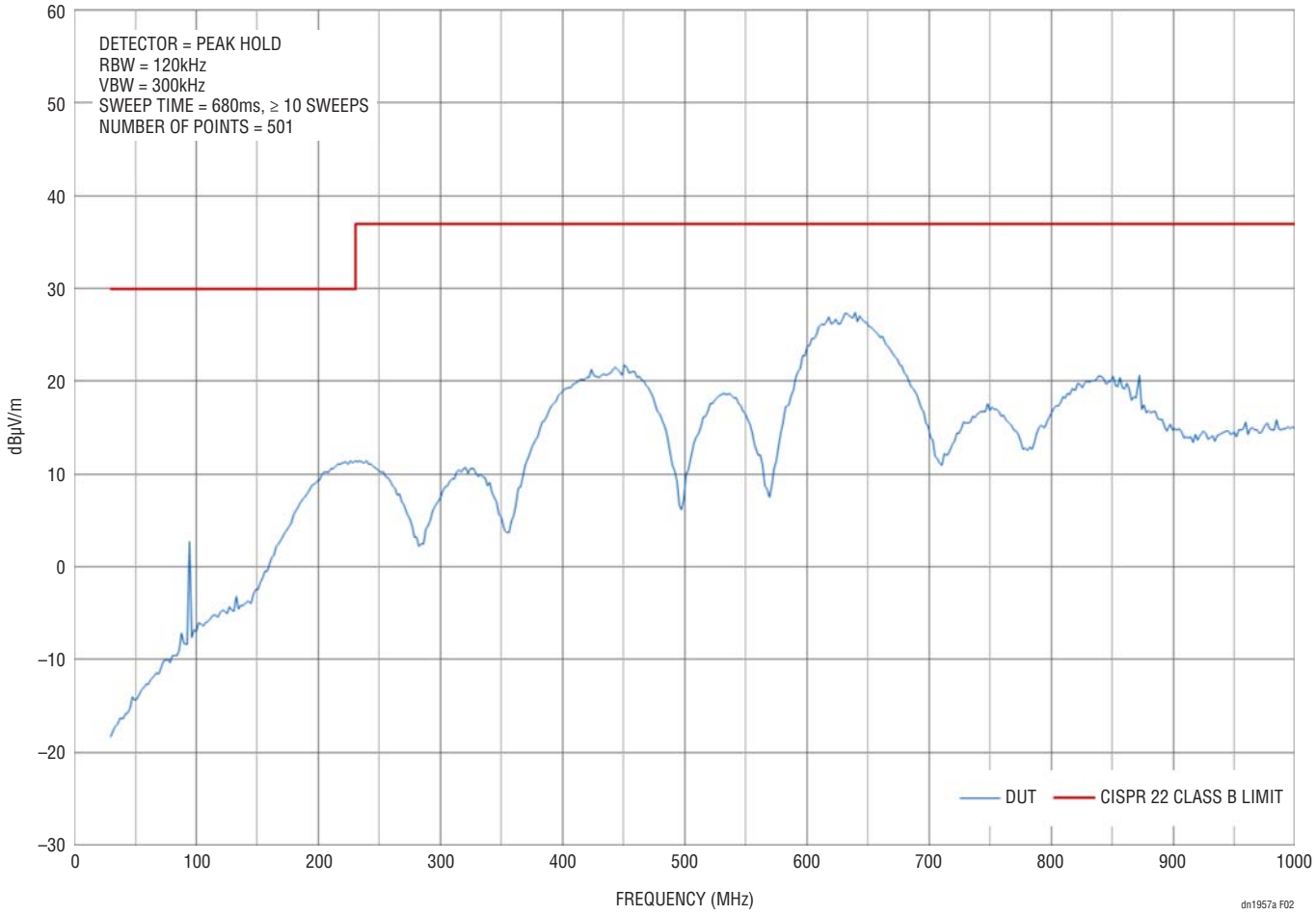


Figure 2. DC1957A Radiated Emissions

QUICK START PROCEDURE

Demonstration circuit 1957A is easy to set up and evaluate the performance of the LTM2892-S. Refer to Figure 3 for proper measurement equipment setup and follow the procedure below.

NOTE: When measuring the input or output voltage ripple or high speed signals, care must be taken to avoid a long ground lead on the oscilloscope probe.

1. Install jumpers as shown in Figure 3 and the schematic diagram.
2. With power off, connect the input power supplies to V_{CC1} - GND1 and V_{CC2} - GND2 as shown.
3. Turn on the power at the input.

   NOTE: Make sure that the input voltage does not exceed 6V.
4. Configure jumpers or connect signals to turrets as appropriate. If a signal is connected to an input channel turret the associated channel jumper must be removed for proper operation.

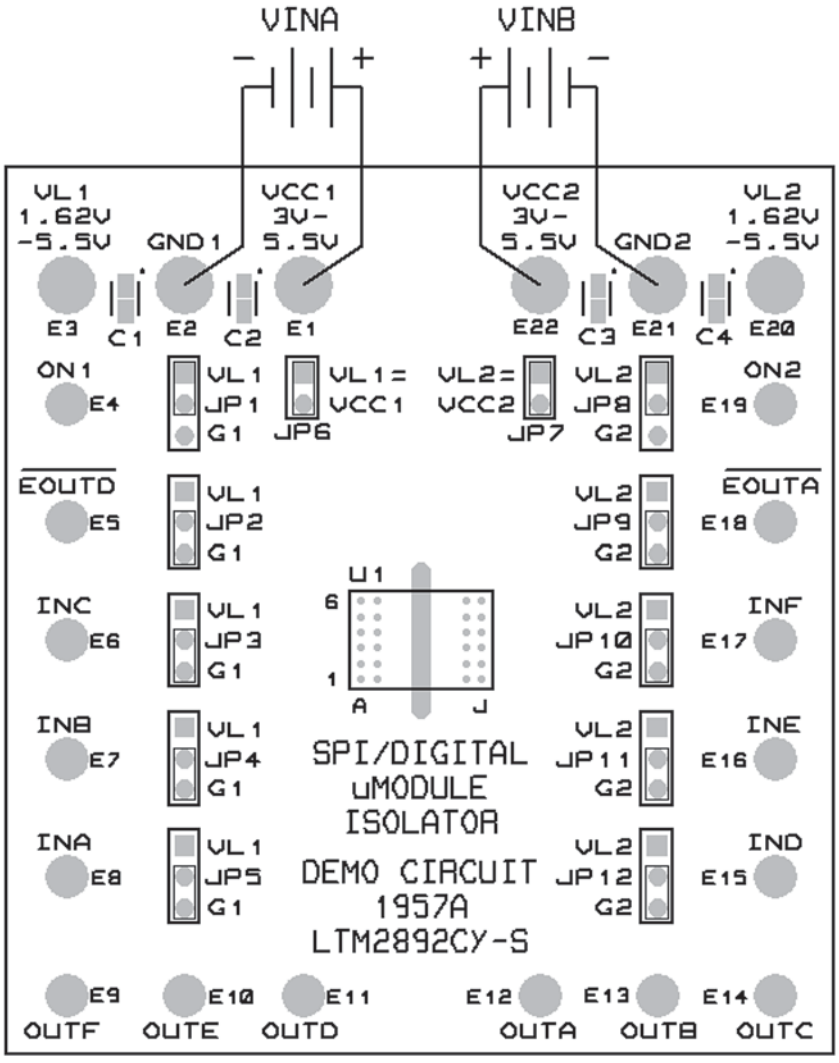
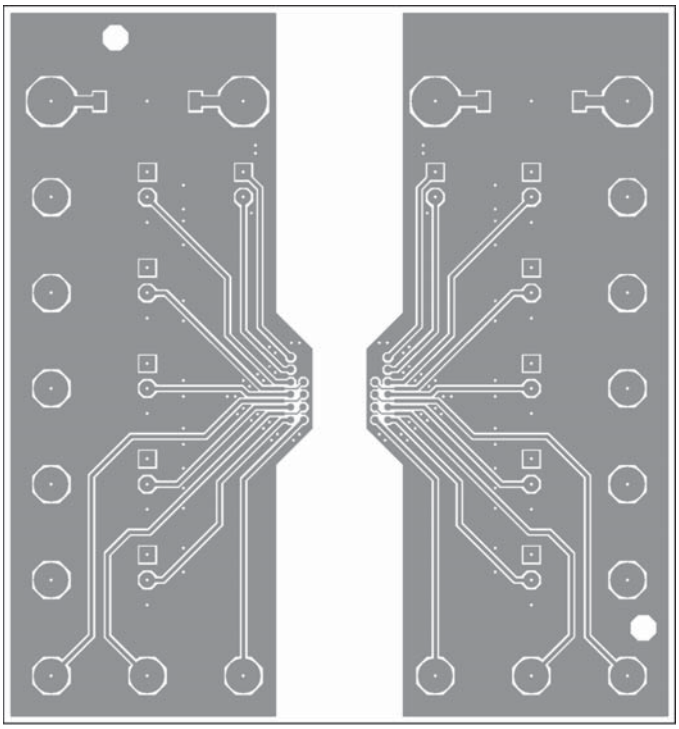
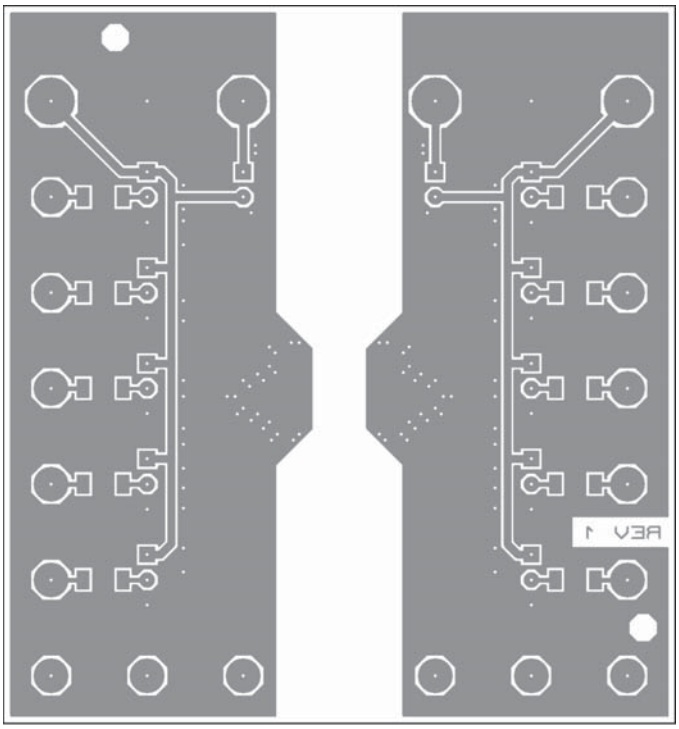


Figure 3. Demo Board Setup

PCB LAYOUT



Top Copper

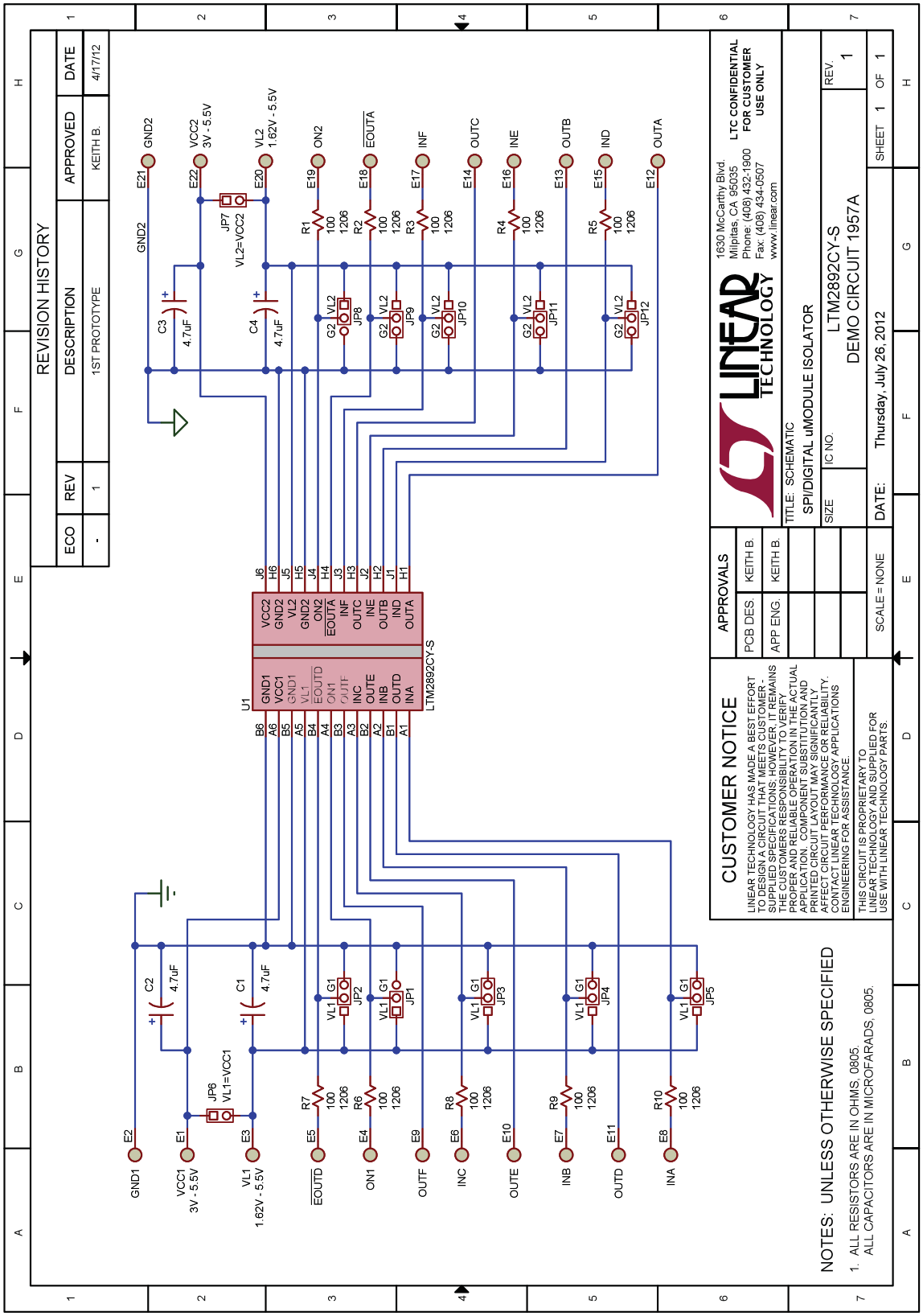


Bottom Copper

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	U1	I.C., LTM2892CY-S	LINEAR LTM2892CY-S#PBF
Hardware: For Demo Board Only				
2	4	C1-4	CAP., TANT 4.7µF 10V 20% 0805	NICHICON F921A475MPA
3	16	E4-19	TURRET, 0.065"	MILL-MAX 2308-2-00-80-00-00-07-0
4	6	E1-3, E20-22	TURRET, 0.095"	MILL-MAX 2501-2-00-80-00-00-07-0
5	2	JP6-7	2mm SINGLE ROW HEADER, 2 X 1 PIN	SAMTEC TMM-102-02-L-S
6	10	JP1-5, JP8-12	2mm SINGLE ROW HEADER, 3 x 1 PIN	SAMTEC TMM-103-02-L-S
7	12	JP1-12	2mm SHUNT	SAMTEC 2SN-BK-G
8	10	R1-R10	RES., CHIP 100Ω 5% 1206	AAC CR18-101JM

SCHEMATIC DIAGRAM



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