IEEE 802.3at High Power PD and Synchronous Forward Controller with AUX Support

FEATURES

- **25.5W IEEE 802.3at Compliant (Type-2) PD**
- **PoE+ 2-Event Classification**
- **IEEE 802.3at *High Power Available* Indicator**
- **Integrated State-of-the-Art Synchronous Forward Controller**
  - **Isolated Power Supply Efficiency >94%**
- **Flexible Auxiliary Power Interface**
- **Superior EMI Performance**
- **Robust 100V 0.7Ω (Typ) Integrated Hot Swap™ MOSFET**
- Integrated Signature Resistor, Programmable Class Current, UVLO, OVLO and Thermal Protection
- Short-Circuit Protection with Auto-Restart
- Programmable Switching Frequency from 100kHz to 500kHz
- Thermally Enhanced 7mm × 4mm DFN Package

APPLICATIONS

- IP Phones with Large Color Screens
- Dual Radio 802.11n Access Points
- PTZ Security Cameras

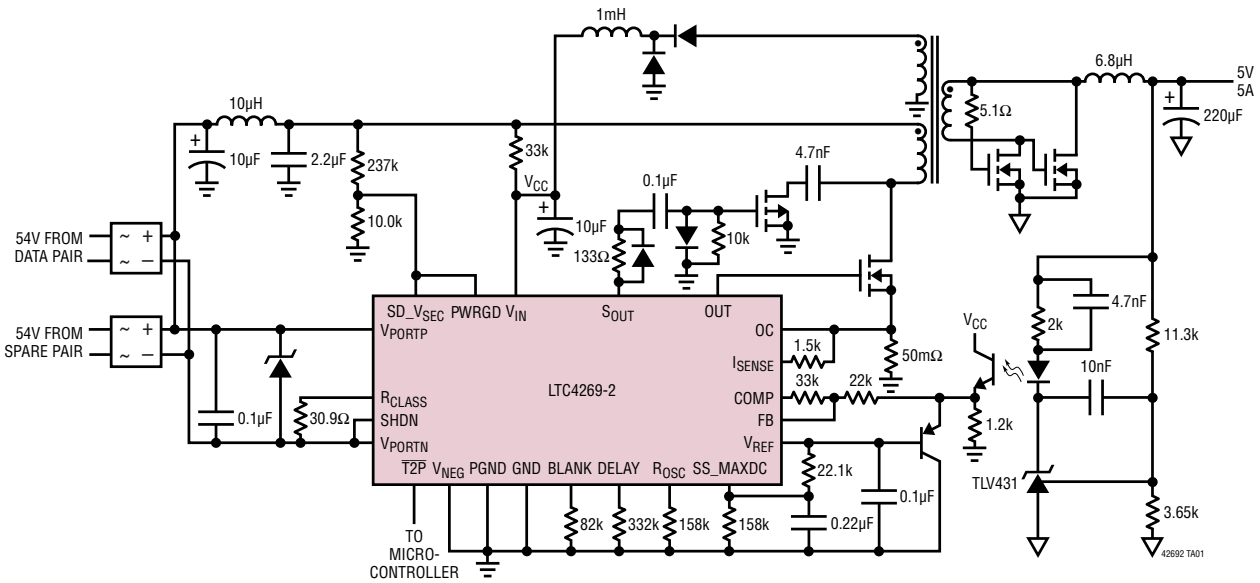
DESCRIPTION

The LTC®4269-2 is an integrated Powered Device (PD) interface and power supply controller featuring 2-event classification signaling, flexible auxiliary power options, and a power supply controller suitable for synchronously rectified forward supplies. These features make the LTC4269-2 ideally suited for an IEEE802.3at PD application.

The PD controller features a 100V MOSFET that isolates the power supply during detection and classification, and provides 100mA inrush current limit. Also included are power good outputs, an undervoltage/overvoltage lockout and thermal protection. The current mode forward controller allows for synchronous rectification, resulting in an extremely high efficiency, green product. Soft-start for controlled output voltage start-up and fault recovery is included. Programmable frequency over 100kHz to 500kHz allows flexibility in efficiency vs size and low EMI.

TYPICAL APPLICATION

PoE-Based Self-Driven Synchronous Forward Power Supply



ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Pins with Respect to V_{PORTN}

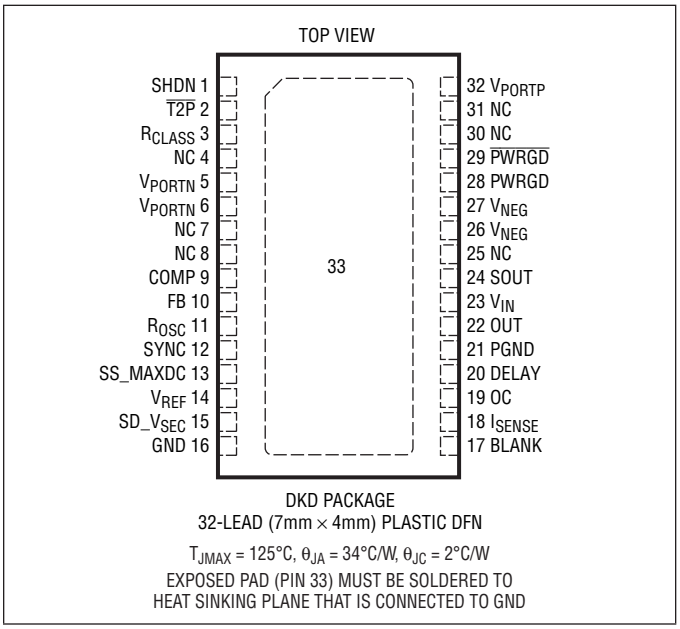
V_{PORTP} Voltage ..... –0.3V to 100V
V_{NEG} Voltage ..... –0.3V to V_{PORTP}
V_{NEG} Pull-Up Current 1A
SHDN ..... –0.3V to 100V
R_{CLASS}, Voltage ..... –0.3V to 7V
R_{CLASS} Source Current 50mA
PWRGD Voltage (Note 3)
  Low Impedance Source .... V_{NEG} – 0.3V to V_{NEG} + 11V
  Sink Current 5mA
$\overline{PWRGD}$, $\overline{T2P}$ Voltage ..... –0.3V to 100V
$\overline{PWRGD}$, $\overline{T2P}$ Sink Current 10mA

Pins with Respect to GND

V_{IN} (Note 4) ..... –0.3V to 25V
SYNC, SS_MAXDC, SD_V_{SEC},
I_{SENSE}, OC ..... –0.3V to 6V
COMP, BLANK, DELAY ..... –0.3V to 3.5V
FB ..... –0.3V to 3V
R_{OSC} Current ..... –50µA
V_{REF} Source Current 10mA

Operating Ambient Temperature Range
  LTC4269C-2 ..... 0°C to 70°C
  LTC4269I-2 ..... –40°C to 85°C

PIN CONFIGURATION



DKD PACKAGE
32-LEAD (7mm × 4mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W, θ_{JC} = 2°C/W

EXPOSED PAD (PIN 33) MUST BE SOLDERED TO HEAT SINKING PLANE THAT IS CONNECTED TO GND

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4269CDKD-2#PBF	LTC4269CDKD-2#TRPBF	42692	32-Lead (7mm × 4mm) Plastic DFN	0°C to 70°C
LTC4269IDKD-2#PBF	LTC4269IDKD-2#TRPBF	42692	32-Lead (7mm × 4mm) Plastic DFN	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC4269CDKD-2	LTC4269CDKD-2#TR	42692	32-Lead (7mm × 4mm) Plastic DFN	0°C to 70°C
LTC4269IDKD-2	LTC4269IDKD-2#TR	42692	32-Lead (7mm × 4mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Interface Controller (Note 5)						
Operating Input Voltage	At V_{PORTP} (Note 6)				60	V
Signature Range		●	1.5		9.8	V
Classification Range		●	12.5		21.0	V
On Voltage		●			37.2	V
Undervoltage Lockout		●	30.0			V
Overvoltage Lockout				71.0		V
ON/UVLO Hysteresis Window		●	4.1			V
Signature/Class Hysteresis Window		●	1.4			V
Reset Threshold	State Machine Reset for 2-Event Classification	●	2.57		5.40	V
Supply Current						
Supply Current at 57V	Measured at V_{PORTP} Pin	●			1.35	mA
Class 0 Current	V_{PORTP} = 17.5V, No R_{CLASS} Resistor	●			0.40	mA
Signature						
Signature Resistance	1.5V ≤ V_{PORTP} ≤ 9.8V (Note 7)	●	23.25		26.00	kΩ
Invalid Signature Resistance, SHDN Invoked	1.5V ≤ V_{PORTP} ≤ 9.8V, V_{SHDN} = 3V (Note 7)	●			11	kΩ
Invalid Signature Resistance During Mark Event	(Notes 7, 8)	●			11	kΩ
Classification						
Class Accuracy	10mA < I_{CLASS} < 40mA, 12.5V < V_{PORTP} < 21V (Notes 9, 10)	●			±3.5	%
Classification Stability Time	V_{PORTP} Pin Step to 17.5V, R_{CLASS} = 30.9Ω, I_{CLASS} within 3.5% of Ideal Value (Notes 9, 10)	●			1	ms
Normal Operation						
Inrush Current	V_{PORTP} = 54V, V_{NEG} = 3V	●	60	100	180	mA
Power FET On-Resistance	Tested at 600mA into V_{NEG}, V_{PORTP} = 54V	●		0.7	1.0	Ω
Power FET Leakage Current at V_{NEG}	V_{PORTP} = SHDN = V_{NEG} = 57V	●			1	µA
Digital Interface						
SHDN Input High Level Voltage		●	3			V
SHDN Input Low Level Voltage		●			0.45	V
SHDN Input Resistance	V_{PORTP} = 9.8V, SHDN = 9.65V	●	100			kΩ
$\overline{PWRGD}$, $\overline{T2P}$ Output Low Voltage	Tested at 1mA, V_{PORTP} = 57V, For $\overline{T2P}$, Must Complete 2-Event Classification to See Active Low	●			0.15	V
$\overline{PWRGD}$, $\overline{T2P}$ Leakage Current	Pin Voltage Pulled 57V, V_{PORTP} = V_{PORTN} = 0V	●			1	µA
PWRGDP Output Low Voltage	Tested at 0.5mA, V_{PORTP} = 52V, V_{NEG} = 4V, Output Voltage is with Respect to V_{NEG}	●			0.4	V
PWRGDP Clamp Voltage	Tested at 2mA, V_{NEG} = 0V, Voltage is with Respect to V_{NEG}	●	12.0		16.5	V
PWRGDP Leakage Current	V_{PWRGD} = 11V, V_{NEG} = 0V, Voltage is with Respect to V_{NEG}	●			1	µA
PWM Controller (Note 11)						
Operational Input Voltage	I_{VREF} = 0µA	●	$V_{IN(OFF)}$		25	V
V_{IN} Quiescent Current	I_{VREF} = 0µA, I_{SENSE} = OC = Open			5.2	6.5	mA
V_{IN} Start-Up Current	FB = 0V, SS_MAXDC = 0V (Notes 12, 13)	●		460	700	µA
V_{IN} Shutdown Current	SD_V_{SEC} = 0V (Notes 12, 13)	●		240	350	µA
SD_V_{SEC} Threshold	10V < SD < 25V		1.261	1.32	1.379	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SD_$V_{SEC(ON)}$ Current	SD_V_{SEC} = SD_V_{SEC} Threshold +100mV			0		µA
SD_$V_{SEC(OFF)}$ Current	SD_V_{SEC} = SD_V_{SEC} Threshold – 100mV		8.3	10	11.7	µA
$V_{IN(ON)}$		●		14.25	15.75	V
$V_{IN(OFF)}$		●		8.75	9.25	V
$V_{IN(HYST)}$		●	3.75	5.5	7.0	V
V_{REF}						
Output Voltage	I_{VREF} = 0	●	2.425	2.5	2.575	V
Line Regulation	I_{VREF} = 0, 10V < V_{IN} < 25V			1	10	mV
Load Regulation	0mA < I_{VREF} < 2.5mA			1	10	mV
Oscillator						
Frequency, f_{OSC}	R_{OSC} = 178k, FB = 1V, SS_MAXDC = 1.84V	●	165	200	240	kHz
$f_{OSC(MIN)}$	R_{OSC} = 365k, FB = 1V		80	100	120	kHz
$f_{OSC(MAX)}$	R_{OSC} = 64.9k, COMP = 2.5V, SD_V_{SEC} = 2.64V		440	500	560	kHz
SYNC Input Resistance				18		kΩ
SYNC Switching Threshold	FB = 1V			1.5	2.2	V
SYNC Frequency/f_{OSC}	FB = 1V (Note 14)			1.25	1.5	
f_{OSC} Line Regulation	R_{OSC} = 178k; 10V < V_{IN} < 25V, SS_MAXDC = 1.84V			0.05	0.33	%/V
V_{ROSC}	R_{OSC} Pin Voltage			1		V
Error Amplifier						
FB Reference Voltage	10V < V_{IN} < 25V, V_{OL} + 0.2V < COMP < V_{OH} – 0.2	●	1.201	1.226	1.250	V
FB Input Bias Current	FB = FB Reference Voltage			-75	-200	nA
Open-Loop Voltage Gain	V_{OL} + 0.2V < COMP < V_{OH} – 0.2		65	85		dB
Unity-Gain Bandwidth	(Note 15)			3		MHz
COMP Source Current	FB = 1V, COMP = 1.6V		–4	–9		mA
COMP Sink Current	COMP = 1.6V		4	10		mA
COMP Current (Disabled)	FB = V_{REF}, COMP = 1.6V		18	23	28	µA
COMP High Level V_{OH}	FB = 1V, I_{COMP} = –250µA		2.7	3.2		V
COMP Active Threshold	FB = 1V, SOUT Duty Cycle > 0%		0.7	0.8		V
COMP Low Level V_{OL}	I_{COMP} = 250µA			0.15	0.4	V
Current Sense						
I_{SENSE} Maximum Threshold	COMP = 2.5V, FB =1V		197	220	243	mV
I_{SENSE} Input Current (Duty Cycle = 0%)	COMP = 2.5V, FB = 1V (Note 12)			–8		µA
I_{SENSE} Input Current (Duty Cycle = 80%)	COMP = 2.5V, FB = 1V (Note 12)			–35		µA
OC Threshold	COMP = 2.5V, FB = 1V		98	107	116	mV
OC Input Current	(OC = 100mV)			–50	–100	nA
Default Blanking Time	COMP = 2.5V, FB = 1V, R_{BLANK} = 40k (Note 16)			180		ns
Adjustable Blanking Time	COMP = 2.5V, FB = 1V, R_{BLANK} = 120k			540		ns
V_{BLANK}				1		V
SOUT Driver						
SOUT Clamp Voltage	I_{GATE} = 0µA, COMP = 2.5V, FB = 1V		10.54	12	13.5	V
SOUT Low Level	I_{GATE} = 25mA			0.5	0.75	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SOUT High Level	I_{GATE} = –25mA, V_{IN} = 12V COMP = 2.5V, FB = 1V		10			V
SOUT Active Pull-Off in Shutdown	V_{IN} = 5V, SD_V_{SEC} = 0V, SOUT = 1V		1			mA
SOUT to OUT (Rise) DELAY (t_{DELAY})	COMP = 2.5V, FB = 1V (Note 16) R_{DELAY} = 120k			40 120		ns ns
V_{DELAY}				0.9		V
OUT Driver						
OUT Rise Time	FB = 1V, C_L = 1nF (Notes 15, 16)			50		ns
OUT Fall Time	FB = 1V, C_L = 1nF (Notes 15, 16)			30		ns
OUT Clamp Voltage	I_{GATE} = 0µA, COMP = 2.5V, FB = 1V		11.5	13	14.5	V
OUT Low Level	I_{GATE} = 20mA I_{GATE} = 200mA			0.45 1.25	0.75 1.8	V V
OUT High Level	I_{GATE} = –20mA, V_{IN} = 12V COMP = 2.5V, FB = 1V I_{GATE} = –200mA, V_{IN} = 12V COMP = 2.5V, FB = 1V		9.9 9.75			V V
OUT Active Pull-Off in Shutdown	V_{IN} = 5V, SD_V_{SEC} = 0V, OUT = 1V		20			mA
OUT Max Duty Cycle	COMP = 2.5V, FB = 1V, R_{DELAY} = 10k (f_{OSC} = 200kHz), V_{IN} = 10V, SD_V_{SEC} = 1.4V, SS_MAXDC = V_{REF}		83	90		%
OUT Max Duty Cycle Clamp	COMP = 2.5V, FB = 1V, R_{DELAY} = 10k (f_{OSC} = 200kHz), V_{IN} = 10V SD_V_{SEC} = 1.32V, SS_MAXDC = 1.84V SD_V_{SEC} = 2.64V, SS_MAXDC = 1.84V		 63.5 25	 72 33	 80.5 41	 % %
Soft-Start						
SS_MAXDC Low Level: V_{OL}	I_{SS_MAXDC} = 150µA, OC = 1V			0.2		V
SS_MAXDC Soft-Start Reset Threshold	Measured on SS_MAXDC			0.45		V
SS_MAXDC Active Threshold	FB + 1V, DC > 0%			0.8		V
SS_MAXDC Input Current (Soft-Start Pull-Down: I_{DIS})	SS_MAXDC = 1V, SD_V_{SEC} = 1.4V, OC = 1V			800		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Pins with 100V absolute maximum guaranteed for T ≥ 0°C, otherwise 90V.

Note 3: PWRGD voltage clamps at 14V with respect to V_{NEG}.

Note 4: In applications where the V_{IN} pin is supplied via an external RC network from a system V_{IN} > 25V, an external Zener with clamp voltage $V_{IN\ ON(MAX)}$ < V_Z < 25V should be connected from the V_{IN} pin to GND.

Note 5: All voltages are with respect to V_{PORTN} pin unless otherwise noted.

Note 6: Input voltage specifications are defined with respect to LTC4269-2 pins and meet IEEE 802.3af/at specifications when the input diode bridge is included.

Note 7: Signature resistance is measured via the ΔV/ΔI method with the minimum ΔV of 1V. The LTC4269-2 signature resistance accounts for the additional series resistance in the input diode bridge.

Note 8: An invalid signature after the 1st classification event is mandated by IEEE 802.3at standard. See the Applications Information section.

Note 9: Class accuracy is respect to the ideal current defined as 1.237/R_{CLASS} and does not include variations in R_{CLASS} resistance.

Note 10: This parameter is assured by design and wafer level testing.

Note 11: Voltages are with respect to GND unless otherwise specified. Tested with COMP open, V_{FB} = 1.4V, R_{ROSC} = 178k, V_{SYNC} = 0V, $V_{SS(MAXDC)}$ set to V_{REF} (but electrically isolated), C_{VREF} = 0.1µF, V_{SD_VSEC} = 2V, R_{BLANK} = 121k, R_{DELAY} = 121k, V_{ISENSE} = 0V, V_{OC} = 0V, C_{OUT} = 1nF, V_{IN} = 15V, SOUT open, unless otherwise specified.

Note 12: Guaranteed by correlation to static test.

Note 13: V_{IN} start-up current is measured at V_{IN} = $V_{IN(ON)}$ – 0.25V and scaled by × 1.18 (to correlate to worst-case V_{IN} start-up current at $V_{IN(ON)}$.

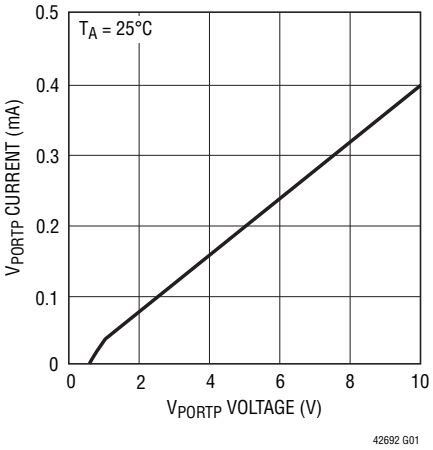
Note 14: Maximum recommended SYNC frequency = 500kHz.

Note 15: Guaranteed but not tested.

Note 16: Timing for R = 40k derived from measurement with R = 240k.

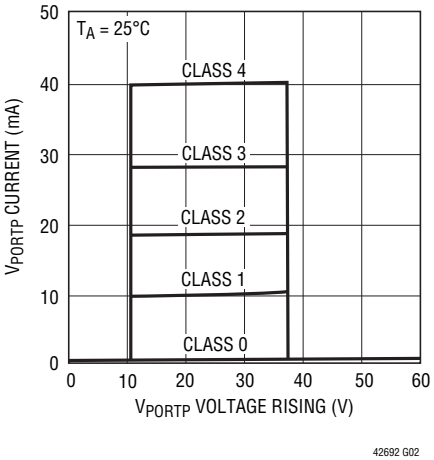
TYPICAL PERFORMANCE CHARACTERISTICS

Input Current vs Input Voltage 25k Detection Range



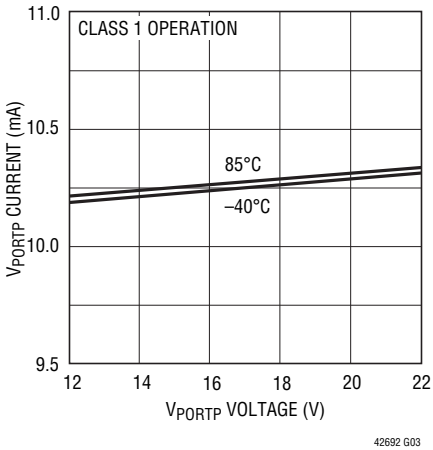
42692 G01

Input Current vs Input Voltage



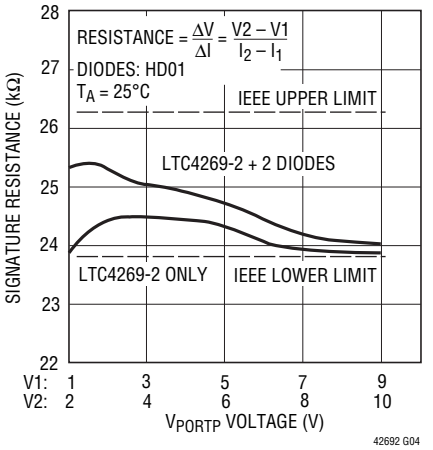
42692 G02

Input Current vs Input Voltage



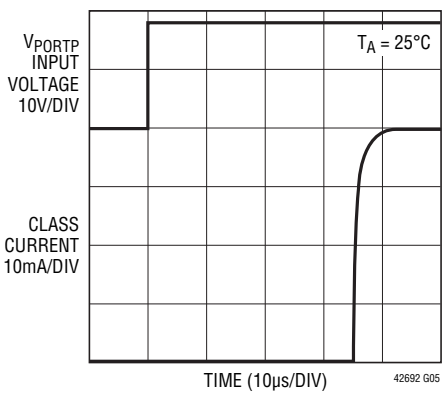
42692 G03

Signature Resistance vs Input Voltage



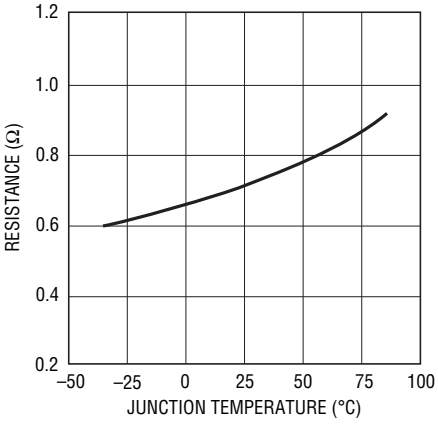
42692 G04

Class Operation vs Time



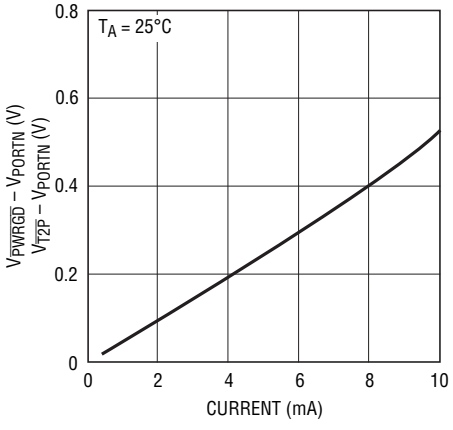
42692 G05

On-Resistance vs Temperature



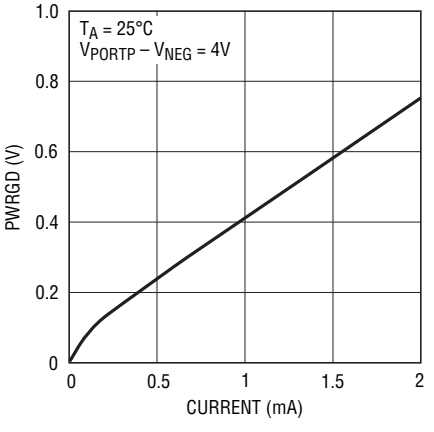
42692 G06

$\overline{PWRGD}$, $\overline{T2P}$ Output Low Voltage vs Current



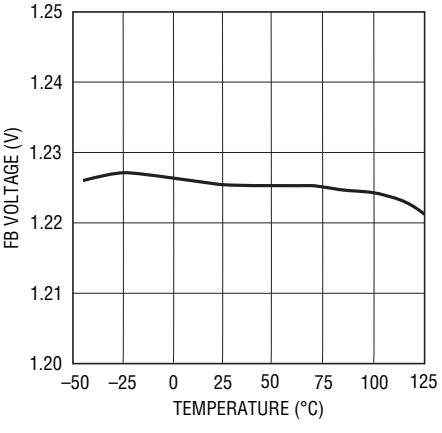
42692 G07

Active High PWRGD Output Low Voltage vs Current



42692 G08

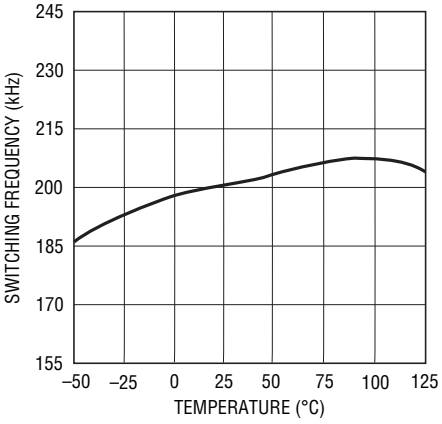
FB Voltage vs Temperature



42692 G09

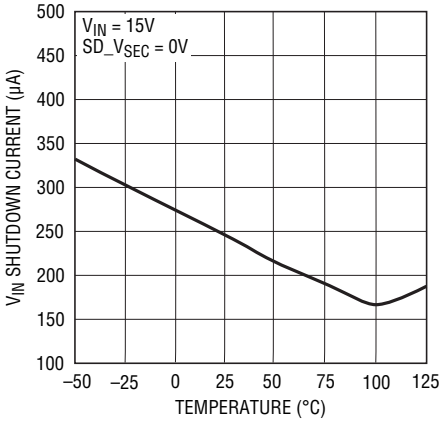
TYPICAL PERFORMANCE CHARACTERISTICS

Switching Frequency vs Temperature



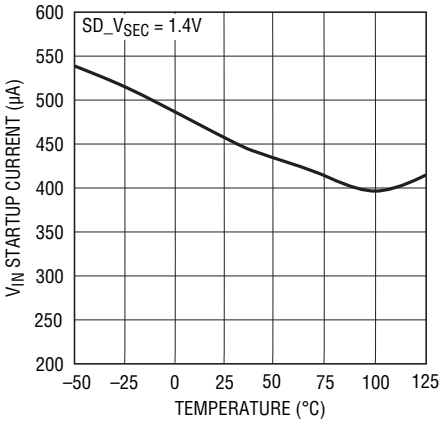
42692 G10

V_{IN} Shutdown Current vs Temperature



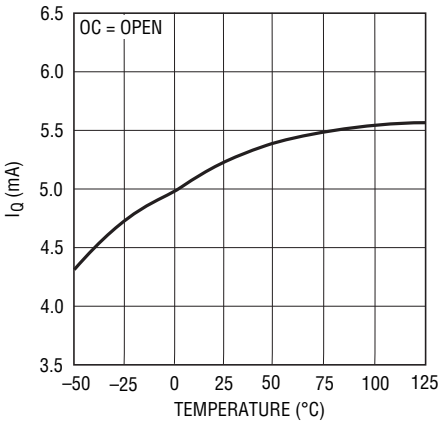
42692 G11

V_{IN} Start-Up Current vs Temperature



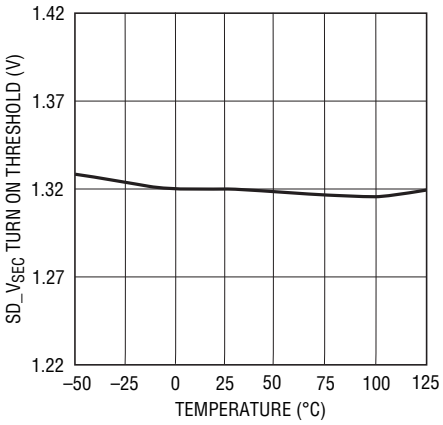
42692 G12

I_Q (V_{IN}) vs Temperature



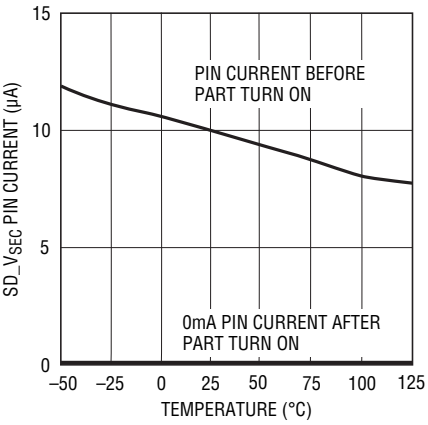
42692 G13

SD_V_{SEC} Turn On Threshold vs Temperature



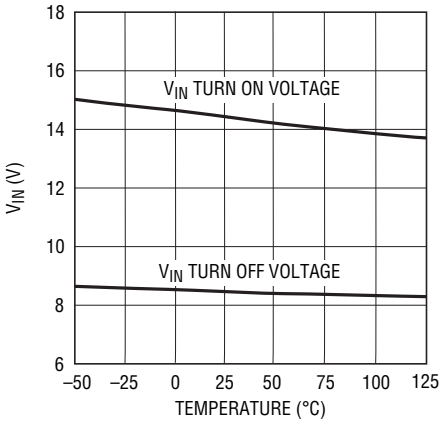
42692 G14

SD_V_{SEC} Pin Current vs Temperature



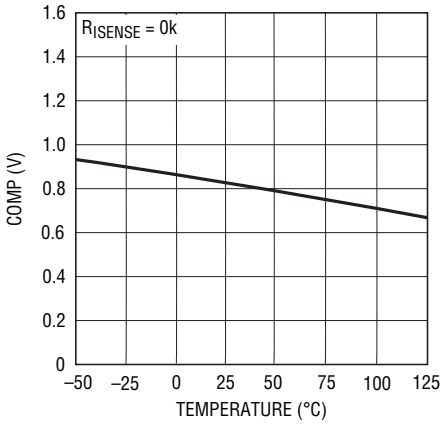
42692 G15

V_{IN} Turn On/Off Voltage vs Temperature



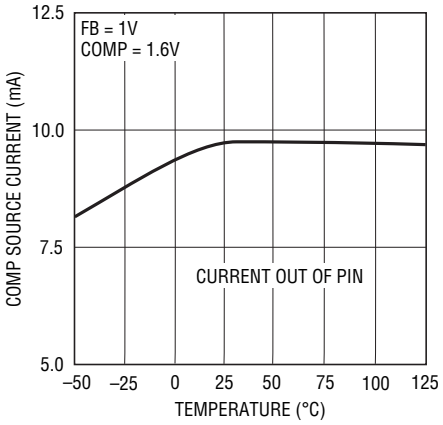
42692 G16

COMP Active Threshold vs Temperature



42692 G17

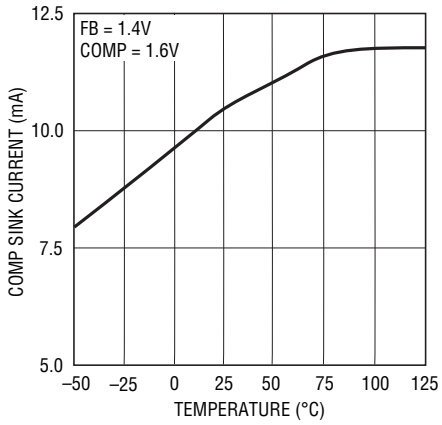
COMP Source Current vs Temperature



42692 G18

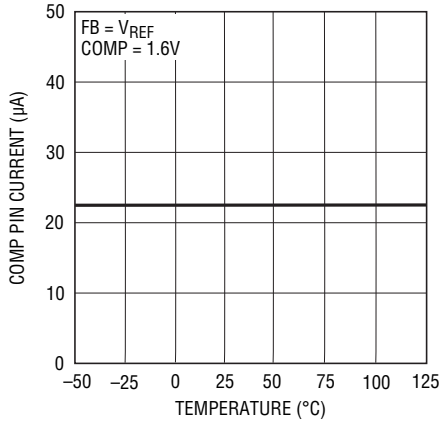
TYPICAL PERFORMANCE CHARACTERISTICS

COMP Sink Current vs Temperature



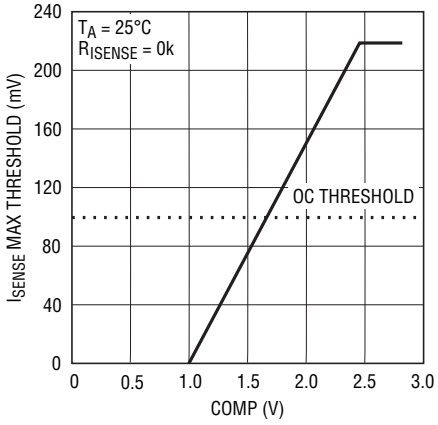
42692 G19

(Disabled) COMP Pin Current vs Temperature



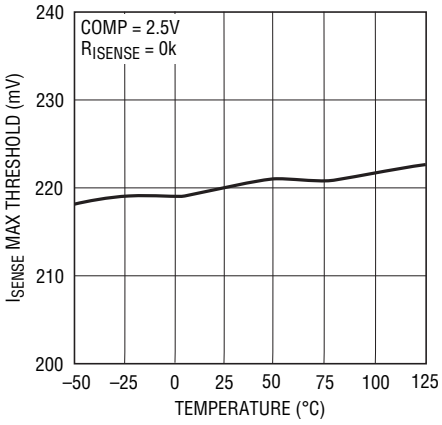
42692 G20

ISENSE Maximum Threshold vs COMP



42692 G21

ISENSE Maximum Threshold vs Temperature



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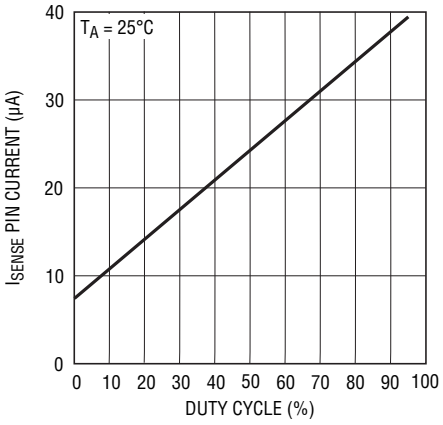
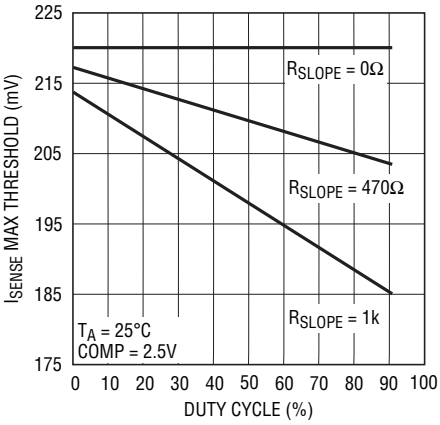
ISENSE Pin Current (Out of Pin) vs Duty Cycle



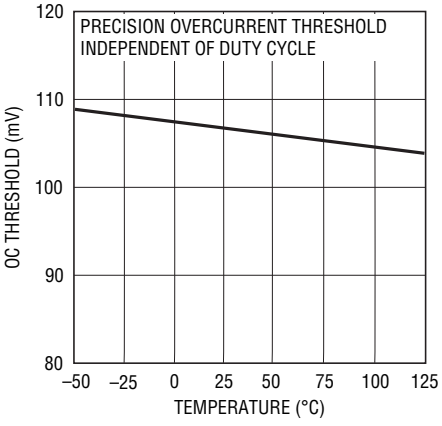
42692 G23

ISENSE Maximum Threshold vs Duty Cycle (Programming Slope Compensation)



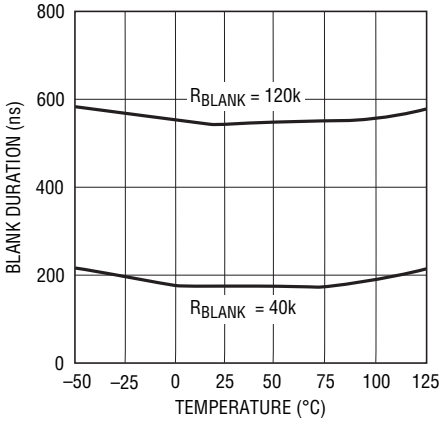
42692 G24

OC (Overcurrent) Threshold vs Temperature



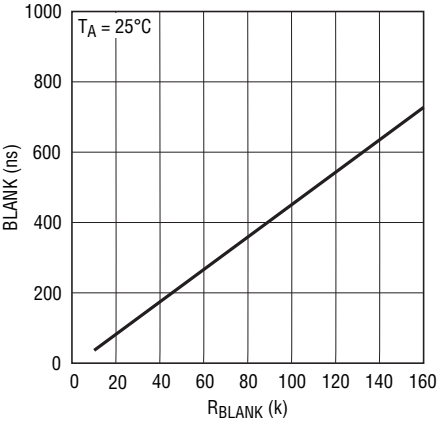
42692 G25

Blank Duration vs Temperature



42692 G26

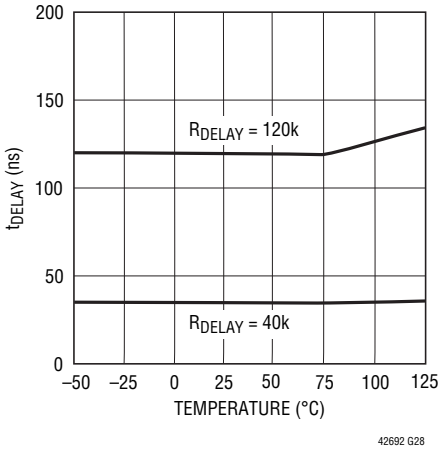
BLANK Duration vs RBLANK



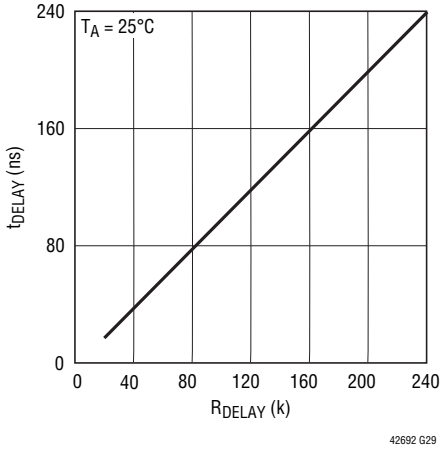
42692 G27

TYPICAL PERFORMANCE CHARACTERISTICS

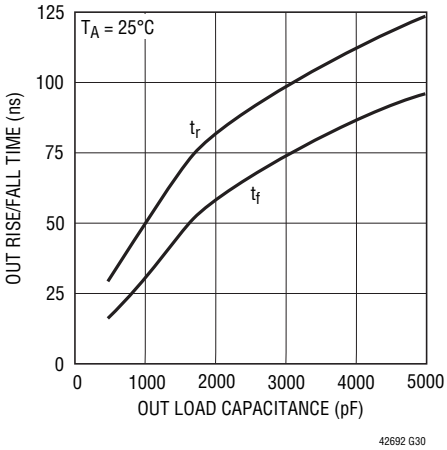
t_{DELAY}: SOUT Rise to OUT Rise vs Temperature



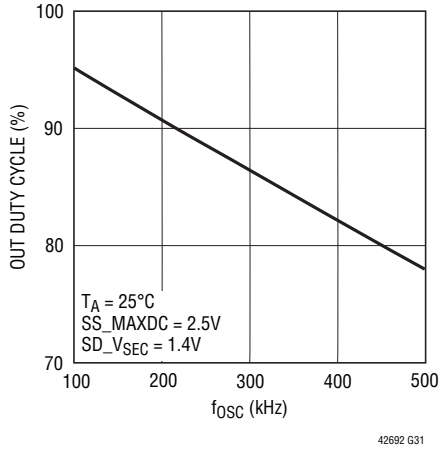
t_{DELAY}: SOUT Rise to OUT Rise vs R_{DELAY}



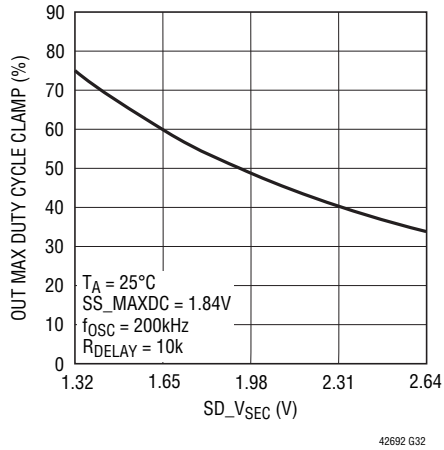
OUT Rise/Fall Time vs OUT Load Capacitance



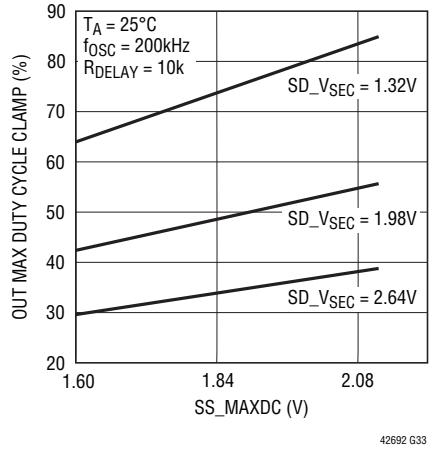
OUT: Max Duty Cycle vs f_{OSC}



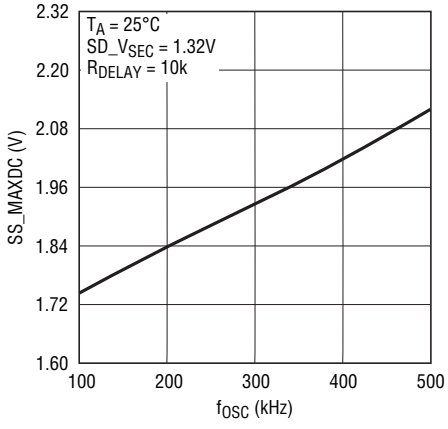
OUT: Max Duty Cycle CLAMP vs SD_V_{SEC}



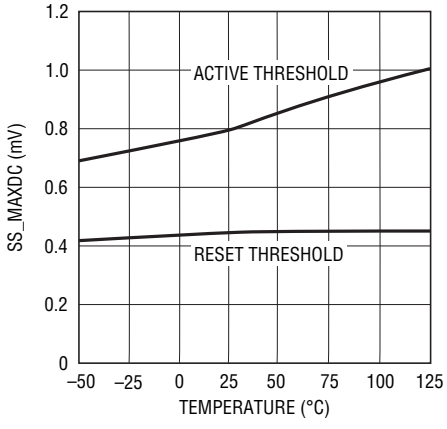
OUT: Max Duty Cycle CLAMP vs SS_MAXDC



SS_MAXDC Setting vs f_{OSC} (for OUT DC = 72%)



SS_MAXDC Reset and Active Thresholds vs Temperature



PIN FUNCTIONS

SHDN (Pin 1): Shutdown Input. Use this pin for auxiliary power application. Drive SHDN high to disable LTC4269-2 operation and corrupt the signature resistance. If unused, tie SHDN to V_{PORTN}.

$\overline{T2P}$ (Pin 2): Type-2 PSE Indicator, Open-Drain. Low impedance indicates the presence of a Type-2 PSE.

R_{CLASS} (Pin 3): Class Select Input. Connect a resistor between R_{CLASS} and V_{PORTN} to set the classification load current.

V_{PORTN} (Pins 5, 6): Power Input. Tie to the PD input through the diode bridge. Pins 5 and 6 must be electrically tied together at the package.

NC (Pins 4, 7, 8, 25, 30, 31): No Connect.

COMP (Pin 9): Output Pin of the Error Amplifier. The error amplifier is an op amp, allowing various compensation networks to be connected between the COMP pin and FB pin for optimum transient response in a nonisolated supply. The voltage on this pin corresponds to the peak current of the external FET. Full operating voltage range is between 0.8V and 2.5V corresponding to 0mV to 220mV at the I_{SENSE} pin. For applications using the 100mV OC pin for overcurrent detection, typical operating range for the COMP pin is 0.8V to 1.6V. For isolated applications where COMP is controlled by an opto-coupler, the COMP pin output drive can be disabled with FB = V_{REF}, reducing the COMP pin current to (COMP – 0.7)/40k.

FB (Pin 10): In a nonisolated supply, FB monitors the output voltage via an external resistor divider and is compared with an internal 1.23V reference by the error amplifier. FB connected to V_{REF} disables error amplifier output.

R_{OSC} (Pin11): A resistor to GND programs the operating frequency of the IC between 100kHz and 500kHz. Nominal voltage on the R_{OSC} pin is 1.0V.

SYNC (Pin 12): Used to synchronize the internal oscillator to an external signal. It is directly logic compatible and can be driven with any signal between 10% and 90% duty cycle. If unused, the pin should be connected to GND.

SS_MAXDC (Pin 13): The external resistor divider from V_{REF} sets the maximum duty cycle clamp (SS_MAXDC = 1.84V, SD_V_{SEC} = 1.32V gives 72% duty cycle). Capacitor on SS_MAXDC pin in combination with external resistor divider sets soft-start timing.

V_{REF} (Pin 14): The output of an internal 2.5V reference which supplies internal control circuitry. Capable of sourcing up to 2.5mA drive for external use. Bypass to GND with a 0.1µF ceramic capacitor.

SD_V_{SEC} (Pin 15): The SD_V_{SEC} pin, when pulled below its accurate 1.32V threshold, is used to turn off the IC and reduce current drain from V_{IN}. The SD_V_{SEC} pin is connected to system input voltage through a resistor divider to define undervoltage lockout (UVLO) for the power supply and to provide a volt-second clamp on the OUT pin. An 11µA pin current hysteresis allows external programming of UVLO hysteresis.

GND (Pin 16): Analog Ground. Tie to V_{NEG}.

BLANK (Pin 17): A resistor to GND adjusts the extended blanking period of the overcurrent and current sense amplifier outputs during FET turn-on—to prevent false current limit trip. Increasing the resistor value increases the blanking period.

I_{SENSE} (Pin 18): The Current Sense Input for the Control Loop. Connect this pin to the sense resistor in the source of the external power MOSFET. A resistor in series with the I_{SENSE} pin programs slope compensation.

PIN FUNCTIONS

OC (Pin 19): OC is an accurate 107mV threshold, independent of duty cycle, for overcurrent detection and trigger of soft-start. Connect this pin directly to the sense resistor in the source of the external power MOSFET.

DELAY (Pin 20): A resistor to GND adjusts the delay period between SOUT rising edge and OUT rising edge. Used to maximize efficiency in forward converter applications by adjusting the timing. Increasing the resistor value increases the delay period.

PGND (Pin 21): Power Ground. Carries the gate driver's return current. Tie to V_{NEG}.

OUT (Pin 22): Drives the gate of an N-channel MOSFET between 0V and V_{IN} with a maximum limit of 13V on OUT pin set by an internal clamp. Active pull-off exists in shutdown (see electrical specification).

V_{IN} (Pin 23): Input Supply for the Power Supply Controller. It must be closely decoupled to GND. An internal undervoltage lockout threshold exists for V_{IN} at approximately 14.25V on and 8.75V off.

SOUT (Pin 24): Switched Output in Phase with OUT Pin. Provides sync signal for control of secondary-side FETs in forward converter applications requiring highly efficient synchronous rectification. SOUT is actively clamped to 12V. Active pull-off exists in shutdown (see electrical specification). Can also be used to drive the active clamp FET of an active clamp forward supply.

V_{NEG} (Pins 26, 27): Power Output. Connects the PoE return line to the power supply through the internal Hot Swap power MOSFET. Pins 26 and 27 must be electrically tied together at the package.

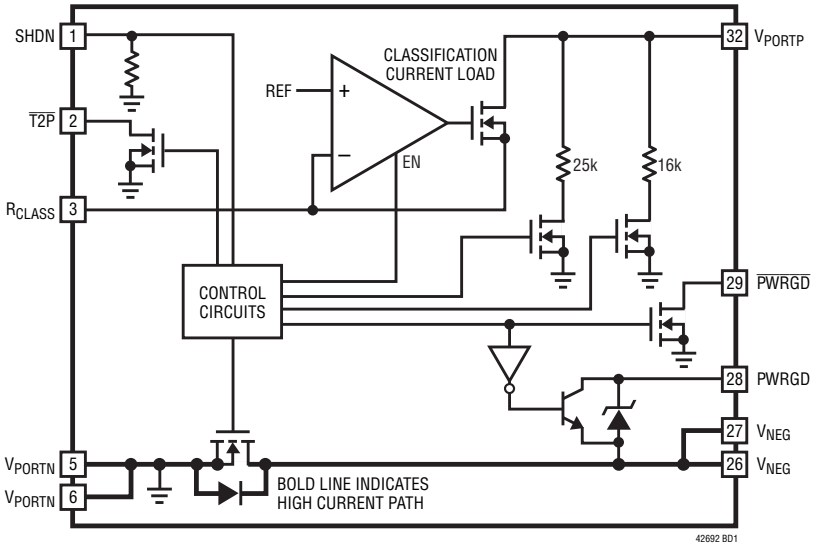
PWRGD (Pin 28): Active High Power Good Output, Open Collector. Signals that the internal Hot Swap MOSFET is on. High Impedance indicates power is good. PWRGD is referenced to V_{NEG} and is low impedance during inrush and in the event of thermal overload. PWRGD is clamped 14V above V_{NEG}.

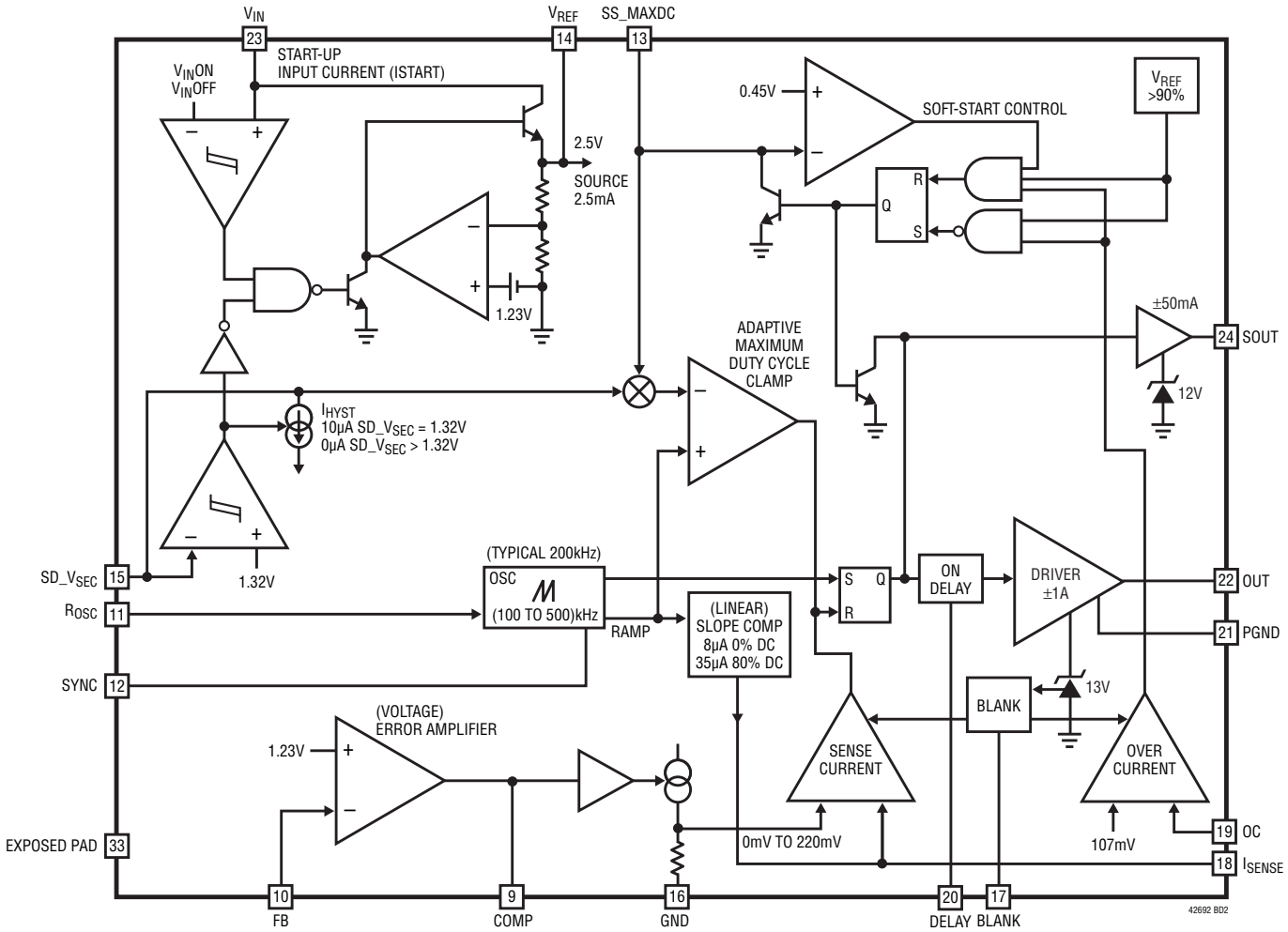
$\overline{\text{PWRGD}}$ (Pin 29): Active Low Power Good Output, Open Drain. Signals that the internal Hot Swap MOSFET is on. Low Impedance indicates power is good. $\overline{\text{PWRGD}}$ is referenced to V_{PORTN} and is high impedance during inrush and in the event of thermal overload. $\overline{\text{PWRGD}}$ has no internal clamps.

V_{PORTP} (Pin 32): Input Voltage Positive Rail. This pin is connected to the PD's positive rail.

Exposed Pad (Pin 33): Tie to GND and PCB heat sink.

BLOCK DIAGRAMS





APPLICATIONS INFORMATION

OVERVIEW

Power over Ethernet (PoE) continues to gain popularity as more products are taking advantage of having DC power and high speed data available from a single RJ45 connector. As PoE continues to grow in the marketplace, Powered Device (PD) equipment vendors are running into the 12.95W power limit established by the IEEE 802.3af standard.

The IEE802.3at standard establishes a higher power allocation for Power over Ethernet while maintaining backwards compatibility with the existing IEEE 802.3af systems. Power Sourcing Equipment (PSE) and Powered Devices are distinguished as Type 1 complying with the IEEE 802.3af power levels, or Type 2 complying with the IEEE 802.3at power levels. The maximum available power of a Type 2 PD is 25.5W.

The IEEE 802.3at standard also establishes a new method of acquiring power classification from a PD and communicating the presence of a Type 2 PSE. A Type 2 PSE has the option of acquiring PD power classification by performing 2-event classification (Layer 1) or by communicating with the PD over the data line (Layer 2). In turn, a Type 2 PD must be able to recognize both layers of communications and identify a Type 2 PSE.

The LTC4269-2 is specifically designed to support a PD that must operate under the IEEE 802.3at standard. In particular, the LTC4269-2 provides the $\overline{T2P}$ indicator bit which recognizes 2-event classification. This indicator bit may be used to alert the LTC4269-2 output load that a Type 2 PSE is present. With an internal signature resistor, classification circuitry, inrush control, and thermal shutdown, the LTC4269-2 is a complete PD interface solution capable of supporting in the next generation PD applications. In addition to the PD front end, the LTC4269-2 also incorporates a high efficiency synchronous forward controller that minimizes component sizes while maximizing output power.

MODES OF OPERATION

The LTC4269-2 has several modes of operation depending on the input voltage applied between the V_{PORTP} and V_{PORTN} pins. Figure 1 presents an illustration of voltage

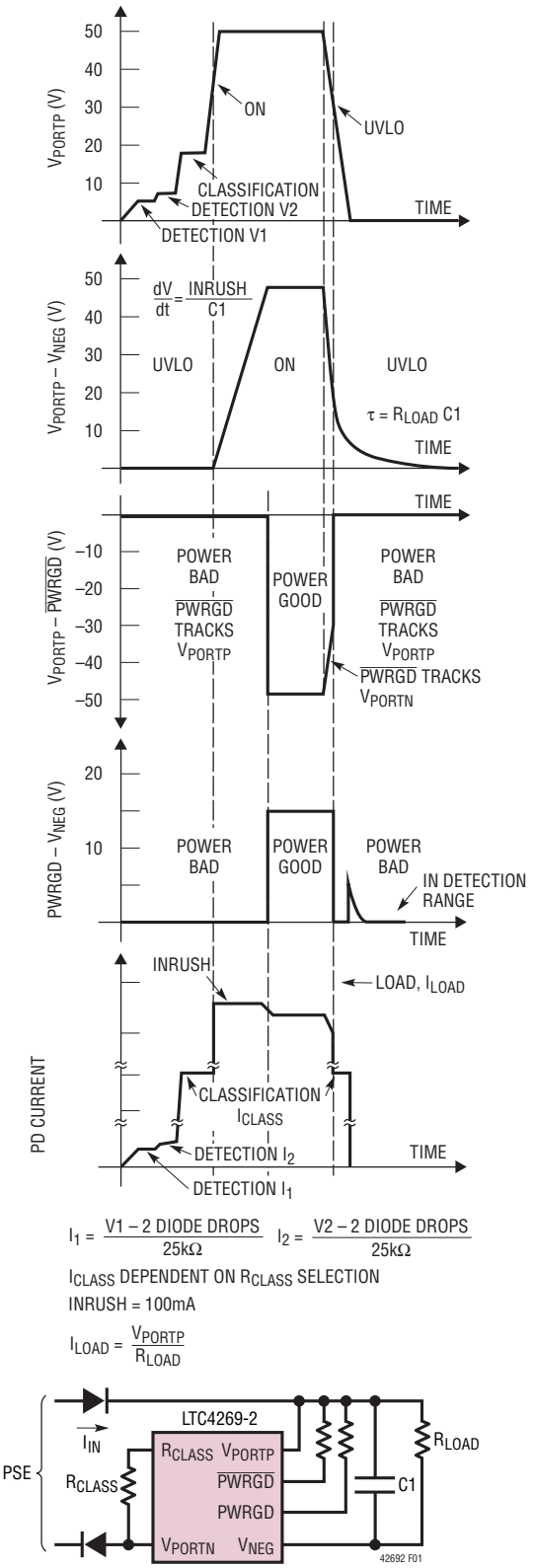


Figure 1. Output Voltage, $\overline{PWRGD}$, PWRGD and PD Current as a Function of Input Voltage

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and current waveforms the LTC4269-2 may encounter with the various modes of operation summarized in Table 1.

Table 1. LTC4269-2 Modes of Operation as a Function of Input Voltage

$V_{PORTP} – V_{PORTN}$ (V)	LTC4269-2 MODES OF OPERATION
0V to 1.4V	Inactive (Reset after 1st Classification Event)
1.5V to 9.8V (5.4V to 9.8V)	25k Signature Resistor Detection Before 1st Classification Event (Mark, 11k Signature Corrupt After 1st Classification Event)
12.5V to On/UVLO	Classification Load Current Active
On/UVLO to 60V	Inrush and Power Applied to PD Load
>71V	Overvoltage Lockout, Classification and Hot Swap are Disabled.

On/UVLO includes hysteresis. Rising input threshold: 37.2V max. Falling input threshold: 30.0V min.

These modes satisfy the requirements defined in the IEEE 802.3af/at specification.

INPUT DIODE BRIDGE

In the IEEE 802.3af/at standard, the modes of operation reference the input voltage at the PD's RJ45 connector. Since the PD must handle power received in either polarity from either the data or the spare pair, input diode bridges BR1 and BR2 are connected between the RJ45 connector and the LTC4269-2 (Figure 2).

The input diode bridge introduces a voltage drop that affects the range for each mode of operation. The LTC4269-2 compensates for these voltage drops so that a PD built with the LTC4269-2 meets the IEEE 802.3af/at-established voltage ranges. Note that the Electrical Specifications are referenced with respect to the LTC4269-2 package pins.

DETECTION

During detection, the PSE looks for a 25k signature resistor which identifies the device as a PD. The PSE will apply two voltages in the range of 2.8V to 10V and measures the corresponding currents. Figure 1 shows the detection voltages V1 and V2 and the corresponding PD current. The PSE calculates the signature resistance using the $\Delta V/\Delta I$ measurement technique.

The LTC4269-2 presents its precision, temperature-compensated 25k resistor between the V_{PORTP} and V_{PORTN} pins, alerting the PSE that a PD is present and requests power to be applied. The LTC4269-2 signature resistor also compensates for the additional series resistance introduced by the input diode bridge. Thus a PD built with the LTC4269-2 conforms to the IEEE 802.3af/at detection specifications.

SIGNATURE CORRUPT OPTION

In some designs that include an auxiliary power option, it is necessary to prevent a PD from being detected by a PSE. The LTC4269-2 signature resistance can be corrupted with the SHDN pin (Figure 3). Taking the SHDN pin high will reduce the signature resistor below 11k which is an invalid signature per the IEEE 802.3af/at specifications, and alerts the PSE not to apply power. Invoking the SHDN pin

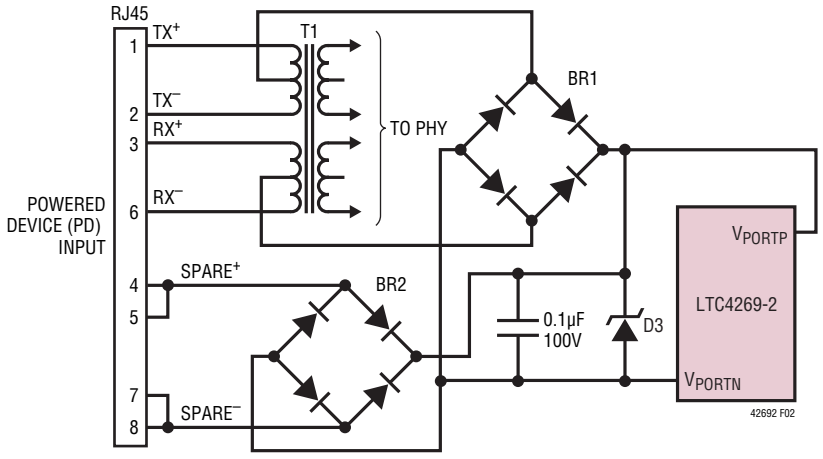

Figure 2. PD Front End Using Diode Bridge on Main and Spare Inputs

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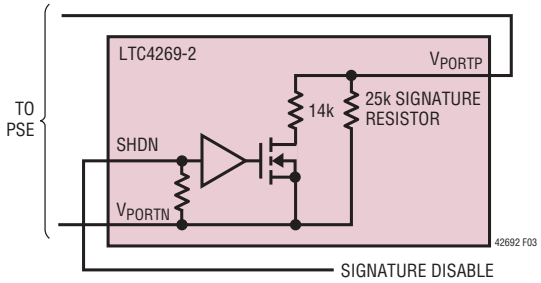

Figure 3. 25k Signature Resistor with Disable

also ceases operation for classification and turns off the internal Hot Swap FET. If this feature is not used, connect SHDN to V_{PORTN}.

CLASSIFICATION

Classification provides a method for more efficient power allocation by allowing the PSE to identify a PD power classification. Class 0 is included in the IEEE specification for PDs that don't support classification. Class 1-3 partitions PDs into three distinct power ranges. Class 4 includes the new power range under IEEE 802.3at (see Table 2).

During classification probing, the PSE presents a fixed voltage between 15.5V and 20.5V to the PD (Figure 1). The LTC4269-2 asserts a load current representing the PD power classification. The classification load current is programmed with a resistor R_{CLASS} that is chosen from Table 2.

Table 2. Summary of Power Classifications and LTC4269-2 R_{CLASS} Resistor Selection

CLASS	USAGE	MAXIMUM POWER LEVELS AT INPUT OF PD (W)	NOMINAL CLASSIFICATION LOAD CURRENT (mA)	LTC4269-2 R_{CLASS} RESISTOR (Ω, 1%)
0	Type 1	0.44 to 12.95	<0.4	Open
1	Type 1	0.44 to 3.84	10.5	124
2	Type 1	3.84 to 6.49	18.5	69.8
3	Type 1	6.49 to 12.95	28	45.3
4	Type 2	12.95 to 25.5	40	30.9

2-EVENT CLASSIFICATION AND THE $\overline{T2P}$ PIN

A Type 2 PSE may declare the availability of high power by performing a 2-event classification (Layer 1) or by communicating over the high speed data line (Layer 2). A Type 2 PD must recognize both layers of communication. Since Layer 2 communications takes place directly between the PSE and the PD, the LTC4269-2 concerns itself only with recognizing 2-event classification.

In 2-event classification, a Type 2 PSE probes for power classification twice. Figure 4 presents an example of a 2-event classification. The 1st classification event occurs

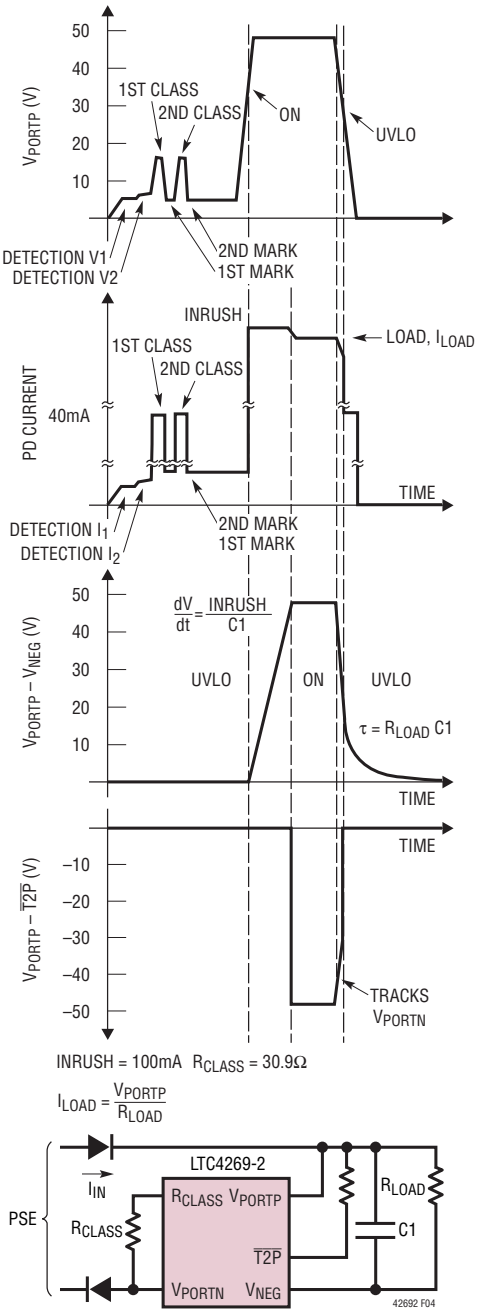

Figure 4. V_{NEG}, $\overline{T2P}$ and PD Current as a Result of 2-Event Classification

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when the PSE presents an input voltage between 15.5V to 20.5V and the LTC4269-2 presents a Class 4 load current. The PSE then drops the input voltage into the mark voltage range of 7V to 10V, signaling the 1st mark event. The PD in the mark voltage range presents a load current between 0.25mA to 4mA.

The PSE repeats this sequence, signaling the 2nd Classification and 2nd mark event occurrence. This alerts the LTC4269-2 that a Type 2 PSE is present. The Type 2 PSE then applies power to the PD and the LTC4269-2 charges up the reservoir capacitor C1 with a controlled inrush current. When C1 is fully charged, and the LTC4269-2 declares power good, the $\overline{T2P}$ pin presents an active low signal, or low impedance output with respect to V_{PORTN}. The $\overline{T2P}$ output becomes inactive when the LTC4269-2 input voltage falls below the PoE undervoltage lockout threshold.

SIGNATURE CORRUPT DURING MARK

As a member of the IEEE 802.3at working group, Linear noted that it is possible for a Type 2 PD to receive a false indication of a 2-event classification if a PSE port is precharged to a voltage above the detection voltage range before the first detection cycle. The IEEE working group modified the standard to prevent this possibility by requiring a Type 2 PD to corrupt the signature resistance during the mark event, alerting the PSE not to apply power. The LTC4269-2 conforms to this standard by internally corrupting the signature resistance. This also discharges the port before the PSE begins the next detection cycle.

PD STABILITY DURING CLASSIFICATION

Classification presents a challenging stability problem due to the wide range of possible classification load current. The onset of the classification load current introduces a voltage drop across the cable and increases the forward voltage of the input diode bridge. This may cause the PD to oscillate between detection and classification with the onset and removal of the classification load current.

The LTC4269-2 prevents this oscillation by introducing a voltage hysteresis window between the detection and classification ranges. The hysteresis window accommodates the voltage changes a PD encounters at the onset of the classification load current, thus providing a trouble-free transition between detection and classification modes.

The LTC4269-2 also maintains a positive I-V slope throughout the classification range up to the on voltage. In the event a PSE overshoots beyond the classification voltage range, the available load current aids in returning the PD back into the classification voltage range. (The PD input may otherwise be “trapped” by a reverse-biased diode bridge and the voltage held by the 0.1µF capacitor.)

INRUSH CURRENT

Once the PSE detects and optionally classifies the PD, the PSE then applies power to the PD. When the LTC4269-2 port voltage rises above the on voltage threshold, LTC4269-2 connects V_{NEG} to V_{PORTN} through the internal power MOSFET.

To control the power-on surge currents in the system, the LTC4269-2 provides a fixed inrush current, allowing C1 to ramp up to the line voltage in a controlled manner.

The LTC4269-2 keeps the PD inrush current below the PSE current limit to provide a well-controlled power-up characteristic that is independent of the PSE behavior. This ensures a PD using the LTC4269-2 interoperability with any PSE.

POE UNDERVOLTAGE LOCKOUT

The IEEE 802.3af/at specification for the PD dictates a maximum turn-on voltage of 42V and a minimum turn-off voltage of 30V. This specification provides an adequate voltage to begin PD operation, and to discontinue PD operation when the port voltage is too low. In addition, this specification allows PD designs to incorporate an on-off hysteresis window to prevent start-up oscillations.

The LTC4269-2 features a PoE undervoltage lockout (UVLO) hysteresis window (See Figure 5) that conforms with the IEEE 802.3af/at specification and accommodates the voltage drop in the cable and input diode bridge at the onset of the inrush current.

Once C1 is fully charged, the LTC4269-2 turns on its internal MOSFET and passes power to the PD. The LTC4269-2

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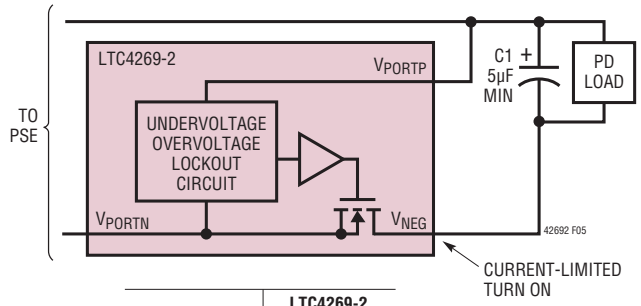

$V_{PORTP} - V_{PORTN}$	LTC4269-2 POWER MOSFET
0V TO ON*	OFF
>ON*	ON
<UVLO*	OFF
>OVLO	OFF

*INCLUDES ON-UVLO HYSTERESIS
ON THRESHOLD ≅ 36.1V
UVLO THRESHOLD ≅ 30.7V
OVLO THRESHOLD ≅ 71.0V

Figure 5. LTC4269-2 Undervoltage and Overvoltage Lockout

continues to power the PD load as long as the port voltage does not fall below the UVLO threshold. When the LTC4269-2 port voltage falls below the UVLO threshold, the PD is disconnected, and classification mode resumes. C1 discharges through the LTC4269-2 circuitry.

COMPLEMENTARY POWER GOOD

When LTC4269-2 fully charges the load capacitor (C1), power good is declared and the LTC4269-2 load can safely begin operation. The LTC4269-2 provides complementary power good signals that remain active during normal operation and are deasserted when the port voltage falls below the PoE UVLO threshold, when the voltage exceeds the overvoltage lockout (OVLO) threshold, or in the event of a thermal shutdown. See Figure 6.

The PWRGD pin features an open-collector output referenced to V_{NEG} which can interface directly with the SD_V_{SEC} pin. When power good is declared and active, the PWRGD pin is high impedance with respect to V_{NEG}. An internal 14V clamp limits the PWRGD pin voltage. Connecting the PWRGD pin to the SD_V_{SEC} pin prevents the DC/DC converter from commencing operation before the PDI interface completely charges the reservoir capacitor, C1.

The active low $\overline{PWRGD}$ pin connects to an internal, open-drain MOSFET referenced to V_{PORTN} and can interface directly to the shutdown pin of a DC/DC converter product.

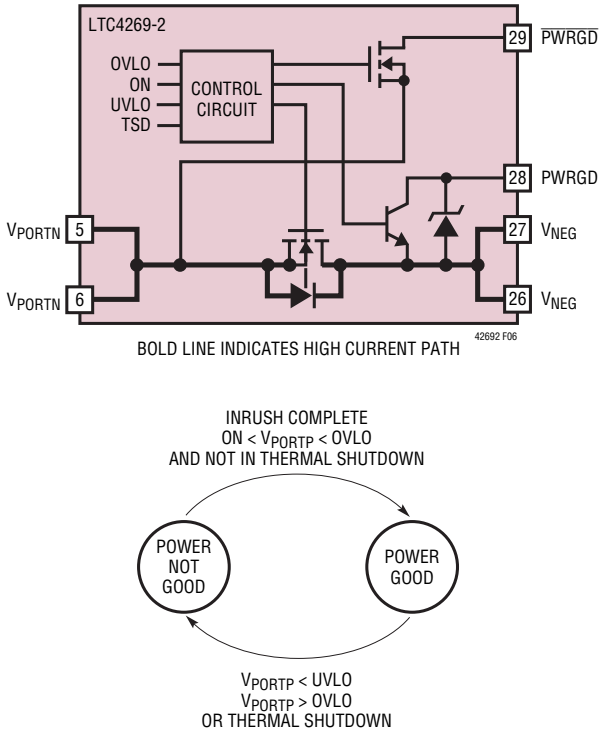

Figure 6. LTC4269-2 Power Good Functional and State Diagram

When power good is declared and active, the $\overline{PWRGD}$ pin is low impedance with respect to V_{PORTN}.

PWRGD PIN WHEN SHDN IS INVOKED

In PD applications where an auxiliary power supply invokes the SHDN feature, the PWRGD pin becomes high impedance. This prevents the PWRGD pin that is connected to the "RUN" pin of the DC/DC converter from interfering with the DC/DC converter operations when powered by an auxiliary power supply.

OVERVOLTAGE LOCKOUT

The LTC4269-2 includes an Overvoltage Lockout (OVLO) feature (Figure 5) which protects the LTC4269-2 and its load from an overvoltage event. If the input voltage exceeds the OVLO threshold, the LTC4269-2 discontinues PD operation. Normal operations resume when the input voltage falls below the OVLO threshold and when C1 is charged up.

APPLICATIONS INFORMATION

THERMAL PROTECTION

The IEEE 802.3af/at specification requires a PD to withstand any applied voltage from 0V to 57V indefinitely. However, there are several possible scenarios where a PD may encounter excessive heating.

During classification, excessive heating may occur if the PSE exceeds the 75ms probing time limit. At turn-on, when the load capacitor begins to charge, the instantaneous power dissipated by the PD interface can be large before it reaches the line voltage. And if the PD experiences a fast input positive voltage step in its operational mode (for example, from 37V to 57V), the instantaneous power dissipated by the PD Interface can be large.

The LTC4269-2 includes a thermal protection feature which protects the LTC4269-2 from excessive heating. If the LTC4269-2 junction temperature exceeds the overtemperature threshold, the LTC4269-2 discontinues PD operations. Normal operation resumes when the junction temperature falls below the overtemperature threshold and when C1 is charged up and power good becomes inactive.

EXTERNAL INTERFACE AND COMPONENT SELECTION

Transformer

Nodes on an Ethernet network commonly interface to the outside world via an isolation transformer. For PDs, the isolation transformer must also include a center tap on the RJ45 connector side (see Figure 7).

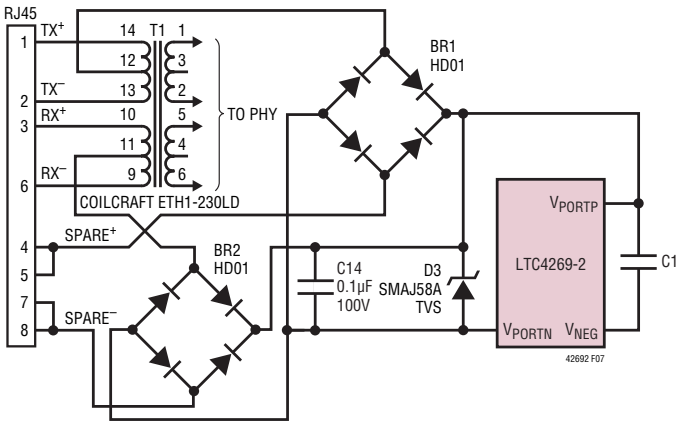

Figure 7. PD Front End with Isolation Transformer, Diode Bridges, Capacitors and a Transient Voltage Suppressor (TVS)

The increased current levels in a Type 2 PD over a Type 1 increase the current imbalance in the magnetics which can interfere with data transmission. In addition, proper termination is also required around the transformer to provide correct impedance matching and to avoid radiated and conducted emissions. Transformer vendors such as Bel Fuse, Coilcraft, Halo, Pulse and Tyco (Table 4) can assist in selecting an appropriate isolation transformer and proper termination methods.

Table 4. Power over Ethernet Transformer Vendors

VENDOR	CONTACT INFORMATION
Bel Fuse Inc.	206 Van Vorst Street Jersey City, NJ 07302 Tel: 201-432-0463 www.belfuse.com
Coilcraft Inc.	1102 Silver Lake Road Gary, IL 60013 Tel: 847-639-6400 www.coilcraft.com
Halo Electronics	1861 Landings Drive Mountain View, CA 94043 Tel: 650-903-3800 www.haloelectronics.com
PCA Electronics	16799 Schoenborn Street North Hills, CA 91343 Tel: 818-892-0761 www.pca.com
Pulse Engineering	12220 World Trade Drive San Diego, CA 92128 Tel: 858-674-8100 www.pulseeng.com
Tyco Electronics	308 Constitution Drive Menlo Park, CA 94025-1164 Tel: 800-227-7040 www.circuitprotection.com

Input Diode Bridge

Figure 2 shows how two diode bridges are typically connected in a PD application. One bridge is dedicated to the data pair while the other bridge is dedicated to the spare pair. The LTC4269-2 supports the use of either silicon or Schottky input diode bridges. However, there are trade-offs in the choice of diode bridges.

An input diode bridge must be rated above the maximum current the PD application will encounter at the temperature the PD will operate. Diode bridge vendors typically call out the operating current at room temperature, but derate the maximum current with increasing temperature. Consult the diode bridge vendors for the operating current de-rating curve.

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A silicon diode bridge can consume over 4% of the available power in some PD applications. Using Schottky diodes can help reduce the power loss with a lower forward voltage.

A Schottky bridge may not be suitable for some high temperature PD applications. The leakage current has a temperature and voltage dependency that can reduce the perceived signature resistance. In addition, the IEEE 802.3af/at specification mandates the leakage back-feeding through the unused bridge cannot generate more than 2.8V across a 100k resistor when a PD is powered with 57V.

Sharing Input Diode Bridges

At higher temperatures, a PD design may be forced to consider larger bridges in a bigger package because the maximum operating current for the input diode bridge is drastically derated. The larger package may not be acceptable in some space-limited environments.

One solution to consider is to reconnect the diode bridges so that only one of the four diodes conducts current in each package. This configuration extends the maximum operating current while maintaining a smaller package profile. Figure 7 shows how the reconnect the two diode bridges. Consult the diode bridge vendors for the de-rating curve when only one of four diodes is in operation.

Input Capacitor

The IEEE 802.3af/at standard includes an impedance requirement in order to implement the AC disconnect function. A 0.1µF capacitor (C14 in Figure 7) is used to meet this AC impedance requirement. Place this capacitor as close to the LTC4269-2 as possible.

Transient Voltage Suppressor

The LTC4269-2 specifies an absolute maximum voltage of 100V and is designed to tolerate brief overvoltage events. However, the pins that interface to the outside world can routinely see excessive peak voltages. To protect the LTC4269-2, install a transient voltage suppressor (D3) between the input diode bridge and the LTC4269-2 as close to the LTC4269-2 as possible as shown in Figure 7.

Classification Resistor (R_{CLASS})

The R_{CLASS} resistor sets the classification load current, corresponding to the PD power classification. Select the value of R_{CLASS} from Table 2 and connect the resistor between the R_{CLASS} and V_{PORTN} pins as shown in Figure 4, or float the R_{CLASS} pin if the classification load current is not required. The resistor tolerance must be 1% or better to avoid degrading the overall accuracy of the classification circuit.

Load Capacitor

The IEEE 802.3af/at specification requires that the PD maintains a minimum load capacitance of 5µF and does not specify a maximum load capacitor. However, if the load capacitor is too large, there may be a problem with inadvertent power shutdown by the PSE.

This occurs when the PSE voltage drops quickly. The input diode bridge reverses bias, and the PD load momentarily powers off the load capacitor. If the PD does not draw power within the PSE's 300ms disconnection delay, the PSE may remove power from the PD. Thus, it is necessary to evaluate the load current and capacitance to ensure that an inadvertent shutdown cannot occur.

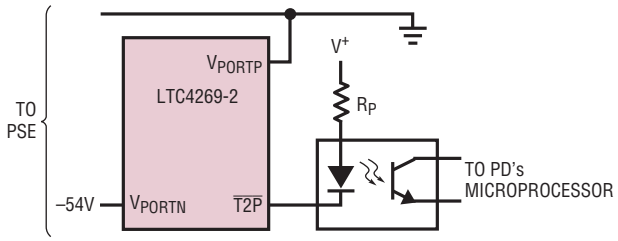
The load capacitor can store significant energy when fully charged. The PD design must ensure that this energy is not inadvertently dissipated in the LTC4269-2. For example, if the V_{PORTP} pin shorts to V_{PORTN} while the capacitor is charged, current will flow through the parasitic body diode of the internal MOSFET and may cause permanent damage to the LTC4269-2.

$\overline{T2P}$ Interface

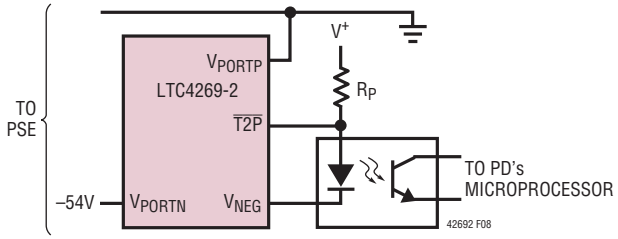
When a 2-event classification sequence successfully completes, the LTC4269-2 recognizes this sequence, and provides an indicator bit, declaring the presence of a Type 2 PSE. The open-drain output provides the option to use this signal to communicate to the LTC4269-2 load, or to leave the pin unconnected.

Figure 8 shows two interface options using the $\overline{T2P}$ pin and the opto-isolator. The $\overline{T2P}$ pin is active low and connects to an optoisolater to communicate across the

APPLICATIONS INFORMATION



OPTION 1: SERIES CONFIGURATION FOR ACTIVE LOW/LOW IMPEDANCE OUTPUT



OPTION 2: SHUNT CONFIGURATION FOR ACTIVE HIGH/OPEN COLLECTOR OUTPUT

Figure 8. $\overline{T2P}$ Interface Examples

DC/DC converter isolation barrier. The pull-up resistor R_P is sized according to the requirements of the opto-isolator operating current, the pull-down capability of the $\overline{T2P}$ pin, and the choice of V^+. V^+ for example can come from the PoE supply rail (which the LTC4269-2 V_{PORTP} is tied to), or from the voltage source that supplies power to the DC/DC converter. Option 1 has the advantage of not drawing power unless $\overline{T2P}$ is declared active.

Shutdown Interface

To corrupt the signature resistance, the SHDN pin can be driven high with respect to V_{PORTN}. If unused, connect SHDN directly to V_{PORTN}.

Exposed Pad

The LTC4269-2 uses a thermally enhanced DFN12 package that includes an Exposed Pad. The Exposed Pad should be electrically connected to the GND pin's PCB copper plane. This plane should be large enough to serve as the heat sink for the LTC4269-2.

Auxiliary Power Source

In some applications, it is desirable to power the PD from an auxiliary power source such as a wall adapter. Auxiliary power can be injected into the PD at several locations with priority chosen between PoE or auxiliary power sources. These options come with various trade-offs and design considerations. Contact Linear Technology applications support for detailed information on implementing custom auxiliary power sources.

IEEE 802.3AT SYSTEM POWER-UP REQUIREMENT

Under the IEEE 802.3at standard, a PD must operate under 12.95W in accordance with IEEE 802.3at standard until it recognizes a Type 2 PSE. Initializing PD operation in 12.95W mode eliminates interoperability issue in case a Type 2 PD connects to a Type 1 PSE. Once the PD recognizes a Type 2 PSE, the IEEE 802.3at standard requires the PD to wait 80ms in 12.95W operation before 25.5W operation can commence.

MAINTAIN POWER SIGNATURE

In an IEEE 802.3af/at system, the PSE uses the maintain power signature (MPS) to determine if a PD continues to require power. The MPS requires the PD to periodically draw at least 10mA and also have an AC impedance less than 26.25k in parallel with 0.05µF. If one of these conditions is not met, the PSE may disconnect power to the PD.

Isolation

The 802.3 standard requires Ethernet ports to be electrically isolated from all other conductors that are user accessible. This includes the metal chassis, other connectors, and any auxiliary power connection. For PDs, there are two common methods to meet the isolation requirement. If there are any user-accessible connections to the PD, then an isolated DC/DC converter is necessary to meet the isolation requirements. If user connections can be avoided, then it is possible to meet the safety requirement by completely enclosing the PD in an insulated housing.

Switcher Controller Operation

The LTC4269-2 has a current mode synchronous PWM controller optimized for control of a forward converter topology. The LTC4269-2 is ideal for power systems where very high efficiency and reliability, low complexity and cost are required in a small space. Key features of the LTC4269-2 include an adaptive maximum duty cycle clamp.

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An additional output signal is included for synchronous rectifier control or active clamp control. A precision 107mV threshold senses overcurrent conditions and triggers soft-start for low stress short-circuit protection and control. The key functions of the LTC4269-2 PWM controller are shown in the Block Diagrams.

Part Start-Up

In normal operation, the SD_V_{SEC} pin must exceed 1.32V and the V_{IN} pin must exceed 14.25V to allow the part to turn on. This combination of pin voltages allows the 2.5V V_{REF} pin to become active, supplying the LTC4269-2 control circuitry and providing up to 2.5mA external drive. SD_V_{SEC} threshold can be used for externally programming the power supply undervoltage lockout (UVLO) threshold on the input voltage to the forward converter. Hysteresis on the UVLO threshold can also be programmed since the SD_V_{SEC} pin draws 11µA just before part turn-on and 0µA after part turn-on.

With the LTC4269-2 turned on, the V_{IN} pin can drop as low as 8.75V before part shutdown occurs. This V_{IN} pin hysteresis (5.5V) combined with low 460µA start-up input current allows low power start-up using a resistor/capacitor network from power supply input voltage to supply the V_{IN} pin (Figure 10). The V_{IN} capacitor value is chosen to prevent V_{IN} falling below its turn-off threshold before a bias winding in the converter takes over supply to the V_{IN} pin.

Output Drivers

The LTC4269-2 has two outputs, SOUT and OUT. The OUT pin provides a ±1A peak MOSFET gate drive clamped to 13V. The SOUT pin has a ±50mA peak drive clamped to 12V and provides sync signal timing for synchronous rectification control or active clamp control.

For SOUT and OUT turn-on, a PWM latch is set at the start of each main oscillator cycle. OUT turn-on is delayed from SOUT turn-on by a time, t_{DELAY} (Figure 14). t_{DELAY} is programmed using a resistor from the DELAY pin to GND and is used to set the timing control of the secondary synchronous rectifiers for optimum efficiency.

SOUT and OUT turn off at the same time each cycle by one of three methods:

(1) MOSFET peak current sense at I_{SENSE} pin

(2) Adaptive maximum duty cycle clamp reached during load/line transients

(3) Maximum duty cycle reset of the PWM latch

During any of the following conditions—low V_{IN}, low SD_V_{SEC} or overcurrent detection at the OC pin—a soft-start event is latched and both SOUT and OUT turn off immediately (Figure 11).

Leading Edge Blanking

To prevent MOSFET switching noise causing premature turn-off of SOUT or OUT, programmable leading edge blanking exists. This means both the current sense comparator and overcurrent comparator outputs are ignored during MOSFET turn-on and for an extended period after the OUT leading edge (Figure 12). The extended blanking period is programmable by adjusting a resistor from the BLANK pin to GND.

Adaptive Maximum Duty Cycle Clamp (Volt-Second Clamp)

For forward converter applications, a maximum switch duty cycle clamp which adapts to transformer input voltage is necessary for reliable control of the MOSFET. This volt-second clamp provides a safeguard for transformer reset that prevents transformer saturation. Instantaneous load changes can cause the converter loop to demand maximum duty cycle. If the maximum duty cycle of the switch is too great, the transformer reset voltage can exceed the voltage rating of the primary-side MOSFETs with catastrophic damage. Many converters solve this problem by limiting the operational duty cycle of the MOSFET to 50% or less—or by using a fixed (non-adaptive) maximum duty cycle clamp with very large voltage rated MOSFETs. The LTC4269-2 provides a volt-second clamp to allow MOSFET duty cycles well above 50%. This gives greater power utilization for the MOSFETs, rectifiers and transformer resulting in less space for a given power output. In addition, the volt-second clamp can allow a reduced voltage rating on the MOSFET resulting in lower $R_{DS(ON)}$ for greater efficiency. The volt-second clamp defines a maximum duty cycle 'guard rail' which falls when power supply input voltage increases.

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An increase of voltage at the SD_V_{SEC} pin causes the maximum duty cycle clamp to decrease. If SD_V_{SEC} is resistively divided down from power supply input voltage, a volt-second clamp is realized. To adjust the initial maximum duty cycle clamp, the SS_MAXDC pin voltage is programmed by a resistor divider from the 2.5V V_{REF} pin to GND. An increase of programmed voltage on SS_MAXDC pin provides an increase of switch maximum duty cycle clamp.

Soft-Start

The LTC4269-2 provides true PWM soft-start by using the SS_MAXDC pin to control soft-start timing. The proportional relationship between SS_MAXDC voltage and switch maximum duty cycle clamp allows the SS_MAXDC pin to slowly ramp output voltage by ramping the maximum switch duty cycle clamp—until switch duty cycle clamp seamlessly meets the natural duty cycle of the converter. A soft-start event is triggered whenever V_{IN} is too low, SD_V_{SEC} is too low (power supply UVLO), or a 107mV overcurrent threshold at OC pin is exceeded. Whenever a soft-start event is triggered, switching at SOUT and OUT is stopped immediately.

The SS_MAXDC pin is discharged and only released for charging when it has fallen below its reset threshold of 0.45V and all faults have been removed. Increasing voltage on the SS_MAXDC pin above 0.8V will increase switch maximum duty cycle. A capacitor to GND on the SS_MAXDC pin in combination with a resistor divider from V_{REF}, defines the soft-start timing.

Current Mode Topology (I_{SENSE} Pin)

The LTC4269-2 current mode topology eases frequency compensation requirements because the output inductor does not contribute to phase delay in the regulator loop. This current mode technique means that the error amplifier (nonisolated applications) or the opto-coupler (isolated applications) commands current (rather than voltage) to be delivered to the output. This makes frequency compensation easier and provides faster loop response to output load transients.

A resistor divider from the application's output voltage generates a voltage at the inverting FB input of the LTC4269-2 error amplifier (or to the input of an external opto-coupler) and is compared to an accurate reference (1.23V for LTC4269-2). The error amplifier output (COMP) defines the input threshold (I_{SENSE}) of the current sense comparator. COMP voltages between 0.8V (active threshold) and 2.5V define a maximum I_{SENSE} threshold from 0mV to 220mV. By connecting I_{SENSE} to a sense resistor in series with the source of an external power MOSFET, the MOSFET peak current trip point (turn off) can be controlled by COMP level and hence by the output voltage. An increase in output load current causing the output voltage to fall, will cause COMP to rise, increasing I_{SENSE} threshold, increasing the current delivered to the output. For isolated applications, the error amplifier COMP output can be disabled to allow the opto-coupler to take control. Setting FB = V_{REF} disables the error amplifier COMP output, reducing pin current to (COMP – 0.7)/40k.

Slope Compensation

The current mode architecture requires slope compensation to be added to the current sensing loop to prevent subharmonic oscillations which can occur for duty cycles above 50%. Unlike most current mode converters which have a slope compensation ramp that is fixed internally, placing a constraint on inductor value and operating frequency, the LTC4269-2 has externally adjustable slope compensation. Slope compensation can be programmed by inserting an external resistor (R_{SLOPE}) in series with the I_{SENSE} pin. The LTC4269-2 has a linear slope compensation ramp which sources current out of the I_{SENSE} pin of approximately 8µA at 0% duty cycle to 35µA at 80% duty cycle.

Overcurrent Detection and Soft-Start (OC Pin)

An added feature to the LTC4269-2 is a precise 107mV sense threshold at the OC pin used to detect overcurrent conditions in the converter and set a soft-start latch. The OC pin is connected directly to the source of the primary-side MOSFET to monitor peak current in the MOSFET (Figure 13). The 107mV threshold is constant over the entire duty cycle range of the converter because it is unaffected by the slope compensation added to the I_{SENSE} pin.

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Synchronizing

A SYNC pin allows the LTC4269-2 oscillator to be synchronized to an external clock. The SYNC pin can be driven from a logic-level output, requiring less than 0.8V for a logic-level low and greater than 2.2V for a logic-level high. Duty cycle should run between 10% and 90%. To avoid loss of slope compensation during synchronization, the free running oscillator frequency, f_{OSC}, should be programmed to 80% of the external clock frequency (f_{SYNC}). The R_{SLOPE} resistor chosen for nonsynchronized operation should be increased by 1.25x (= f_{SYNC}/f_{OSC}).

Shutdown and Programming the Power Supply Undervoltage Lockout

The LTC4269-2 has an accurate 1.32V shutdown threshold at the SD_V_{SEC} pin. This threshold can be used in conjunction with a resistor divider to define the power supply undervoltage lockout threshold (UVLO) of the power supply input voltage (V_S) (Figure 9). A pin current hysteresis (11µA before part turn-on, 0µA after part turn-on) allows power supply UVLO hysteresis to be programmed. Calculation of the on/off thresholds for the power supply input voltage can be made as follows:

$V_{S(OFF)}$ Threshold = 1.32[1 + (R1/R2)]

$V_{S(ON)}$ Threshold = $V_{S(OFF)}$ + (11µA • R1)

Connect the PWRGD pin to the resistive divider network at the SD_V_{SEC} pin to prevent the DC/DC converter from starting before the PD interface completely charges the reservoir capacitor, C1 (Figure 9).

The SD_V_{SEC} pin must not be left open since there must be an external source current >11µA to lift the pin past its 1.32V threshold for part turn-on.

Micropower Start-Up: Selection of Start-Up Resistor and Capacitor for V_{IN}

The LTC4269-2 uses turn-on voltage hysteresis at the V_{IN} pin and low start-up current to allow micropower start-up (Figure 10). The LTC4269-2 monitors V_{IN} pin voltage to allow the part to turn-on at 14.25V and the part to turn-off at 8.75V. Low start-up current (460µA) allows a large resistor to be connected between the power supply input supply and V_{IN}. Once the part is turned on, input current

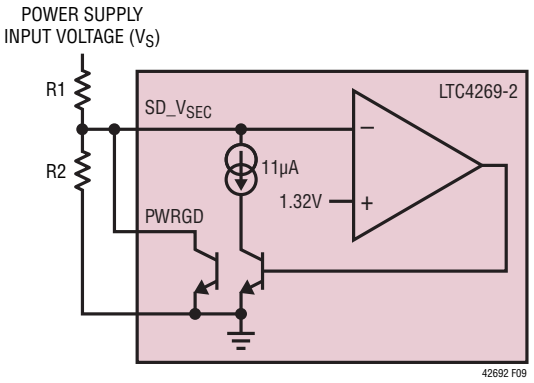

Figure 9. Programming Power Supply Undervoltage Lockout (UVLO)

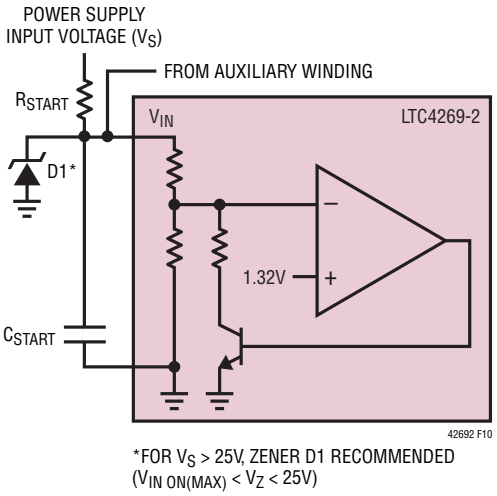

Figure 10. Low Power Start-Up

increases to drive the IC (5.2mA) and the output drivers (I_{DRIVE}). A large enough capacitor is chosen at the V_{IN} pin to prevent V_{IN} falling below its turn-off threshold before a bias winding in the converter takes over supply to V_{IN}. This technique allows a simple resistor/capacitor for start-up which draws low power from the system supply to the converter.

For system input voltages exceeding the absolute maximum rating of the LTC4269-2 V_{IN} pin, an external Zener should be connected from the V_{IN} pin to GND. This covers the condition where V_{IN} charges past $V_{IN(ON)}$ but the part does not turn on because SD_V_{SEC} < 1.32V. In this condition, V_{IN} will continue to charge towards system V_{IN}, possibly exceeding the rating for the V_{IN} pin. The Zener voltage should obey $V_{IN(ONMAX)} < V_Z < 25V$.

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Programming Oscillator Frequency

The oscillator frequency (f_{OSC}) of the LTC4269-2 is programmed using an external resistor, R_{OSC}, connected between the R_{OSC} pin and GND. Figure 11 shows typical f_{OSC} vs R_{OSC} resistor values. The LTC4269-2 free-running oscillator frequency is programmable in the range of 100kHz to 500kHz.

Stray capacitance and potential noise pickup on the R_{OSC} pin should be minimized by placing the R_{OSC} resistor as close as possible to the R_{OSC} pin and keeping the area of the R_{OSC} node as small as possible. The ground side of the R_{OSC} resistor should be returned directly to the (analog ground) GND pin. R_{OSC} can be calculated by:

$$R_{OSC} = 9.125k\ [(4100k/f_{OSC}) - 1]$$

Programming Leading Edge Blank Time

For PWM controllers driving external MOSFETs, noise can be generated at the source of the MOSFET during gate rise time and some time thereafter. This noise can potentially exceed the OC and I_{SENSE} pin thresholds of the LTC4269-2 to cause premature turn-off of SOUT and OUT pins in addition to false trigger of soft-start. The LTC4269-2 provides a programmable leading edge blanking of the OC and I_{SENSE} comparator outputs to avoid false current sensing during MOSFET switching.

Blanking is provided in two phases (Figure 12): The first phase automatically blanks during gate rise time. Gate rise times can vary depending on MOSFET type. For this reason the LTC4269-2 performs true 'leading edge blanking' by automatically blanking OC and I_{SENSE} comparator outputs until OUT rises to within 0.5V of V_{IN} or reaches its clamp level of 13V. The second phase of blanking starts after the leading edge of OUT has been completed. This phase is programmable by the user with a resistor connected from the BLANK pin to GND. Typical durations for this portion of the blanking period are from 45ns at R_{BLANK} = 10k to 540ns at R_{BLANK} = 120k. Blanking duration can be approximated as:

$$\text{Blanking (extended)} = [45(R_{BLANK}/10k)]ns$$

(See graph in the Typical Performance Characteristics section).

Programming Current Limit (OC Pin)

The LTC4269-2 uses a precise 107mV sense threshold at the OC pin to detect overcurrent conditions in the converter and set a soft-start latch. It is independent of duty cycle because it is not affected by slope compensation programmed at the I_{SENSE} pin. The OC pin monitors the peak current in the primary MOSFET by sensing the voltage across a sense resistor (R_S) in the source of the MOSFET. The overcurrent limit for the converter can be programmed by:

$$\text{Overcurrent limit} = (107mV/R_S)(N_P/N_S) - (½)(I_{RIPPLE})$$

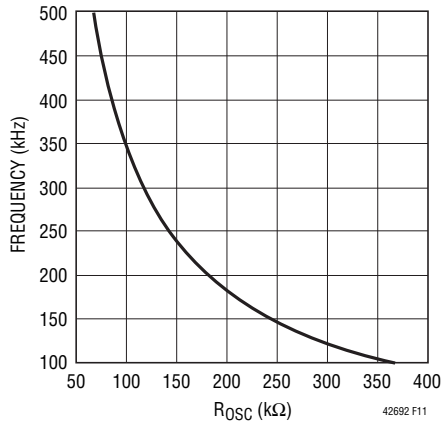

Figure 11. Oscillator Frequency, f_{OSC}, vs R_{OSC}

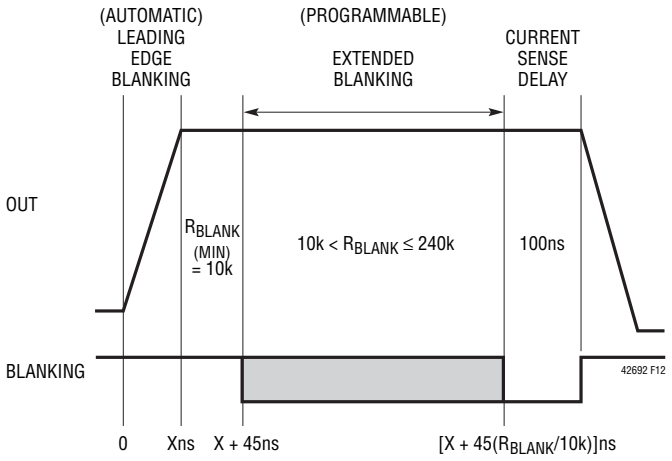

Figure 12. Leading Edge Blank Timing

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where:

R_S = sense resistor in source of primary MOSFET

I_{RIPPLE} = I_{P-P} ripple current in the output inductor L1

N_S = number of transformer secondary turns

N_P = number of transformer primary turns

Programming Slope Compensation

The LTC4269-2 uses a current mode architecture to provide fast response to load transients and to ease frequency compensation requirements. Current mode switching regulators which operate with duty cycles above 50% and have continuous inductor current must add slope compensation to their current sensing loop to prevent subharmonic oscillations. (For more information on slope compensation, see Application Note 19.) The LTC4269-2 has programmable slope compensation to allow a wide range of inductor values, to reduce susceptibility to PCB generated noise and to optimize loop bandwidth. The LTC4269-2 programs slope compensation by inserting a resistor, R_{SLOPE}, in series with the I_{SENSE} pin (Figure 13). The LTC4269-2 generates a current at the I_{SENSE} pin which is linear from 0% duty cycle to the maximum duty cycle of the OUT pin. A simple calculation of $I_{SENSE} \bullet R_{SLOPE}$ gives an added ramp to the voltage at the I_{SENSE} pin for programmable slope compensation. (See both graphs I_{SENSE} Pin Current vs Duty Cycle and I_{SENSE} Maximum Threshold vs Duty Cycle in the Typical Performance Characteristics section.)

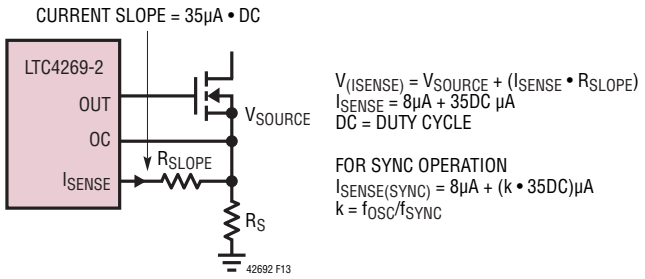

Figure 13. Programming Slope Compensation

Programming Synchronous Rectifier Timing: SOUT to OUT delay ('t_{DELAY}')

The LTC4269-2 has an additional output SOUT which provides a ±50mA peak drive clamped to 12V. In applications requiring synchronous rectification for high efficiency, the LTC4269-2 SOUT provides a sync signal for secondary side control of the synchronous rectifier MOSFETs (Figure 14). Timing delays through the converter can cause non-optimum control timing for the synchronous rectifier MOSFETs. The LTC4269-2 provides a programmable delay (t_{DELAY}, Figure 14) between SOUT rising edge and OUT rising edge to optimize timing control for the synchronous rectifier MOSFETs to achieve maximum efficiency gains. A resistor R_{DELAY} connected from the DELAY pin to GND sets the value of t_{DELAY}. Typical values for t_{DELAY} range from 10ns with R_{DELAY} = 10k to 160ns with R_{DELAY} = 160k (see graph in the Typical Performance Characteristics section).

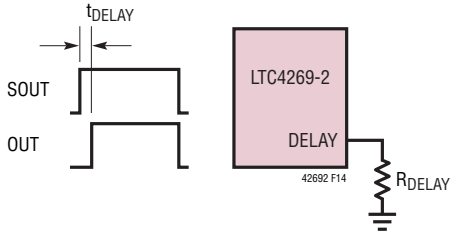

Figure 14. Programming SOUT and OUT Delay: t_{DELAY}

Programming Maximum Duty Cycle Clamp

For forward converter applications, a maximum switch duty cycle clamp which adapts to transformer input voltage is necessary for reliable control of the MOSFETs. This volt-second clamp provides a safeguard for transformer reset that prevents transformer saturation. The LTC4269-2 SD_V_{SEC} and SS_MAXDC pins provide a capacitor-less, programmable volt-second clamp solution using simple resistor ratios (Figure 15).

An increase of voltage at the SD_V_{SEC} pin causes the maximum duty cycle clamp to decrease. Deriving SD_V_{SEC} from a resistor divider connected to system input voltage

APPLICATIONS INFORMATION

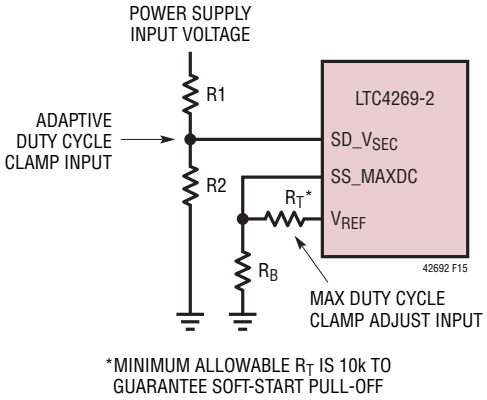

Figure 15. Programming Maximum Duty Cycle Clamp

creates the volt-second clamp. The maximum duty cycle clamp can be adjusted by programming voltage on the SS_MAXDC pin using a resistor divider from V_{REF}. An increase of voltage at the SS_MAXDC pin causes the maximum duty cycle clamp to increase.

To program the volt-second clamp, the following steps should be taken:

(1) The maximum operational duty cycle of the converter should be calculated for the given application.

(2) An initial value for the maximum duty cycle clamp should be calculated using the equation below with a first pass guess for SS_MAXDC.

Note: Since maximum operational duty cycle occurs at minimum system input voltage (UVLO), the voltage at the SD_V_{SEC} pin = 1.32V.

Max Duty Cycle Clamp (OUT Pin) =
$k \bullet 0.522(SS\_MAXDC(DC)/SD\_V_{SEC}) – (t_{DELAY} \bullet f_{OSC})$

where:

$SS\_MAXDC(DC) = V_{REF}(R_B/(R_T + R_B)$

SD_V_{SEC} = 1.32V at minimum system input voltage

t_{DELAY} = programmed delay between SOUT and OUT

$k = 1.11 – 5.5e–7 \bullet (f_{OSC})$

(3) The maximum duty cycle clamp calculated in (2) should be programmed to be 10% greater than the maximum operational duty cycle calculated in (1). Simple adjustment of maximum duty cycle can be achieved by adjusting SS_MAXDC.

Example calculation for (2):

For R_T = 35.7k, R_B = 100k, V_{REF} = 2.5V, R_{DELAY} = 40k, f_{OSC} = 200kHz and SD_V_{SEC} = 1.32V, this gives SS_MAXDC(DC) = 1.84V, t_{DELAY} = 40ns and k = 1

Maximum Duty Cycle Clamp
= 1 • 0.522(1.84/1.32) – (40ns • 200kHz)
= 0.728 – 0.008 = 0.72 (Duty Cycle Clamp = 72%)

Note 1: To achieve the same maximum duty cycle clamp at 100kHz as calculated for 200kHz, the SS_MAXDC voltage should be reprogrammed by,

SS_MAXDC(DC) (100kHz)
= SS_MAXDC(DC) (200kHz) • k (200kHz)/k (100kHz)
= 1.84 • 1.0/1.055 = 1.74V (k = 1.055 for 100kHz)

Note 2 : To achieve the same maximum duty cycle clamp while synchronizing to an external clock at the SYNC pin, the SS_MAXDC voltage should be reprogrammed as,

SS_MAXDC (DC) (fsync)
= SS_MAXDC (DC) (200kHz) • [(fosc/fsync) + 0.09(fosc/200kHz)0.6]

For SS_MAXDC (DC) (200kHz) = 1.84V for 72% duty cycle

SS_MAXDC (DC) (fsync = 250kHz) for 72% duty cycle
= 1.84 • [(200kHz/250kHz) + 0.09(1)0.6]
= 1.638V

Programming Soft-Start Timing

The LTC4269-2 has built-in soft-start capability to provide low stress controlled start-up from a list of fault conditions that can occur in the application (see Figures 16 and 17). The LTC4269-2 provides true PWM soft-start by

APPLICATIONS INFORMATION

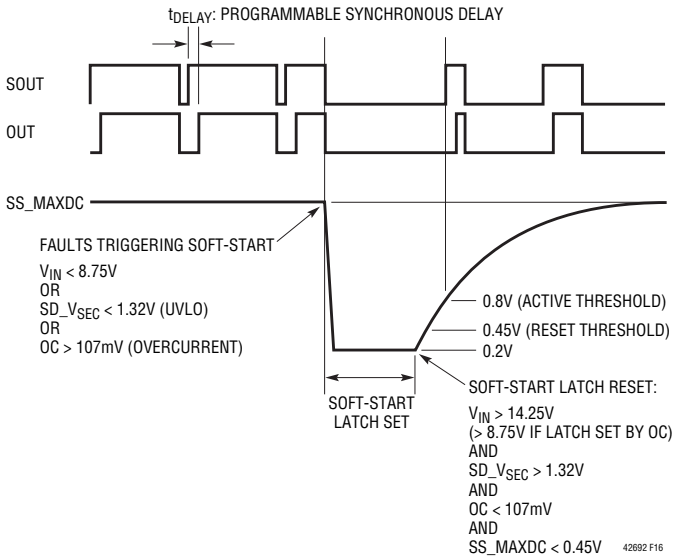

Figure 16. Timing Diagram

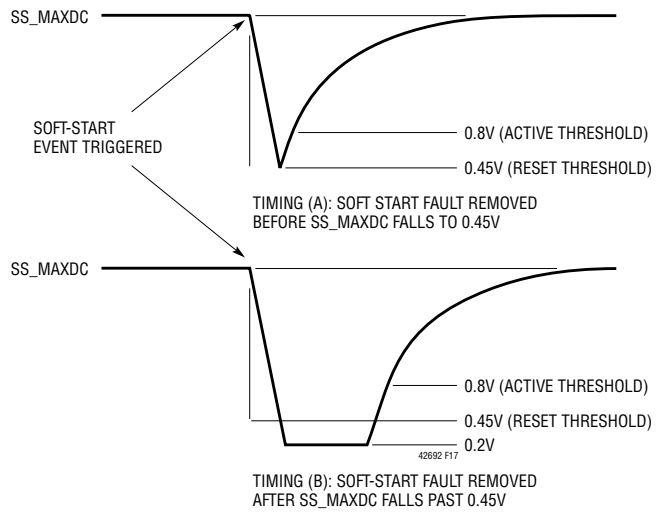

Figure 17. Soft-Start Timing

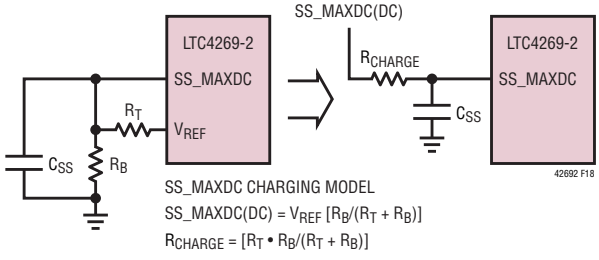

Figure 18. Programming Soft-Start Timing

using the SS_MAXDC pin to control soft-start timing. The proportional relationship between SS_MAXDC voltage and switch maximum duty cycle clamp allows the SS_MAXDC pin to slowly ramp output voltage by ramping the maximum switch duty cycle clamp—until switch duty cycle clamp seamlessly meets the natural duty cycle of the converter. A capacitor C_{SS} on the SS_MAXDC pin and the resistor divider from V_{REF} used to program maximum switch duty cycle clamp, determine soft-start timing (Figure 18).

A soft-start event is triggered for the following faults:

(1) V_{IN} < 8.75V, or

(2) SD_V_{SEC} < 1.32V (UVLO), or

(3) OC > 107mV (overcurrent condition)

When a soft-start event is triggered, switching at SOUT and OUT is stopped immediately. A soft-start latch is set and SS_MAXDC pin is discharged. The SS_MAXDC pin can only recharge when the soft-start latch has been reset.

Note: A soft-start event caused by (1) or (2) above, also causes V_{REF} to be disabled and to fall to GND.

Soft-start latch reset requires all of the following:

(A) V_{IN} > 14.25V*, and

(B) SD_V_{SEC} > 1.32V, and

(C) OC < 107mV, and

(D) SS_MAXDC < 0.45V (SS_MAXDC reset threshold)

*V_{IN} > 8.75V is okay for latch reset if the latch was only set by overcurrent condition in (3) above.

SS_MAXDC Discharge Timing

It can be seen in Figure 17 that two types of discharge can occur for the SS_MAXDC pin. In timing (A) the fault that caused the soft-start event has been removed before SS_MAXDC falls to 0.45V. This means the soft-start latch will be reset when SS_MAXDC falls to 0.45V and SS_MAXDC will begin charging. In timing (B), the fault that caused the soft-start event is not removed until some time after SS_MAXDC has fallen past 0.45V. The SS_MAXDC pin continues to discharge to 0.2V and remains low until all faults are removed.

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The time for SS_MAXDC to fall to a given voltage can be approximated as:

$SS\_MAXDC(t_{FALL}) = (C_{SS}/I_{DIS}) \bullet [SS\_MAXDC(DC) – V_{SS(MIN)}]$

where:

I_{DIS} = net discharge current on C_{SS}

C_{SS} = capacitor value at SS_MAXDC pin

SS_MAXDC(DC) = programmed DC voltage

$V_{SS(MIN)}$ = minimum SS_MAXDC voltage before recharge

$I_{DIS} \cong 8e^{-4} + (V_{REF} – V_{SS(MIN)})[(1/2R_B) – (1/R_T)]$

For faults arising from (1) and (2):

V_{REF} = 100mV.

For a fault arising from (3):

V_{REF} = 2.5V.

$SS\_MAXDC(DC) = V_{REF}[R_B/(R_T + R_B)]$

$V_{SS(MIN)}$ = SS_MAXDC reset threshold = 0.45V (if fault removed before t_{FALL})

Example

For an overcurrent fault (OC > 100mV), V_{REF} = 2.5V, R_T = 35.7k, R_B = 100k, C_{SS} = 0.1µF and assume $V_{SS(MIN)}$ = 0.45V,

$I_{DIS} \cong 8e^{-4} + (2.5 – 0.45)[(½ \bullet 100k) – (1/35.7k)]$
$= 8e^{-4} + (2.05)(–0.23e^{-4}) = 7.5e^{-4}$

SS_MAXDC(DC) = 1.84V

$SS\_MAXDC(t_{FALL}) = (1e^{-7}/7.5e^{-4}) \bullet (1.84 – 0.45) = 1.85e^{-4}s$

If the OC fault is not removed before 185µs then SS_MAXDC will continue to fall past 0.45V towards a new $V_{SS(MIN)}$. The typical V_{OL} for SS_MAXDC at 150µA is 0.2V.

SS_MAXDC Charge Timing

When all faults are removed and the SS_MAXDC pin has fallen to its reset threshold of 0.45V or lower, the SS_MAXDC pin will be released and allowed to charge.

SS_MAXDC will rise until it settles at its programmed DC voltage—setting the maximum switch duty cycle clamp.

The calculation of charging time for the SS_MAXDC pin between any two voltage levels can be approximated as an RC charging waveform using the model shown in Figure 16.

The ability to predict SS_MAXDC rise time between any two voltages allows prediction of several key timing periods:

(1) No Switching Period (time from SS_MAXDC(DC) to $V_{SS(MIN)}$ + time from $V_{SS(MIN)}$ to $V_{SS(ACTIVE)}$)

(2) Converter Output Rise Time (time from $V_{SS(ACTIVE)}$ to $V_{SS(REG)}$; $V_{SS(REG)}$ is the level of SS_MAXDC where maximum duty cycle clamp equals the natural duty cycle of the switch)

(3) Time For Maximum Duty Cycle Clamp within X% of Target Value

The time for SS_MAXDC to charge to a given voltage V_{SS} is found by re-arranging:

$V_{SS}(t) = SS\_MAXDC(DC)\ (1 – e^{(–t/RC)})$

to give,

$t = RC \bullet (–1) \bullet \ln(1 – V_{SS}/SS\_MAXDC(DC))$

where,

V_{SS} = SS_MAXDC voltage at time t

SS_MAXDC(DC) = programmed DC voltage setting maximum duty cycle clamp = $V_{REF}(R_B/(R_T + R_B)$

$R = R_{CHARGE}$ (Figure 16) = $R_T \bullet R_B/(R_T + R_B)$

$C = C_{SS}$ (Figure 16)

Example (1) No Switching Period

The period of no switching for the converter, when a soft-start event has occurred, depends on how far SS_MAXDC can fall before recharging occurs and how long a fault exists. It will be assumed that a fault triggering soft-start is removed before SS_MAXDC can reach its reset threshold (0.45V).

No Switching Period = $t_{DISCHARGE} + t_{CHARGE}$

$t_{DISCHARGE}$ = discharge time from SS_MAXDC(DC) to 0.45V

t_{CHARGE} = charge time from 0.45V to $V_{SS(ACTIVE)}$

$t_{DISCHARGE}$ was already calculated earlier as 185µs.

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t_{CHARGE} is calculated by assuming the following:

V_{REF} = 2.5V, R_T = 35.7k, R_B = 100k, C_{SS} = 0.1µF and $V_{SS(MIN)}$ = 0.45V.

$t_{CHARGE} = t(V_{SS} = 0.8V) – t(V_{SS} = 0.45V)$

Step 1:

SS_MAXDC(DC) = 2.5[100k/(35.7k + 100k)] = 1.84V

R_{CHARGE} = (35.7k • 100k/135.7k) = 26.3k

Step 2:

$t(V_{SS} = 0.45V)$ is calculated from:

$t = R_{CHARGE} • C_{SS} • (–1) • \ln(1 – V_{SS}/SS\_MAXDC(DC))$
$= 2.63e^{4} • 1e^{–7} • (–1) • \ln(1 – 0.45/1.84)$
$= 2.63e^{–3} • (–1) • \ln(0.755) = 7.3e^{–4}$ s

Step 3:

$t(V_{SS} = 0.8V)$ is calculated from:

$t = R_{CHARGE} • C_{SS} • (–1) • \ln(1 – V_{SS}/SS–MAXDC(DC))$
$= 2.63e^{4} • 1e^{–7} • (–1) • \ln(1 – 0.8/1.84)$
$= 2.63e^{–3} • (–1) • \ln(0.565) = 1.5e^{–3}$ s

From Step 1 and Step 2

$t_{CHARGE} = (1.5 – 0.73)e^{–3}$ s = $7.7e^{–4}$ s

The total time of no switching for the converter due to a soft-start event

$= t_{DISCHARGE} + t_{CHARGE} = 1.85e^{–4} + 7.7e^{–4} = 9.55e^{–4}$ s

Example (2) Converter Output Rise Time

The rise time for the converter output to reach regulation can be closely approximated as the time between the start of switching (SS_MAXDC = $V_{SS(ACTIVE)}$) and the time where converter duty cycle is in regulation (DC(REG)) and no longer controlled by SS_MAXDC (SS_MAXDC = $V_{SS(REG)}$). Converter output rise time can be expressed as:

Output Rise Time = $t(V_{SS(REG)}) – t(V_{SS(ACTIVE)})$

Step 1: Determine converter duty cycle DC(REG) for output in regulation.

The natural duty cycle DC(REG) of the converter depends on several factors. For this example it is assumed that DC(REG) = 60% for power supply input voltage near the power supply UVLO. This gives SD_V_{SEC} = 1.32V.

Also assume that the maximum duty cycle clamp programmed for this condition is 72% for SS_MAXDC(DC) = 1.84V, f_{OSC} = 200kHz and R_{DELAY} = 40k.

Step 2: Calculate $V_{SS(REG)}$

To calculate the level of SS_MAXDC ($V_{SS(REG)}$) that no longer clamps the natural duty cycle of the converter, the equation for maximum duty cycle clamp must be used (see previous section Programming Maximum Duty Cycle Clamp).

The point where the maximum duty cycle clamp meets DC(REG) during soft-start is given by:

DC(REG) = Max Duty Cycle Clamp

$0.6 = k • 0.522(SS\_MAXDC(DC)/SD\_V_{SEC}) – (t_{DELAY} • f_{OSC})$
For SD_V_{SEC} = 1.32V, f_{OSC} = 200kHz and R_{DELAY} = 40k

This gives k = 1 and t_{DELAY} = 40ns.

Rearranging the above equation to solve for SS_MAXDC = $V_{SS(REG)}$

$= [0.6 + (t_{DELAY} • f_{OSC})(SD\_V_{SEC})]/(k • 0.522)$
$= [0.6 + (40ns • 200kHz)(1.32V)]/(1 • 0.522)$
$= (0.608)(1.32)/0.522 = 1.537V$

Step 3: Calculate $t(V_{SS(REG)}) – t(V_{SS(ACTIVE)})$

Recall the time for SS_MAXDC to charge to a given voltage V_{SS} is given by:

$t = R_{CHARGE} • C_{SS} • (–1) • \ln(1 – V_{SS}/SS\_MAXDC(DC))$

(Figure 16 gives the model for SS_MAXDC charging)

For R_T = 35.7k, R_B = 100k, R_{CHARGE} = 26.3k

For C_{SS} = 0.1µF, this gives $t(V_{SS(ACTIVE)})$
$= t(V_{SS(0.8V)}) = 2.63e^{4} • 1e^{–7} • (–1) • \ln(1 – 0.8/1.84)$
$= 2.63e^{–3} • (–1) • \ln(0.565) = 1.5e^{–3}$ s

$t(V_{SS(REG)}) = t(V_{SS(1.537V)}) = 26.3k • 0.1µF • –1 • \ln(1 – 1.66/1.84) = 2.63e^{–3} • (–1) • \ln(0.146) = 5e^{–3}$ s

The rise time for the converter output:

$= t(V_{SS(REG)}) – t(V_{SS(ACTIVE)}) = (5 – 1.5)e^{–3}$ s
$= 3.5e^{–3}$ s

APPLICATIONS INFORMATION

Example (3) Time For Maximum Duty Cycle Clamp to Reach Within X% of Target Value

A maximum duty cycle clamp of 72% was calculated previously in the section 'Programming Maximum Duty Cycle Clamp'. The programmed value used for SS_MAXDC(DC) was 1.84V.

The time for SS_MAXDC to charge from its minimum value $V_{SS(MIN)}$ to within X% of SS_MAXDC(DC) is given by:

t(SS_MAXDC charge time within X% of target)
= t[(1 – (X/100) • SS_MAXDC(DC)] – t($V_{SS(MIN)}$)

For X = 2 and $V_{SS(MIN)}$ = 0.45V, t(0.98 • 1.84) – t(0.45)
= t(1.803) – t(0.45)

From previous calculations, t(0.45) = $7.3e^{-4}$s.

Using previous values for R_T, R_B and C_{SS},

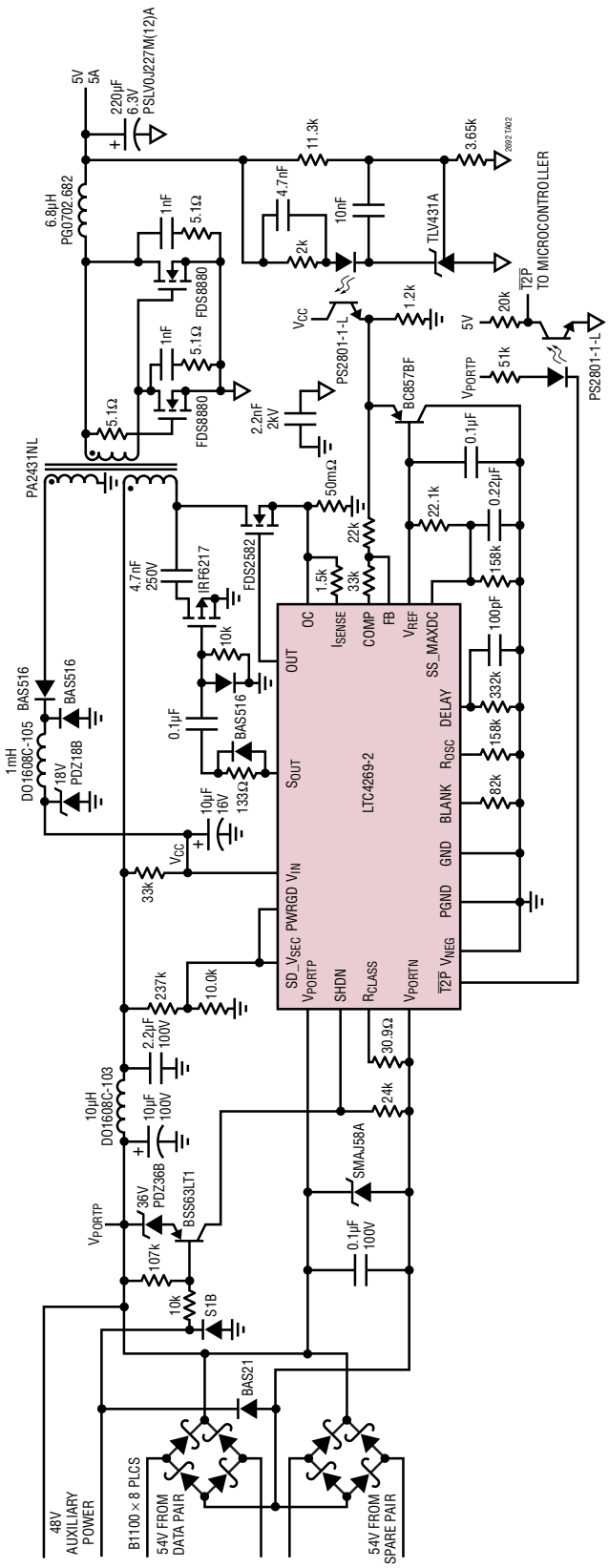
t(1.803) = $2.63e^{-4}$ • $1e^{-7}$ • (–1) • ln(1 – 1.803/1.84)
= $2.63e^{-3}$ • (–1) • ln(0.02) = $1.03e^{-2}$ s

Hence the time for SS_MAXDC to charge from its minimum reset threshold of 0.45V to within 2% of its target value is given by:

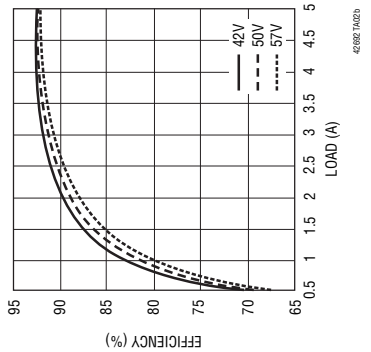
t(1.803) – t(0.45) = $1.03e^{-2}$ – $7.3e^{-4}$ = $9.57e^{-3}$s

TYPICAL APPLICATION

PoE-Based Self-Driven Synchronous Forward Power Supply

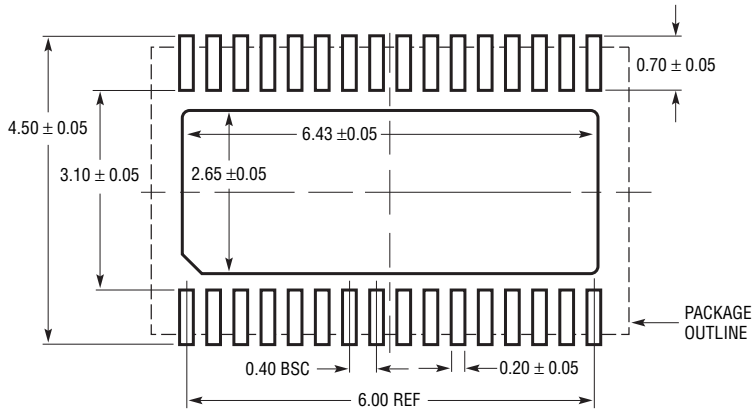


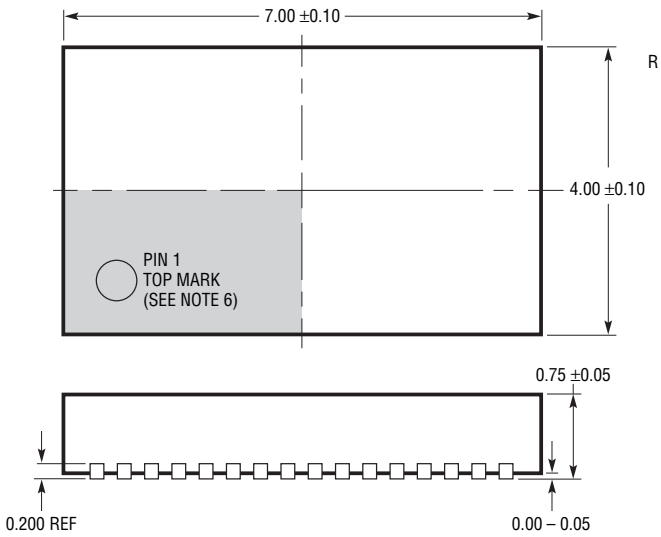
Efficiency vs Load Current

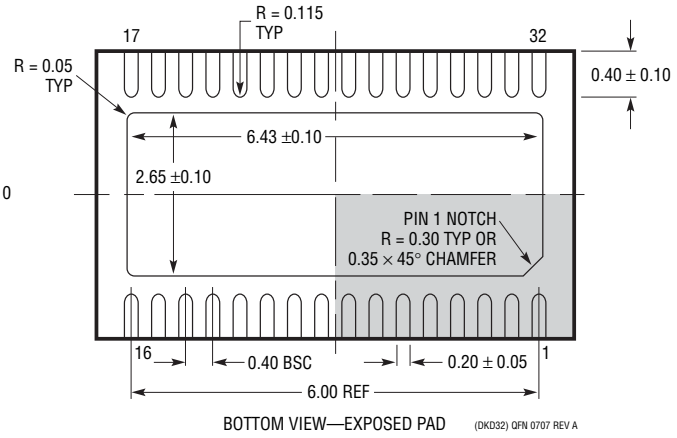


PACKAGE DESCRIPTION

DKD Package
32-Lead Plastic DFN (7mm × 4mm)
(Reference LTC DWG # 05-08-1734 Rev A)







NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WXXX) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	04/10	Connected PWRGD Pin to SD_V_{SEC} Pin in Typical Applications Circuits.	1, 23, 31
		Added Text Clarifying Connecting PWRGD Pin to SD_V_{SEC} Pin in Shutdown and Programming the Power Supply Undervoltage Lockout Section of Applications Information.	23

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1952	Single Switch Synchronous Forward Controller	Synchronous Controller, Programmable Volt-Sec Clamp, Low Start Current
LTC3803	Current Mode Flyback DC/DC Controller in ThinSOT™	200kHz Constant Frequency, Adjustable Slope Compensation, Optimized for High Input Voltage Applications
LTC3805	Adjustable Frequency Current Mode Flyback Controller	Slope Comp Overcurrent Protect, Internal/External Clock
LTC3825	Isolate No-Opto Synchronous Flyback Controller with Wide Input Supply Range	Adjustable Switching Frequency, Programmable Undervoltage Lockout, Accurate Regulation Without Trim, Synchronous for High Efficiency.
LTC4257-1	IEEE 802.3af PD Interface Controller	100V 400mA Internal Switch, Programmable Classification Dual Current Limit
LTC4258	Quad IEEE 802.3af Power over Ethernet Controller	DC Disconnect Only, IEEE-Compliant PD Detection and Classification, Autonomous Operation or I^2C Control
LTC4259A-1	Quad IEEE 802.3af Power over Ethernet Controller	AC or DC Disconnect IEEE-Compliant PD Detection and Classification, Autonomous Operation or I^2C Control
LTC4263	Single IEEE 802.3af Power over Ethernet Controller	AC or DC Disconnect IEEE-Compliant PD Detection and Classification, Autonomous Operation
LTC4263-1	High Power Single PSE Controller	Internal Switch, Autonomous Operation, 30W
LTC4265	IEEE 802.3at PD Interface Controller	2-Event Classification Signaling, Programmable Classification, Auxiliary Support
LTC4266	Quad IEEE 802.3at PSE Controller	Type 1 and 2 Compliant, 180mW/Port at 720mA, Advanced Power Management, 4-Point PD Detection
LTC4267-1/ LTC4267-3	IEEE 802.3af PD Interface with Integrated Switching Regulator	100V 400mA Internal Switch, Programmable Classification, 200KHz or 300kHz Constant Frequency PWM, Interface and Switcher Optimized for IEEE-Compliant PD System.
LTC4268-1	35W High Power PD Interface with Integrated Switching Regulator	750mA MOSFET, Programmable Classification, Synchronous No-Opto Flyback Controller, 50kHz to 250kHz
LTC4269-1	IEEE 802.3at PD Interface Integrated Switching Regulator	2-Event Classification, Programmable Classification, Synchronous No-Opto Flyback Controller, 50kHz to 250kHz

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