S71PL-J Based MCPs

SPANSION®

Data Sheet *(Retired Product)*

This product has been retired and is not recommended for new designs. For new designs, S71GL-A or S71GL-N supersedes S71PL-J. Please contact your local Spansion sales office to determine the appropriate migration device, specifications, and ordering information. Availability of this document is retained for reference and historical purposes only.

S71PL-J Based MCPs

Stacked Multi-Chip Product (MCP) Flash Memory and RAM

256M/128/64/32 Megabit (16/8/4/2M x 16-bit) CMOS 3.0 Volt-only Simultaneous Operation Page Mode Flash Memory and 64/32/16/8/4 Megabit (4M/2M/1M/512K/256K x 16-bit) Static RAM/pSRAM

Data Sheet

Note: This product has been retired and is not recommended for new designs. For new designs, S71GL-A or S71GL-N supersedes S71PL-J. Please contact your local Spansion sales office to determine the appropriate migration device, specifications, and ordering information. Availability of this document is retained for reference and historical purposes only.

Features

- ■ **Power supply voltage of 2.7 V to 3.1 V**
- ■ **High performance**
  - – 65 ns (65 ns Flash, 70 ns pSRAM)
- ■ **Packages**
  - – 7 x 9 x 1.2 mm 56 ball FBGA

  - – 8 x 11.6 x 1.2 mm 64 ball FBGA
  - – 8 x 11.6 x 1.4 mm 84 ball FBGA
- ■ **Operating Temperature**
  - – –25°C to +85°C
  - – –40°C to +85°C

General Description

The S71PL series is a product line of stacked Multi-Chip Product (MCP) packages and consists of:

- ■ One or more S29PL (Simultaneous Read/Write) Flash memory die

- ■ pSRAM or SRAM

The 256 Mb Flash memory consists of two S29PL127J devices. In this case, CE#f2 is used to access the second Flash and no extra address lines are required.

The products covered by this document are listed in the table below:

		Flash Memory Density			
		32Mb (1)	**64Mb** (1)	**128Mb** (2)	**256Mb** (2)
pSRAM Density	4 Mb	S71PL032J40			
	8 Mb	S71PL032J80	S71PL064J80		
	16 Mb	S71PL032JA0	S71PL064JA0		
	32 Mb		S71PL064JB0	S71PL127JB0	
	64 Mb			S71PL127JC0	S71PL254JC0

		Flash Memory Density	
		32Mb	**64Mb**
SRAM Density (1)	4 Mb	S71PL032J04	
	8 Mb	S71PL032J08	S71PL064J08
	16 Mb		S71PL064J0A

Notes
1. *Not recommended for new designs; contact your local Spansion sales representative for details.*

2. *Not recommended for new designs: use S71PL127N and S71PL256N instead.*

Publication Number S71PL-J_00   **Revision** B   **Amendment** 6   **Issue Date** February 17, 2010

For detailed specifications, please refer to the individual data sheets listed in the following table.

Document	Publication Identification Number (PID)
S29PL-J	S29PL-J_M0
pSRAM Type 1	psram_12
pSRAM Type 2	psram_15
8 Mb pSRAM Type 3	psram_25
16 Mb pSRAM Type 3	psram_06
pSRAM Type 4	psram_18
pSRAM Type 5	psram_21
pSRAM Type 6	psram_14
pSRAM Type 7	psram_13
4 Mb/8 Mb SRAM Type 1	sram_02
16 Mb SRAM Type 1	sram_06
SRAM Type 4	sram_07
32 Mb pSRAM Type 8	psram_31

Note
None of these RAM specifications are applicable for new designs. Please contact your local Spansion sales representative for details.

1. Product Selector Guide

1.1 32 Mb Flash Memory

Device-Model#	Flash Access time (ns)	(p)SRAM density	(p)SRAM Access time (ns)	pSRAM type	Package
S71PL032J04-0B	65	4M SRAM	70	SRAM1	TSC056
S71PL032J04-0K	65	4M SRAM	70	SRAM4	TSC056
S71PL032J40-0K	65	4M pSRAM	70	pSRAM4	TLC056
S71PL032J08-0B	65	8M SRAM	70	SRAM1	TSC056
S71PL032J80-0F	65	8M pSRAM	70	pSRAM5	TSC056
S71PL032J80-Q7	65	8M pSRAM	70	pSRAM1	TSC056
S71PL032J80-QF	65	8M pSRAM	70	pSRAM3	TSC056
S71PL032JA0-0K	65	16 Mb pSRAM	70	pSRAM1	TSC056
S71PL032JA0-QF	65	16 Mb pSRAM	70	pSRAM3	TSC056
S71PL032JA0-0Z	65	16M pSRAM	70	pSRAM7	TLC056

1.2 64 Mb Flash Memory

Device-Model#	Flash Access time (ns)	(p)SRAM density	(p)SRAM Access time (ns)	(p)SRAM type	Package
S71PL064J80-07	65	8M pSRAM	70	pSRAM4	TSC056
S71PL064J0A-0S	65	16M SRAM	70	SRAM 4	TLC056
S71PL064JA0-0Z	65	16M pSRAM	70	pSRAM7	TLC056
S71PL064JA0-0B	65	16M pSRAM	70	pSRAM3	TLC056
S71PL064JA0-07	65	16M pSRAM	70	pSRAM1	TLC056
S71PL064JA0-0P	65	16M pSRAM	70	pSRAM7	TLC056
S71PL064JB0-QB	65	32M pSRAM	70	pSRAM2	TLC056
S71PL064JB0-0U	65	32M pSRAM	70	pSRAM8	TLC056

1.3 128 Mb Flash Memory

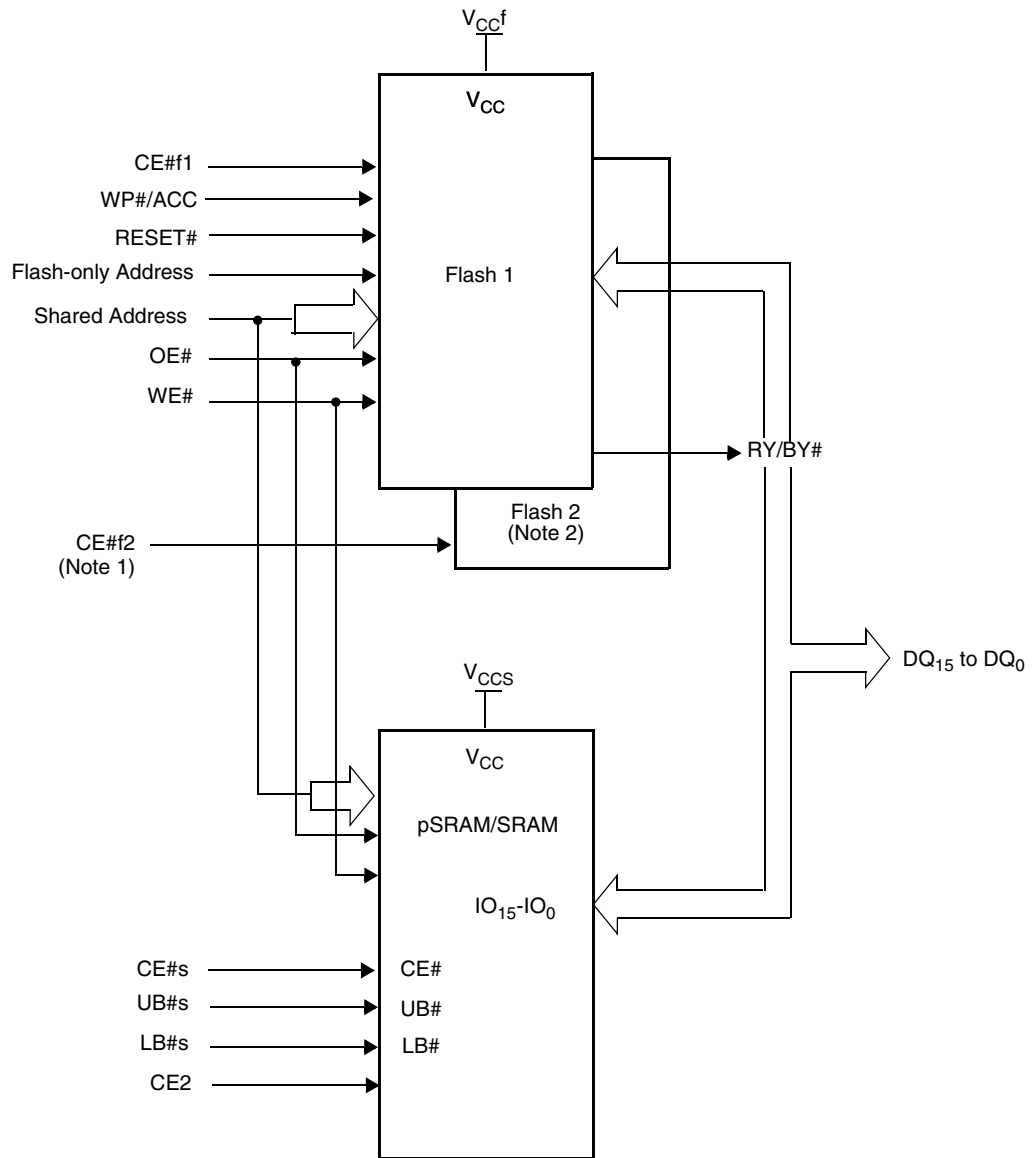Not recommended for new designs; use S71PL127N instead.

Device-Model#	Flash Access time (ns)	pSRAM density	pSRAM Access time (ns)	pSRAM type	Package
S71PL127JB0-9Z	65	32M pSRAM	70	pSRAM7	TLA064
S71PL127JB0-9U	65	32M pSRAM	70	pSRAM6	TLA064
S71PL127JB0-9B	65	32M pSRAM	70	pSRAM2	TLA064
S71PL127JC0-9B	65	64M pSRAM	70	pSRAM2	TLA064
S71PL127JC0-9Z	65	64M pSRAM	70	pSRAM7	TLA064
S71PL127JC0-9U	65	64M pSRAM	70	pSRAM6	TLA064

1.4 256Mb Flash Memory (2xS29PL127J)

Not recommended for new designs: use S71PL256N instead.

Device-Model#	Flash Access time (ns)	pSRAM density	pSRAM Access time (ns)	pSRAM type	Package
S71PL254JC0-TB	65	64M pSRAM	70	pSRAM2	FTA084
S71PL254JC0-TZ	65	64M pSRAM	70	pSRAM7	FTA084

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2. MCP Block Diagram

$V_{CC}f$

V_{CC}

CE#f1
WP#/ACC
RESET#
Flash-only Address
Shared Address
OE#
WE#

Flash 1

RY/BY#

CE#f2
(Note 1)

Flash 2
(Note 2)

DQ_{15} to DQ_0

V_{CCS}

V_{CC}

pSRAM/SRAM

IO_{15}-IO_0

CE#s   CE#
UB#s   UB#
LB#s   LB#
CE2

Notes

1. *For 1 Flash + pSRAM, CE#f1=CE#. For 2 Flash + pSRAM, CE#=CE#f1 and CE#f2 is the chip-enable for the second Flash.*

2. *For 256Mb only, Flash 1 = Flash 2 = S29PL127J.*

3. Connection Diagrams

Figure 3.1 S71PL032J Connection Diagram

56-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)

Notes
1. May be shared depending on density.
   – A19 is shared for the 16M pSRAM configuration.
   – A18 is shared for the 8M pSRAM and above configurations.
2. Connecting all V_{CC} and V_{SS} balls to V_{CC} and V_{SS} is recommended.

MCP	Flash-only Addresses	Shared Addresses
S71PL032JA0	A20	A19-A0
S71PL032J80	A20-A19	A18-A0
S71PL032J08	A20-A19	A18-A0
S71PL032J40	A20-A18	A17-A0
S71PL032J04	A20-A18	A17-A0

Figure 3.2 S71PL064J Connection Diagram

56-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)
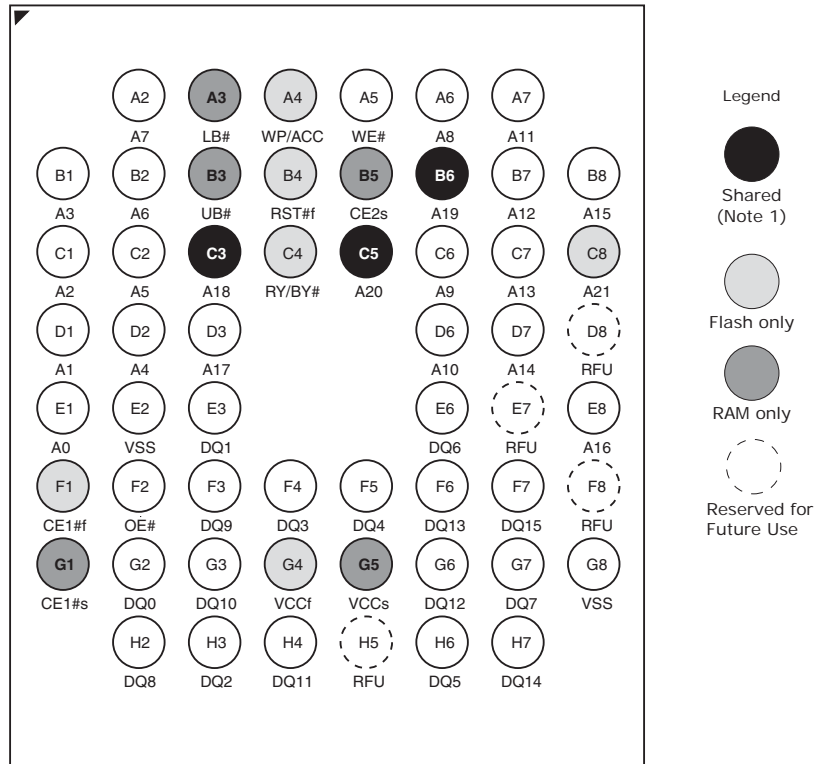
Notes

1. *May be shared depending on density.*
   - *A20 is shared for the 32M pSRAM configuration.*
   - *A19 is shared for the 16M pSRAM and above configurations.*
   - *A18 is shared for the 8M pSRAM and above configurations.*
2. *Connecting all V_{CC} and V_{SS} balls to V_{CC} and V_{SS} is recommended.*

MCP	Flash-only Addresses	Shared Addresses
S71PL064JB0	A21	A20-A0
S71PL064JA0	A21-A20	A19-A0
S71PL064J0A	A21-A20	A19-A0
S71PL064J80	A21-A19	A18-A0
S71PL064J08	A21-A19	A18-A0

Figure 3.3 S71PL127J Connection Diagram

64-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)

Legend

⚫ Shared (Note 1)

◯ Flash only

🔘 RAM only

⌂ Reserved for Future Use

*See notes below

Notes

1. May be shared depending on density.
    – A21 is shared for the 64M pSRAM configuration.
    – A20 is shared for the 32M pSRAM and above configurations.
2. A19 is shared for the 16M pSRAM and above configurations

MCP	Flash-only Addresses	Shared Addresses
S71PL127JC0	A22	A21-A0
S71PL127JB0	A22-A21	A20-A0

3. Connecting all V_{CC} and V_{SS} balls to V_{CC} & V_{SS} is recommended.
4. Ball L5 will be $V_{CC}F$ in the 84-ball density upgrades. Do not connect to V_{SS} or any other signal.

Figure 3.4 S71PL254J Connection Diagram

84-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)
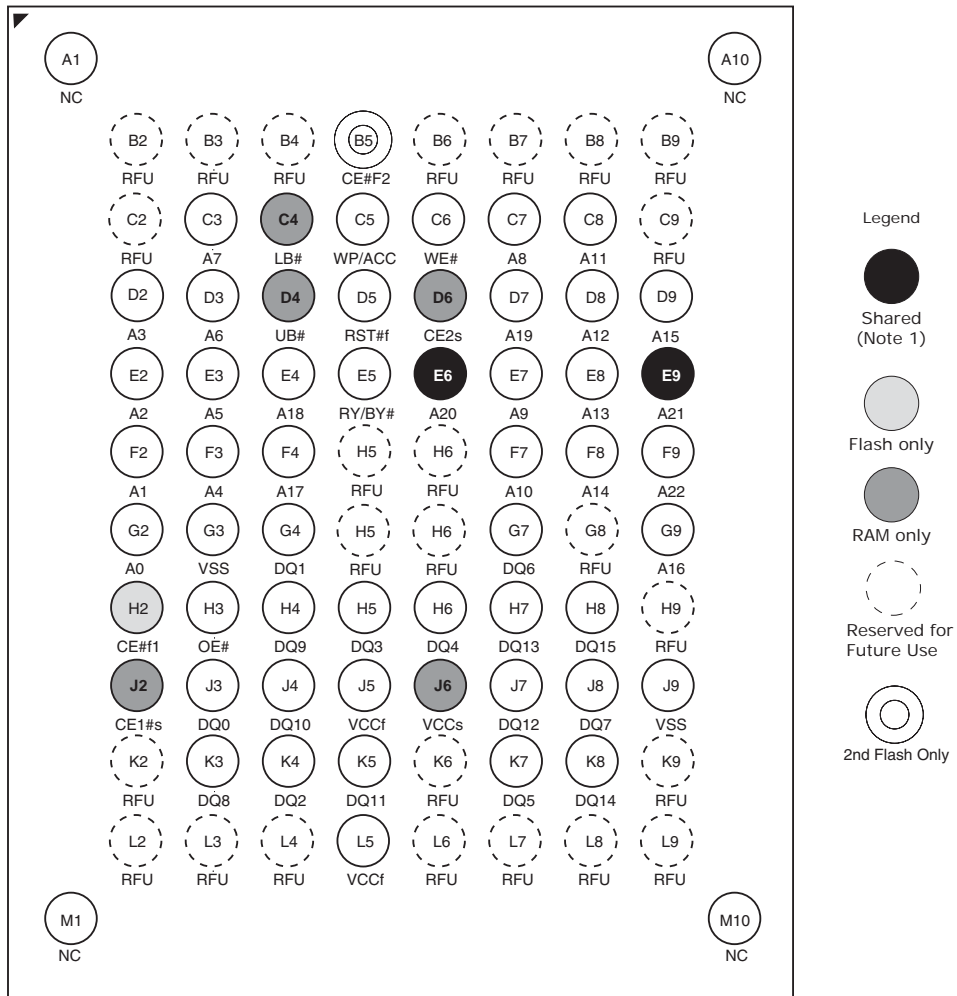
Notes

1. *May be shared depending on density.*
   – *A21 is shared for the 64M pSRAM configuration.*
   – *A20 is shared for the 32M pSRAM configuration.*

MCP	Flash-only Addresses	Shared Addresses
S71PL254JC0	A22	A21-A0

2. *Connecting all V_{CC} & V_{SS} balls to V_{CC} & V_{SS} is recommended.*

Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150° C for prolonged periods of time.

4. Pin Description

Signal	Description
A21–A0	22 Address Inputs (Common)
DQ15–DQ0	16 Data Inputs/Outputs (Common)
CE1#f	Chip Enable 1 (Flash)
CE#f2	Chip Enable 2 (Flash)
CE1#ps	Chip Enable 1 (pSRAM)
CE2ps	Chip Enable 2 (pSRAM)
OE#	Output Enable (Common)
WE#	Write Enable (Common)
RY/BY#	Ready/Busy Output (Flash 1)
UB#	Upper Byte Control (pSRAM)
LB#	Lower Byte Control (pSRAM)
RESET#	Hardware Reset Pin, Active Low (Flash 1)
WP#/ACC	Hardware Write Protect/Acceleration Pin (Flash)
$V_{CC}f$	Flash 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
$V_{CC}ps$	pSRAM Power Supply
V_{SS}	Device Ground (Common)
NC	Pin Not Connected Internally

5. Logic Symbol
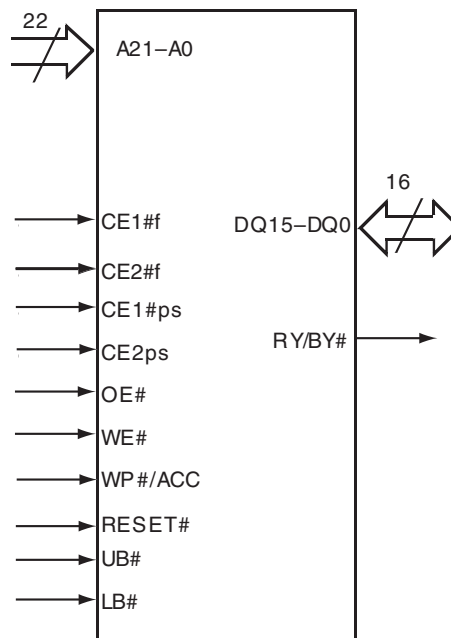
6. Ordering Information

The order number is formed by a valid combinations of the following:

```
S71PL    127    J    B0    BA    W    9    Z    0
```

Packing Type
0 = Tray
2 = 7" Tape and Reel
3 = 13" Tape and Reel

MODEL NUMBER
See the Valid Combinations table.

Package Modifier
0 = 7 x 9 mm, 1.2 mm height, 56 balls (TLC056 or TSC065)
9 = 8 x 11.6 mm, 1.2 mm height, 64 balls (TLA064 or TSB064)
T = 8 x 11.6 mm, 1.4 mm height, 84 balls (FTA084)
Q = See the Valid Combinations table

Temperature Range
W = Wireless (-25° C to +85° C)

Package Type
BA = Fine-pitch BGA Lead (Pb)-free compliant package
BF = Fine-pitch BGA Lead (Pb)-free package

pSRAM Density
C0 = 64 Mb pSRAM
B0 = 32 Mb pSRAM
A0 = 16 Mb pSRAM
80 = 8 Mb pSRAM
40 = 4 Mb pSRAM
0A = 16 Mb pSRAM
08 = 8 Mb SRAM
04 = 4 Mb SRAM

Process Technology
J = 110 nm, Floating Gate Technology

Flash Density
254= 256 Mb
127= 128 Mb
064= 64 Mb
032= 32 Mb

Product Family
S71PL Multi-chip Product (MCP)3.0-volt Simultaneous Read/Write, Page
Mode Flash Memory and RAM

6.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 6.1 S71PL032J Valid Combinations

Base Ordering Part Number	Package & Temperature	Package Modifier/ Model Number	Packing Type	Speed Options (ns)	(p)SRAM Type/ Access Time (ns)	Package Marking
S71PL032J04	BAW	0B	0, 2, 3 (1)	65	SRAM2 / 70	(2)
S71PL032J04		0K			SRAM4 / 70	
S71PL032J40		0K			pSRAM4 / 70	
S71PL032J80		0F			pSRAM5 / 70	
S71PL032J08		0B			SRAM2 / 70	
S71PL032J80		Q7			pSRAM1 / 70	
S71PL032J80		QF			pSRAM3 / 70	
S71PL032JA0		07			pSRAM1 / 70	
S71PL032JA0		QF			pSRAM3 / 70	
S71PL032JA0		0Z			pSRAM7 / 70	
S71PL032J04	BFW	0B	0, 2, 3 (1)	65	SRAM2 / 70	(2)
S71PL032J04		0K			SRAM4 / 70	
S71PL032J40		0K			pSRAM4 / 70	
S71PL032J80		0F			pSRAM5 / 70	
S71PL032J08		0B			SRAM2 / 70	
S71PL032J80		Q7			pSRAM1 / 70	
S71PL032J80		QF			pSRAM3 / 70	
S71PL032JA0		07			pSRAM1 / 70	
S71PL032JA0		QF			pSRAM3 / 70	
S71PL032JA0		0Z			pSRAM7 / 70	

Table 6.2 S71PL064J Valid Combinations

Base Ordering Part Number	Package & Temperature	Package Modifier/ Model Number	Packing Type	Speed Options (ns)	(p)SRAM Type/ Access Time (ns)	Package Marking
S71PL064J80	BAW	07	0, 2, 3 (1)	65	pSRAM 4/70	(2)
S71PL064J0A		0S			SRAM1 / 70	
S71PL064JA0		0B			pSRAM3 / 70	
S71PL064JA0		07			pSRAM1 / 70	
S71PL064JA0		0P			pSRAM7 / 70	
S71PL064JB0		QB			pSRAM2 / 70	
S71PL064JB0		0U			pSRAM8 / 70	
S71PL064J80	BFW	07	0, 2, 3 (1)	65	pSRAM7 /70	(2)
S71Pl064J0A		0S			SRAM1 / 70	
S71PL064JA0		0B			pSRAM3 / 70	
S71PL064JA0		07			pSRAM1 / 70	
S71PL064JA0		0P			pSRAM7 / 70	
S71PL064JB0		QB			pSRAM2 / 70	
S71PL064JB0		0U			pSRAM8 / 70	

Notes

1. Type 0 is standard. Specify other options as required.

2. BGA package marking omits leading "S" and packing type designator from ordering part number.

**Table 6.3** S71PL127J Valid Combinations

Base Ordering Part Number	Package & Temperature	Package Modifier/ Model Number	Packing Type	Speed Options (ns)	(p)SRAM Type/ Access Time (ns)	Package Marking
S71PL127JB0	BAW	9Z	0, 2, 3 (1)	65	pSRAM7 / 70	(2)
S71PL127JB0		9U			pSRAM6 /70	
S71PL127JC0		9B			pSRAM2 /70	
S71PL127JC0		9Z			pSRAM7 / 70	
S71PL127JC0		9U			pSRAM6 / 70	
S71PL127JB0		9B			pSRAM2 / 70	
S71PL127JB0	BFW	9Z	0, 2, 3 (1)	65	pSRAM7 / 70	(2)
S71PL127JB0		9U			pSRAM6 / 70	
S71PL127JC0		9B			pSRAM2 /70	
S71PL127JC0		9Z			pSRAM7 / 70	
S71PL127JC0		9U			pSRAM6 / 70	
S71PL127JB0		9B			pSRAM2 / 70	

Notes

1. Type 0 is standard. Specify other options as required.

2. BGA package marking omits leading "S" and packing type designator from ordering part number.

Table 6.4 S71PL254J Valid Combinations

Base Ordering Part Number	Package & Temperature	Model Number	Packing Type	Speed Options (ns)	(p)SRAM Type/ Access Time (ns)	Package Marking
S71PL254JC0	BAW	TB	0, 2, 3 (1)	65	pSRAM2 / 70	(2)
S71PL254JC0		TZ			pSRAM7 / 70	
S71PL254JC0	BFW	TB	0, 2, 3 (1)	65	pSRAM2 / 70	(2)
S71PL254JC0		TZ			pSRAM7 / 70	

Notes

1. Type 0 is standard. Specify other options as required.

2. BGA package marking omits leading "S" and packing type designator from ordering part number.

7.   Physical Dimensions

TLC056—56-ball Fine-Pitch Ball Grid Array (FBGA) 9 x 7 mm Package

TOP VIEW

SIDE VIEW

BOTTOM VIEW
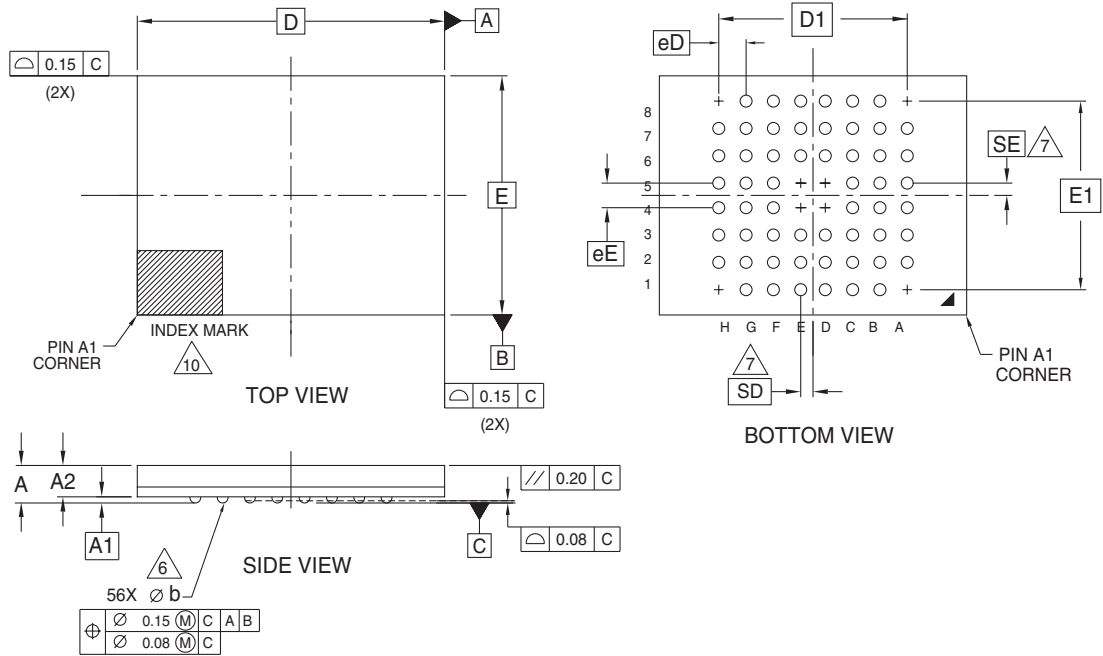
PACKAGE	TLC 056			
JEDEC	N/A			
D x E	9.00 mm x 7.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D	9.00 BSC.			BODY SIZE
E	7.00 BSC.			BODY SIZE
D1	5.60 BSC.			MATRIX FOOTPRINT
E1	5.60 BSC.			MATRIX FOOTPRINT
MD	8			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
n	56			BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A1,A8,D4,D5,E4,E5,H1,H8			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.

4. $\boxed{e}$ REPRESENTS THE SOLDER BALL GRID PITCH.

5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

    SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

    n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

    WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

    WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = $\boxed{e/2}$

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. N/A

10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3348 \ 16-038.22a

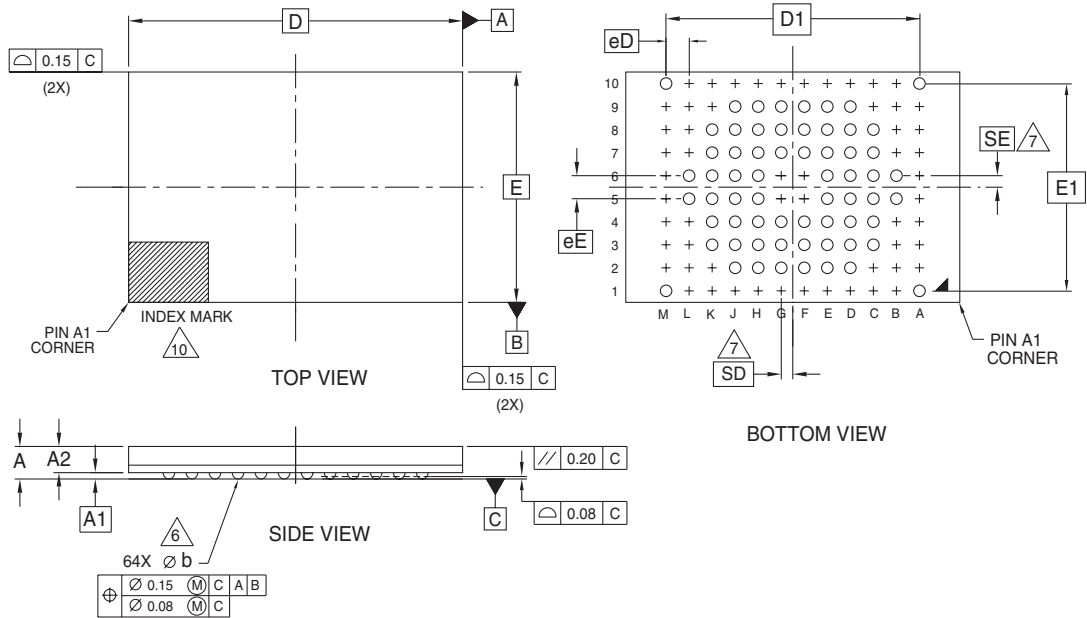## TSC056—56-ball Fine-Pitch Ball Grid Array (FBGA) 9 x 7 mm Package

TOP VIEW

SIDE VIEW

56X $\varnothing$ b

BOTTOM VIEW
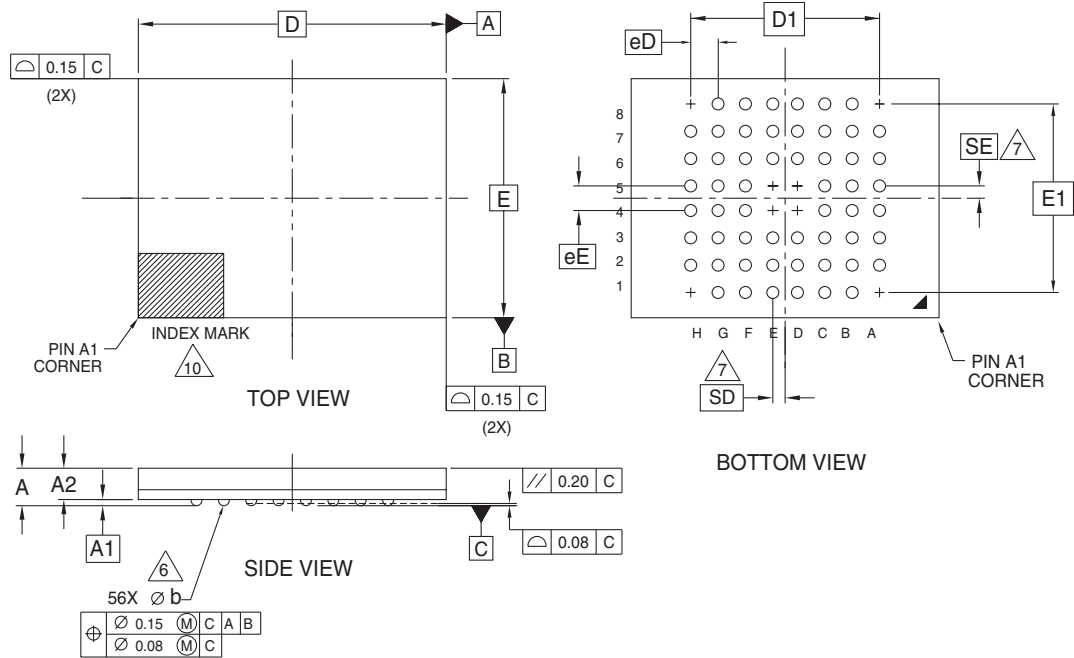
PACKAGE	TSC 056			
JEDEC	N/A			
D x E	9.00 mm x 7.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		9.00 BSC.		BODY SIZE
E		7.00 BSC.		BODY SIZE
D1		5.60 BSC.		MATRIX FOOTPRINT
E1		5.60 BSC.		MATRIX FOOTPRINT
MD		8		MATRIX SIZE D DIRECTION
ME		8		MATRIX SIZE E DIRECTION
n		56		BALL COUNT
φb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
		A1,A8,D4,D5,E4,E5,H1,H8		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.

4. e REPRESENTS THE SOLDER BALL GRID PITCH.

5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = $e/2$

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. N/A

10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3427 \ 16-038.22

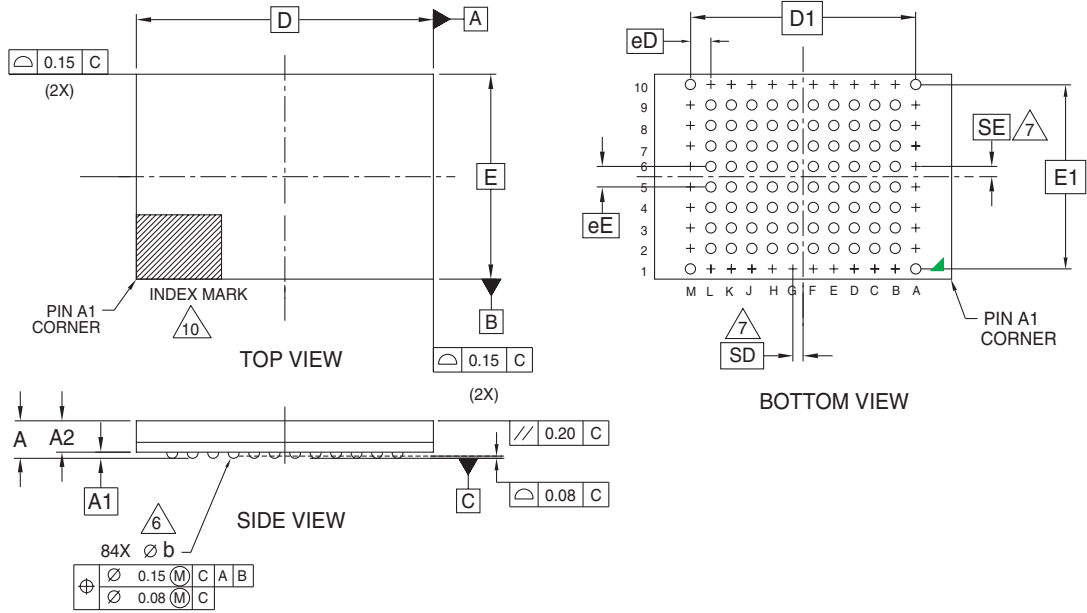## TLA064—64-ball Fine-Pitch Ball Grid Array (FBGA) 8 x 11.6 mm Package

TOP VIEW

SIDE VIEW

BOTTOM VIEW

PACKAGE		TLA 064		
JEDEC		N/A		
D x E		11.60 mm x 8.00 mm PACKAGE		
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		11.60 BSC.		BODY SIZE
E		8.00 BSC.		BODY SIZE
D1		8.80 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		12		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		64		BALL COUNT
φb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
		A2,A3,A4,A5,A6,A7,A8,A9 B1,B2,B3,B4,B7,B8,B9,B10 C1,C2,C9,C10,D1,D10,E1,E10, F1,F5,F6,F10,G1,G5,G6,G10 H1,H10,J1,J10,K1,K2,K9,K10 L1,L2,L3,L4,L7,L8,L9,L10 M2,M3,M4,M5,M6,M7,M8,M9		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.

4. e REPRESENTS THE SOLDER BALL GRID PITCH.

5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. N/A

10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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TSB064—64-ball Fine-Pitch Ball Grid Array (FBGA) 8 x 11.6 mm Package

TOP VIEW

SIDE VIEW

BOTTOM VIEW

PACKAGE		TSB 064		
JEDEC		N/A		
D x E		11.60 mm x 8.00 mm PACKAGE		
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	017	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		11.60 BSC.		BODY SIZE
E		8.00 BSC.		BODY SIZE
D1		8.80 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		12		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		64		BALL COUNT
φb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B2,B3,B4,B7,B8,B9,B10 C1,C2,C9,C10,D1,D10,E1,E10 F1,F5,F6,F10,G1,G5,G6,G10 H1,H10,J1,J10,K1,K2,K9,K10 L1,L2,L3,L4,L7,L8,L9,L10 M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.

4. $\boxed{e}$ REPRESENTS THE SOLDER BALL GRID PITCH.

5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = $\boxed{e/2}$

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. N/A

10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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FTA084—84-ball Fine-Pitch Ball Grid Array (FBGA) 8 x 11.6 mm Package

TOP VIEW

SIDE VIEW

BOTTOM VIEW

PACKAGE	FTA 084			NOTE
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			NOTE
SYMBOL	MIN	NOM	MAX	
A	---	---	1.40	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	1.02	---	1.17	BODY THICKNESS
D	11.60 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	8.80 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	84			BALL COUNT
φb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10,E1,E10 F1,F10,G1,G10,H1,H10 J1,J10,K1,K10,L1,L10 M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.

4. $\boxed{e}$ REPRESENTS THE SOLDER BALL GRID PITCH.

5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = $\boxed{e/2}$

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. N/A

10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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8. Revision History

Section	Description
Revision A (May 3, 2004)	
	Initial release
Revision A1 (May 6, 2004)	
Features	Corrected the high performance access times.
Connection Diagrams	Added reference points on all diagrams.
Ordering Information	Corrected package types. Corrected the description of product family to Page Mode Flash memory.
Revision A2 (May 11, 2004)	
General Description	Corrected the tables to reflect accurate device configurations.
Revision A3 (June 16, 2004)	
Ordering Information	Corrected the Valid Combinations tables to reflect accurate device configurations.
Revision A4 (July 16, 2004)	
Global	Global Change of FASL to Spansion. Global change to remove space between M and Mb callouts.
32 Mb Flash Memory	Replaced "S71PL032J08-07" with "S71PL032J08-0B". Replaced "S71PL032JA0" with "S71PL032JA0-07". Replaced "S71PL032JA0-08" with "S71PL032JA0-0F". Added row with the following content: S71PL032JA0-08; 65; 16Mb pSRAM; 70; pSRAM3; TLC056.
64 Mb Flash Memory	Replaced "S71PL064J08-0K" with "S71PL064J08-0B". Replaced "S71PL064J08-0P" with "S71PL064J08-0U". Deleted "S71PL064J80-05" row. Replaced "S71PL064JA0-07" with "S71PL064JA0-0K". Replaced "S71PL064JA0-0Z" with Added row with the following content:S71PL064JB0-07; 65; 32M pSRAM; 70; Psram 1; TLC056.
128 Mb Flash Memory	Added row with the following content: S71PL127JB0-9; 65; 32M pSRAM; 70; pSRAM; TLA064. Replaced "S71PL127JB0-97" with "S71PL127JB0-9Z". Added row with the following content: S71PL127JC0-97; 65; 64M pSRAM; 70; pSRAM1; TLA064. Replaced "S71PL127JC0-9P" with "S71PL127JC0-9Z". In the S71Pl254JB0-TB row changed pSRAM type from "pSRAM3" to "pSRAM2".
256 Mb Flash Memory	Added row with the following content: S71PL254JB0-TB; 65; 32M pSRAM; 70; pSRAM3; FTA084. Added row with the following content: S71PL254JC0-TB; 65; 64M pSRAM; 70; pSRAM2; FTA084.
Connection Diagrams	Updated pins D8, D9, and L5. Added notes 2 and 3 to drawing. Updated pins D8 and D9. Added Note 2 to drawing.
S71PL032J Valid Combinations	Changed S71PL032J08 (p)SRAM Type Access Time (ns) from "SRAM1" to "SRAM2" (4 changes made in table). Changed S71PL032JA0 (p)SRAM Type Access Time (ns) from "SRAM3 / 70" to pSRAM3 /70". Deleted all cells with the following collaborated text: "BAW,BFW, BAI. BFI". Merged previous place holder with cell above.
S71PL064J Valid Combinations	In (p)SRAM Type/Access Time (ns) changed all instances of "stet" to "pSRAM1/70". In Package Modifier/Model Number changed all instances of "stet" to "07". Added row to BAW Package and Temperature sections with the following content: S71PL064JB0; 07; 65 (previously inclusive); pSRAM1/70.
S71PL127J Valid Combinations	Changed the S71PL127JA0 Package Modifier/Model Number from "9Z" to "9P" (4 instances). Added 4 rows with the following content: S71PL127JC0; 97; pSRAM1/70.
S71PL254J Valid Combinations	Added 4 rows with the following content: S71PL254JC0; TB; pSRAM2/70. Added 4 rows with the following content: S71PL254JB0; TB; pSRAM2/70.

Section	Description
S71PL-J Based MCPs	Added 254M to Megabit indicator.
	Added 16 to CMOS indicator
Revision A5 (September 14, 2004)	
Product Selector Guide	Updated the 128Mb Flash Memory table.
Valid Combinations Table	Updated the S71PL127J Valid Combinations table.
Revision A6 (November 22, 2004)	
Product Selector Guide	Updated the 32Mb and 64Mb tables.
Valid Combinations Table	Updated the 32Mb and 64Mb combinations.
Physical Dimensions	Added the TSB064 package.
Revision A7 (February 8, 2005)	
pSRAM Type 7	Updated all information in this section
Revision A8 (April 6, 2005)	
S29PL-J Flash	Updated all information in this section
Revision A9 (May 12, 2005)	
Global	Added the S71PL064J0A option to cover the inclusion of the 16M SRAM
Revision A10 (June 22, 2005)	
Global	Removed 127/16 and 254/32 pSRAM and updated OPN for 64/16SRAM
Revision A11 (July 29, 2005)	
pSRAM Type 7	Updated this module
Revision B (September 29, 2005)	
S29PL-J Flash	Updated this module
SRAM Type 1	Updated this module
Revision B1 (October 25, 2005)	
pSRAM Type 5	Added this module
Revision B2 (January 25, 2006)	
Global	Added notices for devices not recommended for new designs
	Modified the Product Selection Guide
	Modified the S71PL032J, S71PL064J, S71PL127JValid Combinations tables
Revision B3 (March 17, 2006)	
Global	Modified the stucture of the document. Related data sheets are referenced rather than be embedded. Added data sheet reference table to that effect.
	Added the SRAM Type 4 option
	Added the 8Mb pSRAM Type 3 option
Revision B4 (December 22, 2006)	
Global	Added the S71PL064J80-07 for pSRAM Type 4
	Removed the S71PL064J08-0B
Revision B5 (July 17, 2007)	
Global	Updated product status for all listed products
Ordering Information	Revised ordering information for S71PL032JA0 and S71PL064JB0 MCPs
Revision B6 (February 17, 2010)	
Ordering Information	Added Q description under Package Modifier