| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| | | | |

| | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | | | | | | | | | | | | | | | | | | | | |
| SHEET | 15 | | | | | | | | | | | | | | | | | | | |
| REV STATUS | | | | REV | | | | | | | | | | | | | | | | |
| OF SHEETS | | | | SHEET | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

PREPARED BY
Rajesh Pithadia

**DEFENSE SUPPLY CENTER COLUMBUS**
**COLUMBUS, OHIO 43218-3990**
**http://www.dscc.dla.mil**

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Rajesh Pithadia

APPROVED BY
Charles F. Saffle

DRAWING APPROVAL DATE
10-04-28

REVISION LEVEL

# MICROCIRCUIT, LINEAR, DIFFERENTIAL ANALOG-TO-DIGITAL CONVERTER DRIVER, LOW DISTORTION, MONOLITHIC SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| A | **67268** | **5962-09220** |

SHEET 1 OF 15

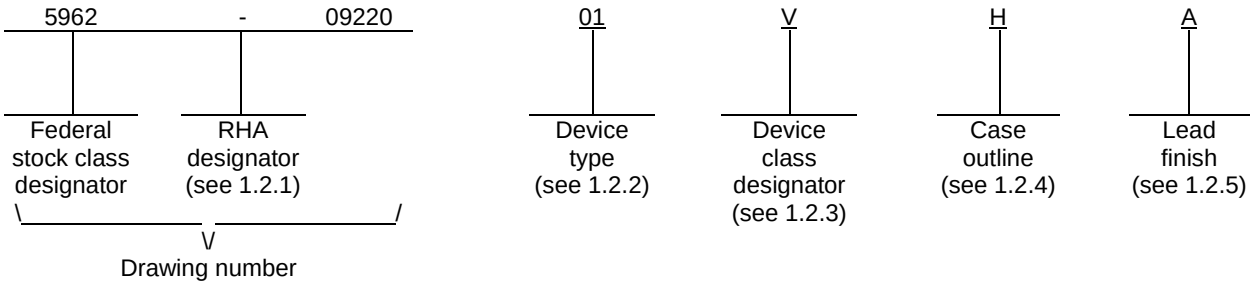
DSCC FORM 2233
APR 97

5962-E507-09

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | AD8138 | Low distortion, differential analog-to-digital converter driver |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| H | GDFP1-F10 | 10 | Flat pack |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

| | |
|---|---|
| Supply Voltage ($+V_S$ to $-V_S$) | 11 V |
| $V_{OCM}$ | ± Vs |
| ±IN (input range) | $-V_S$ + 0.3 V min to $+V_S$ – 1.6 V max |
| Internal Power Dissipation | 550 mW 2/ |
| Storage temperature range | -65°C to +150°C |
| Operating temperature range | -55°C to +125°C |
| Lead temperature range (soldering, 10 sec) | +300°C |
| Junction temperature ($T_J$) | +150°C |
| Thermal resistance, junction-to-case ($\theta_{JC}$) | 50°C/W |
| Thermal resistance, junction-to-ambient ($\theta_{JA}$) | 244°C/W |

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage ($V_{S+}/V_{S-}$) | ±2.5 V ( or +5V, 0V Single Supply) to ±5 V Dual Supply |
| Ambient operating temperature range ($T_A$) | -55°C to +125°C |

1.5 Operating Performance characteristics. 3/

Input/Output characteristics ($T_A$ = 25ºC, $V_S$ = ±5 V, $V_{OCM}$ = 0, G = +1, $R_{L,dm}$ = 500 Ω):

| | |
|---|---|
| Output voltage swing (maximum $\Delta V_{OUT}$, single-ended output) | 7.75 $V_{P-P}$ |
| Output current | 95 mA |
| Input common-mode voltage range (±$D_{IN}$ to ±OUT ) | -4.7 V to +3.4 V |
| Input voltage range ($V_{OCM}$ to ±OUT) | ± 3.8 V |

±$D_{IN}$ to ±OUT parameters ($T_A$ = 25ºC, $V_S$ = ±5 V, $V_{OCM}$ = 0, G = +1, $R_{L,dm}$ = 500 Ω):

| | |
|---|---|
| Dynamic performance: | |
| -3 dB small signal bandwidth ($V_{OUT}$ = 0.5 $V_{P-P}$, $C_F$ = 0 pF) | 320 MHz |
| -3 dB small signal bandwidth ($V_{OUT}$ = 0.5 $V_{P-P}$, $C_F$ = 1 pF) | 225 MHz |
| Bandwidth for 0.1 dB flatness ($V_{OUT}$ = 0.5 $V_{P-P}$, $C_F$ = 0 pF) | 30 MHz |
| Large signal bandwidth ($V_{OUT}$ = 2 $V_{P-P}$, $C_F$ = 0 pF) | 265 MHz |
| Slew rate ($V_{OUT}$ = 2 $V_{P-P}$, $C_F$ = 0 pF) | 1150 V/µs |
| Noise/Harmonic performance: 4/ | |
| Second harmonic ($V_{OUT}$ = 2 $V_{P-P}$, 5 MHz, $R_{L,dm}$ = 800 Ω) | -94 dBc |
| Second harmonic ($V_{OUT}$ = 2 $V_{P-P}$, 20 MHz, $R_{L,dm}$ = 800 Ω) | -87 dBc |
| Second harmonic ($V_{OUT}$ = 2 $V_{P-P}$, 70 MHz, $R_{L,dm}$ = 800 Ω) | -62 dBc |
| Third harmonic ($V_{OUT}$ = 2 $V_{P-P}$, 5 MHz, $R_{L,dm}$ = 800 Ω) | -114 dBc |
| Third harmonic ($V_{OUT}$ = 2 $V_{P-P}$, 20 MHz, $R_{L,dm}$ = 800 Ω) | -85 dBc |
| Third harmonic ($V_{OUT}$ = 2 $V_{P-P}$, 70 MHz, $R_{L,dm}$ = 800 Ω) | -57 dBc |
| Voltage noise (RTI, f = 100 kHz to 40 MHz) | 5 nV/$\sqrt{\text{Hz}}$ |

$V_{OCM}$ to ±OUT parameters ($T_A$ = 25ºC, $V_S$ = ±5 V, $V_{OCM}$ = 0, G = +1, $R_{L,dm}$ = 500 Ω):

| | |
|---|---|
| Dynamic/Noise performance: | |
| -3 dB small signal bandwidth | 250 MHz |
| Slew rate | 330 V/µs |
| Voltage noise (RTI, f = 100 kHz to 100 MHz) | 17 nV/$\sqrt{\text{Hz}}$ |

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ In product application, additional power dissipation created by output load current must not allow internal power dissipation absolute maximum to be exceeded.
3/ Refer to section 6.7 for further information.
4/ Harmonic distortion performance is equal or slightly worse with higher values of $R_{L,dm}$.

1.6 Radiation features :

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s) ..... ≥ 100 Krads(Si) 4/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections and block diagram. The terminal connections and block diagram shall be as specified on figure 1.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

---

4/ These parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Single supply 3/ | | | | | | | |
| $\pm D_{IN}$ to $\pm$OUT | | | | | | | |
| Offset voltage | $V_{OS,dm}$ | $V_{OS,dm} = V_{OUT,dm} / 2$, $V_{DIN+} = V_{DIN-} = V_{OCM} = 0$ V | 1 | 01 | -2.5 | +2.5 | mV |
| | | | 2, 3 | | -5 | +5 | |
| | | M,D,P,L,R | 1 | | -2.5 | +2.5 | |
| Input bias current | $I_B$ | | 1 | 01 | | 7 | µA |
| | | | 2,3 | | | 10 | |
| | | M,D,P,L,R | 1 | | | 7 | |
| Common-mode rejection | CMRR | $\Delta V_{OUT,dm} / \Delta V_{IN,cm}$, $\Delta V_{IN,cm} = 1$ V | 1 | 01 | | 0.316 | mV/V |
| | | | 2, 3 | | | 0.625 | |
| | | M,D,P,L,R | 1 | | | 0.316 | |
| $V_{OCM}$ to $\pm$OUT | | | | | | | |
| Input offset voltage 4/ | $V_{OS,cm}$ | $V_{OS,cm} = V_{OUT,cm}$ , $V_{DIN+} = V_{DIN-} = V_{OCM} = 0$ V | 1 | 01 | -5 | +5 | mV |
| | | | 2, 3 | | -10 | +10 | |
| | | M,D,P,L,R | 1 | | -5 | +5 | |
| Gain | $Gain_{, cm}$ | $\Delta V_{OUT,cm} / \Delta V_{OCM}$, $\Delta V_{OCM} = 2.5$ V $\pm$ 1 V | 1 | 01 | -3.2 | +3.2 | mV/V |
| | | | 2, 3 | | -4.5 | +4.5 | |
| | | M,D,P,L,R | 1 | | -3.2 | +3.2 | |
| Supply current | $I_S$ | | 1 | 01 | | 21 | mA |
| | | | 2, 3 | | | 24 | |
| | | M,D,P,L,R | 1 | | | 21 | |
| Power supply rejection ratio | PSRR | $\Delta V_{OUT,dm} / \Delta V_S$, $\Delta V_S = \pm$ 1 V | 1 | 01 | | 0.316 | mV/V |
| | | | 2, 3 | | | 0.625 | |
| | | M,D,P,L,R | 1 | | | 0.316 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified | | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Dual supply 3/ | | | | | | | | |
| $\pm D_{IN}$ to $\pm$OUT | | | | | | | | |
| Offset voltage | $V_{OS,dm}$ | $V_{OS,dm} = V_{OUT,dm} / 2$, $V_{DIN+} = V_{DIN-} = V_{OCM} = 0$ V | | 1 | 01 | -2.5 | +2.5 | mV |
| | | | | 2, 3 | | -5 | +5 | |
| | | | M,D,P,L,R | 1 | | -2.5 | +2.5 | |
| Input bias current | $I_B$ | | | 1 | 01 | | 7 | µA |
| | | | | 2,3 | | | 10 | |
| | | | M,D,P,L,R | 1 | | | 7 | |
| Common-mode rejection | CMRR | $\Delta V_{OUT,dm} / \Delta V_{IN,cm}$, $\Delta V_{IN,cm} = 1$ V | | 1 | 01 | | 0.316 | mV/V |
| | | | | 2, 3 | | | 0.625 | |
| | | | M,D,P,L,R | 1 | | | 0.316 | |
| $V_{OCM}$ to $\pm$OUT | | | | | | | | |
| Input offset voltage 4/ | $V_{OS,cm}$ | $V_{OS,cm} = V_{OUT,cm}$ , $V_{DIN+} = V_{DIN-} = V_{OCM} = 0$ V | | 1 | 01 | -3.5 | +3.5 | mV |
| | | | | 2, 3 | | -10 | +10 | |
| | | | M,D,P,L,R | 1 | | -3.5 | +3.5 | |
| Gain | Gain, $_{cm}$ | $\Delta V_{OUT,cm} / \Delta V_{OCM}$, $\Delta V_{OCM} = 2.5$ V $\pm$ 1 V | | 1 | 01 | -4.5 | +4.5 | mV/V |
| | | | | 2, 3 | | -5.8 | +5.8 | |
| | | | M,D,P,L,R | 1 | | -4.5 | +4.5 | |
| Supply current | $I_S$ | | | 1 | 01 | | 23 | mA |
| | | | | 2, 3 | | | 27 | |
| | | | M,D,P,L,R | 1 | | | 23 | |
| Power supply rejection ratio | PSRR | $\Delta V_{OUT,dm} / \Delta V_S$, $\Delta V_S = \pm$ 1 V | | 1 | 01 | | 0.316 | mV/V |
| | | | | 2, 3 | | | 0.625 | |
| | | | M,D,P,L,R | 1 | | | 0.316 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

1/ Devices supplied to this drawing have been characterized through all levels M, D, P, L, R of irradiation. However, this device is only tested at the “R” level. Pre and Post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurement for any RHA level, $T_A$ = +25°C.

2/ These parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

3/ For single supply,$V_{S\pm}$ = 5 V/0V, $V_{OCM}$ = 2.5 V, G = +1, $R_{L,dm}$ = 500 Ω, unless otherwise specified. For dual supply, $V_{S\pm}$ = ±5 V, $V_{OCM}$ = 0 V, G = +1, $R_{L,dm}$ = 500 Ω, unless otherwise specified. All specifications refer to single-ended input and differential output, unless otherwise specified. Refer to section 6.7 for further information.

4/ $V_{OS,cm}$ specifications assume the $V_{OCM}$ input pin is driven by a low impedance voltage source.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

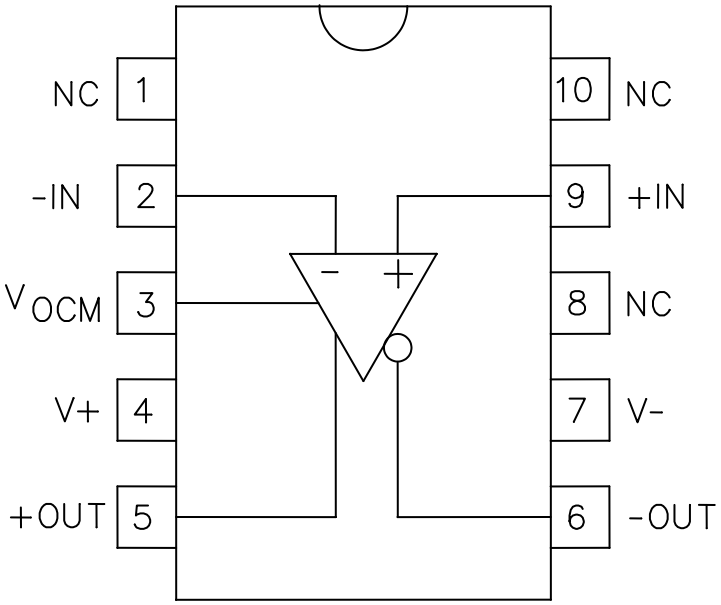
3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 49 (see MIL-PRF-38535, appendix A).




NC = No connect

NOTE:

The $V_{OCM}$ (Output Common Mode) pin is internally biased at a voltage approximately equal to the mid supply point (average value of the the voltages on V+ and V-). Relying on this internal bias results in an output common-mode voltage that is within about 100 mV of the expected value. In cases where more accurate control of the output common-mode level is required, it is recommended that an external source or resistor divider (made up of 10 kΩ resistors) be used. The output common-mode offset listed in table I herein assumes the $V_{OCM}$ input is driven by a low impedance voltage source. Refer to section 6.7 for further information.

FIGURE 1. Terminal connections and block diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, 6, 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|---|
| | Device class M | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | 1 | 1 | 1 |
| Final electrical parameters (see 4.2) | 1, 2, 3 1/ | 1, 2, 3 1/ | 1, 2, 3 1/ 2/ |
| Group A test requirements (see 4.4) | 1, 2, 3 | 1, 2, 3 | 1, 2, 3 |
| Group C end-point electrical parameters (see 4.4) | 1 | 1 | 1, 2, 3 2/ |
| Group D end-point electrical parameters (see 4.4) | 1 | 1 | 1, 2, 3 |
| Group E end-point electrical parameters (see 4.4) | 1 | 1 | 1, |

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous endpoint electrical parameters.

TABLE IIB. Burn-in and operating life test delta parameters. 1/

| Parameter | Symbol | Delta limits | Units |
|---|---|---|---|
| Supply current, $V_S$ = 5 V | $I_S$ | ±2.1 | mA |
| Gain, $_{cm}$, $V_S$ = 5 V | Gain, $_{cm}$ | ±1 | mV/V |
| Input offset voltage, common mode $V_S$ = 5 V | $V_{OS, cm}$ | ±1.5 | mV |

1/ Deltas are performed at room temperature. 240 hour burn-in and group C end-point electrical parameters.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A, and as specified herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Application notes.

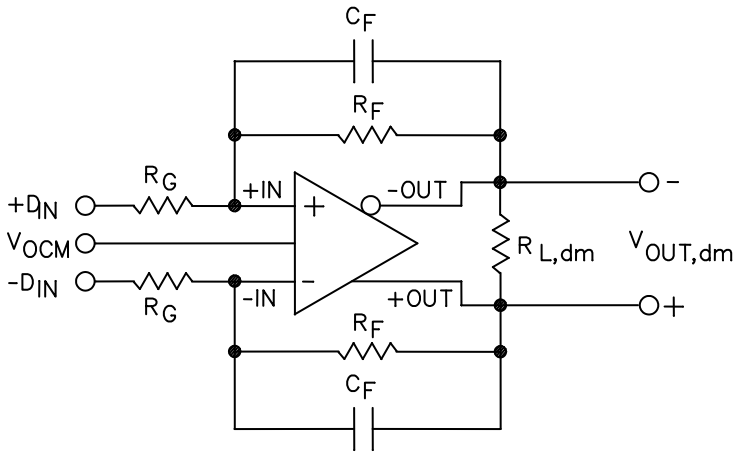



FIGURE 2. Circuit definitions.

Definition of terms

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or equivalently output differential-mode voltage) is defined as $V_{OUT, dm} = (V_{+OUT} - V_{-OUT})$ where $V_{+OUT}$ and $V_{-OUT}$ refer to the voltages at the +OUT and −OUT terminals with respect to a common reference.

Common-mode voltage refers to the average of two node voltages. The output common-mode voltage is defined as $V_{OUT, cm} = (V_{+OUT} + V_{-OUT})/2$. Balance is a measure of how well differential signals are matched in amplitude and exactly 180° apart in phase. Balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the divider's midpoint with the magnitude of the differential signal. By this definition, output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage: Output Balance Error = $|V_{OUT,cm} / V_{OUT,dm}|$.

Theory of operation

The device differs from conventional op amps in that it has two outputs whose voltages move in opposite directions. Like an op amp, it relies on high open-loop gain and negative feedback to force these outputs to the desired voltages. This device behaves much like a standard voltage feedback op amp and makes it easy to perform single-ended-to-differential conversion, common-mode level-shifting, and amplification of differential signals. Also like an op amp, it has high input impedance and low output impedance.

Previous differential drivers, both discrete and integrated designs, have been based on using two independent amplifiers and two independent feedback loops, one to control each of the outputs. When these circuits are driven from a single-ended source, the resulting outputs are typically not well balanced. Achieving a balanced output has typically required exceptional matching of the amplifiers and feedback networks.

DC common-mode level-shifting has also been difficult with previous differential drivers. Level-shifting has required the use of a third amplifier and feedback loop to control the output common-mode level. Sometimes the third amplifier has also been used to attempt to correct an inherently unbalanced circuit. Excellent performance over a wide frequency range has proven difficult with this approach.

6.7 Application notes – continued.

Theory of operation –continued.

The device uses two feedback loops to separately control the differential and common-mode output voltages. The differential feedback, set with external resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to arbitrarily set the output common-mode level. It is forced, by internal common-mode feedback, to be equal to the voltage applied to the $V_{OCM}$ input, without affecting the differential output voltage.

The device architecture results in outputs that are very highly balanced over a wide frequency range without requiring tightly matched external components. The common-mode feedback loop forces the signal component of the output common-mode voltage to be zeroed. The result is nearly perfectly balanced differential outputs of identical amplitude and exactly 180° apart in phase.

Analyzing an application circuit

The device uses high open-loop gain and negative feedback to force its differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled +IN and −IN in Figure 2. For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to $V_{OCM}$ can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

Setting the closed-loop gain

Neglecting the capacitors $C_F$, the differential-mode gain of the circuit in Figure 2 can be determined to be described by $|V_{OUT,dm} / V_{IN,dm}| = R_F/R_G$. This assumes the input resistors, $R_G$, and feedback resistors, $R_F$, on each side are equal.

Estimating the output noise voltage

Similar to the case of a conventional op amp, the differential output errors (noise and offset voltages) can be estimated by multiplying the input referred terms, at +IN and −IN, by the circuit noise gain. The noise gain is defined as $G_N = 1+ R_F/R_G$.

To compute the total output referred noise for the circuit of Figure 2, consideration must also be given to the contribution of the resistors $R_F$ and $R_G$. Refer to table III for the estimated output noise voltage densities at various closed-loop gains.

Table III. Estimated output noise voltage densities at various closed-loop gains.

| Gain | $R_G$ (Ω) | $R_F$ (Ω) | Bandwidth -3 dB | Output noise only | Output noise plus $R_G$, $R_F$ |
|---|---|---|---|---|---|
| 1 | 499 | 499 | 320 MHz | 10 nV/$\sqrt{\text{Hz}}$ | 11.6 nV/$\sqrt{\text{Hz}}$ |
| 2 | 499 | 1.0 k | 180 MHz | 15 nV/$\sqrt{\text{Hz}}$ | 18.2 nV/$\sqrt{\text{Hz}}$ |
| 5 | 499 | 2.49 k | 70 MHz | 30 nV/$\sqrt{\text{Hz}}$ | 37.9 nV/$\sqrt{\text{Hz}}$ |
| 10 | 499 | 4.99 k | 30 MHz | 55 nV/$\sqrt{\text{Hz}}$ | 70.8 nV/$\sqrt{\text{Hz}}$ |

When using this device in gain configurations where RF/RG of one feedback network is unequal to $R_F/R_G$ of the other network, there is a differential output noise due to input-referred voltage in the $V_{OCM}$ circuitry. The output noise is defined in terms of the following feedback terms (refer to Figure 2): $\beta_1 = R_G/(R_F+R_G)$ for −OUT to +IN loop, and $\beta_2 = R_G/(R_F+R_G)$ for +OUT to −IN loop.

With these defined, $V_{nOUT,dm} = 2 \times V_{nIN,VOCM} \times [(\beta_1 - \beta_2)/(\beta_1 + \beta_2)]$ where $V_{nOUT,dm}$ is the output differential noise, and $V_{nIN,VOCM}$ is the input-referred voltage noise in $V_{OCM}$.

6.7 Application notes – continued.

The impact of mismatches in the feedback networks

As previously mentioned, even if the external feedback networks ($R_F/R_G$) are mismatched, the internal common-mode feedback loop still forces the outputs to remain balanced. The amplitudes of the signals at each output remains equal and 180° out of phase. The input-to-output differential-mode gain varies proportionately to the feedback mismatch, but the output balance is unaffected.

Ratio matching errors in the external resistors result in a degradation of the circuit's ability to reject input common-mode signals, much the same as for a four-resistor difference amplifier made from a conventional op amp.

In addition, if the dc levels of the input and output common-mode voltages are different, matching errors result in a small differential-mode output offset voltage. For the G = 1 case, with a ground referenced input signal and the output common-mode level set for 2.5 V, an output offset of as much as 25 mV (1% of the difference in common-mode levels) can result if 1% tolerance resistors are used. Resistors of 1% tolerance result in a worst-case input CMRR of about 40 dB, worst-case differential mode output offset of 25 mV due to 2.5 V level-shift, and no significant degradation in output balance error.

Calculating an application circuit's input impedance

The effective input impedance of a circuit such as the one in Figure 2, at +DIN and –DIN, depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, the input impedance ($R_{IN, dm}$) between the inputs (+DIN and −DIN) is simply:

$$R_{IN, dm} = 2 \times R_G$$

In the case of a single-ended input signal (for example if −DIN is grounded and the input signal is applied to +DIN), the input impedance becomes:

$$R_{IN, dm} = R_G / (1 – (R_F / (2 \times (R_G + R_F))))$$

The circuit's input impedance is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor RG.

Input common-mode voltage range in single supply applications

This device is optimized for level-shifting, ground-referenced input signals. For a single-ended input, this would imply, for example, that the voltage at −DIN in Figure 2 would be 0 V when the amplifier's negative power supply voltage (at V−) is also set to 0 V.

Setting the output common-mode voltage

The device's $V_{OCM}$ pin is internally biased at a voltage approximately equal to the midsupply point (average value of the voltages on V+ and V−). Relying on this internal bias results in an output common-mode voltage that is within about 100 mV of the expected value.

In cases where more accurate control of the output common-mode level is required, it is recommended that an external source, or resistor divider (made up of 10 kΩ resistors), be used. The output common-mode offset listed in table I specifications assumes the $V_{OCM}$ input is driven by a low impedance voltage source.

6.7 Application notes – continued.

Driving a capacitive load

A purely capacitive load can react with the pin and bondwire inductance of the device, resulting in high frequency ringing in the pulse response. One way to minimize this effect is to place a small capacitor across each of the feedback resistors. The added capacitance should be small to avoid destabilizing the amplifier. An alternative technique is to place a small resistor in series with the amplifier's outputs, as shown in Figure 3.

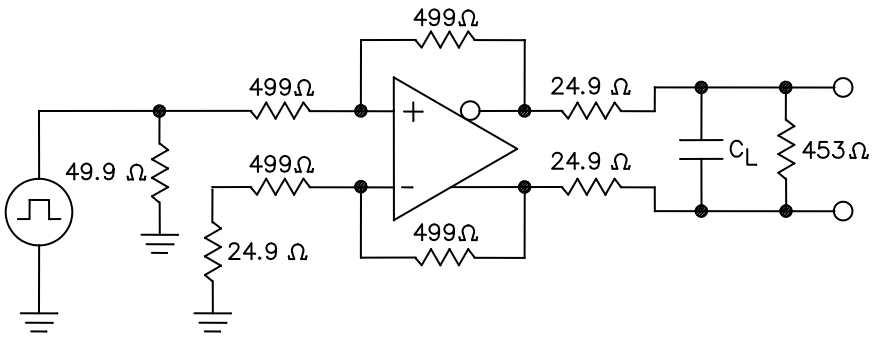



FIGURE 3. Driving capacitive load application.

Layout, grounding, and bypassing

As a high speed part, the device is sensitive to the PCB environment in which it has to operate. Realizing its specifications requires attention to various details of good high speed PCB design.

The first requirement is for a good solid ground plane that covers as much of the board area around the device as possible. The only exception to this is that the two input pins (pin 2 and pin 9) should be kept a few millimeters from the ground plane, and ground should be removed from inner layers and the opposite side of the board under the input pins. This minimizes the stray capacitance on these nodes and helps preserve the gain flatness vs. frequency.

The power supply pins should be bypassed as close as possible to the device to the nearby ground plane. Good high frequency ceramic chip capacitors should be used. This bypassing should be done with a capacitance value of 0.01 µF to 0.1 µF for each supply. Further away, low frequency bypassing should be provided with 10 µF tantalum capacitors from each supply to ground.

The signal routing should be short and direct to avoid parasitic effects. Wherever there are complementary signals, a symmetrical layout should be provided to the extent possible to maximize the balance performance. When running differential signals over a long distance, the traces on the PCB should be close together or any differential wiring should be twisted together to minimize the area of the loop that is formed. This reduces the radiated energy and makes the circuit less susceptible to interference.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-04-28

Approved sources of supply for SMD 5962-09220 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962R0922001VHA | 24355 | AD8138AL/QMLR |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 24355 | Analog Devices<br>Route 1 Industrial Park<br>P.O. Box 9106<br>Norwood, MA 02062<br>Point of contact: 7910 Triad Center Drive<br>Greensboro, NC 27409-9605 |

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.