ANALOG DEVICES

Precision, Low Power BiFET Op Amp

AD548

FEATURES

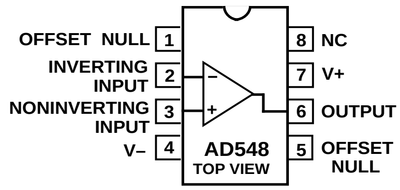
Enhanced Replacement for LF441 and TL061
DC Performance:
- **200 µA max Quiescent Current**
- **10 pA max Bias Current, Warmed Up (AD548C)**
- **250 µV max Offset Voltage (AD548C)**
- **2 µV/°C max Drift (AD548C)**
- **2 µV p-p Noise, 0.1 Hz to 10 Hz**

AC Performance:
- **1.8 V/µs Slew Rate**
- **1 MHz Unity Gain Bandwidth**

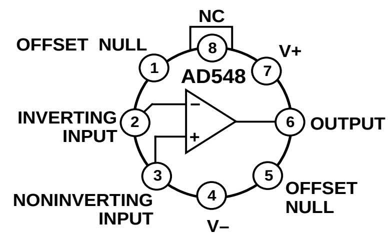
Available in Plastic, Hermetic Cerdip and Hermetic Metal Can Packages and in Chip Form
Available in Tape and Reel in Accordance with EIA-481A Standard
MIL-STD-883B Parts Available
Dual Version Available: AD648
Surface Mount (SOIC) Package Available

CONNECTION DIAGRAMS

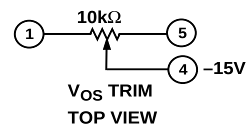
Plastic Mini-DIP (N) Package, Cerdip (Q) Package and SOIC (R)Package



TO-99 (H) Package



NOTE : PIN 4 CONNECTED TO CASE
NC = NO CONNECT



PRODUCT DESCRIPTION

The AD548 is a low power, precision monolithic operational amplifier. It offers both low bias current (10 pA max, warmed up) and low quiescent current (200 µA max) and is fabricated with ion-implanted FET and laser wafer trimming technologies. Input bias current is guaranteed over the AD548's entire common-mode voltage range.

The economical J grade has a maximum guaranteed input offset voltage of less than 2 mV and an input offset voltage drift of less than 20 µV/°C. The C grade reduces input offset voltage to less than 0.25 mV and offset voltage drift to less than 2 µV/°C. This level of dc precision is achieved utilizing Analog's laser wafer drift trimming process. The combination of low quiescent current and low offset voltage drift minimizes changes in input offset voltage due to self-heating effects. Four additional grades are offered over the commercial, industrial and military temperature ranges.

The AD548 is recommended for any dual supply op amp application requiring low power and excellent dc and ac performance. In applications such as battery-powered, precision instrument front ends and CMOS DAC buffers, the AD548's excellent combination of low input offset voltage and drift, low bias current and low 1/f noise reduces output errors. High common-mode rejection (86 dB, min on the "C" grade) and high open-loop gain ensures better than 12-bit linearity in high impedance, buffer applications.

The AD548 is pinned out in a standard op amp configuration and is available in six performance grades. The AD548J and AD548K are rated over the commercial temperature range of 0°C to +70°C. The AD548A, AD548B and AD548C are rated over the industrial temperature range of –40°C to +85°C. The AD548S is rated over the military temperature range of –55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD548 is available in an 8-pin plastic mini-DIP, cerdip, TO-99 metal can, surface mount (SOIC), or in chip form.

PRODUCT HIGHLIGHTS

1. A combination of low supply current, excellent dc and ac performance and low drift makes the AD548 the ideal op amp for high performance, low power applications.
2. The AD548 is pin compatible with industry standard op amps such as the LF441, TL061, and AD542, enabling designers to improve performance while achieving a reduction in power dissipation of up to 85%.
3. Guaranteed low input offset voltage (2 mV max) and drift (20 µV/°C max) for the AD548J are achieved utilizing Analog Devices' laser drift trimming technology, eliminating the need for external trimming.
4. Analog Devices specifies each device in the warmed-up condition, insuring that the device will meet its published specifications in actual use.
5. A dual version, the AD648 is also available.
6. Enhanced replacement for LF441 and TL061.

REV. B

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AD548–SPECIFICATIONS (@ +25°C and V_S = ±15 V dc unless otherwise noted)

Model	AD548J/A/S			AD548K/B			AD548C			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.75	2.0		0.3	0.5		0.10	0.25	mV
T_{MIN} to T_{MAX}			3.0/3.0/3.0			0.7/0.8			0.4	mV
vs. Temperature			20			5			2.0	µV/°C
vs. Supply	80			86			86			dB
vs. Supply, T_{MIN} to T_{MAX}	76/76/76			80			80			dB
Long-Term Offset Stability		15			15			15		µV/Month
INPUT BIAS CURRENT										
Either Input[2], V_{CM} = 0		5	20		3	10		3	10	pA
Either Input[2] at T_{MAX}, V_{CM} = 0			0.45/1.3/20			0.25/0.65			0.65	nA
Max Input Bias Current Over Common-Mode Voltage Range			30			15			15	pA
Offset Current, V_{CM} = 0		5	10		2	5		2	5	pA
Offset Current at T_{MAX}			0.25/0.65/10			0.15/0.35			0.35	nA
INPUT IMPEDANCE										
Differential		$1 \times 10^{12} \parallel 3$			$1 \times 10^{12} \parallel 3$			$1 \times 10^{12} \parallel 3$		Ω∥pF
Common Mode		$3 \times 10^{12} \parallel 3$			$3 \times 10^{12} \parallel 3$			$3 \times 10^{12} \parallel 3$		Ω∥pF
INPUT VOLTAGE RANGE										
Differential[3]		±20			±20			±20		V
Common Mode	±11	±12		±11	±12		±11	±12		V
Common-Mode Rejection										
V_{CM} = ±10 V	76	90		82	92		86	98		dB
T_{MIN} to T_{MAX}	76/76/76	90		82	92		86	98		dB
V_{CM} = ±11 V	70	84		76	86		76	90		dB
T_{MIN} to T_{MAX}	70/70/70	84		76	86		76	90		dB
INPUT VOLTAGE NOISE										
Voltage 0.1 Hz to 10 Hz		2			2			2	4.0	µV p-p
f = 10 Hz		80			80			80		nV/√Hz
f = 100 Hz		40			40			40		nV/√Hz
f = 1 kHz		30			30			30		nV/√Hz
f = 10 kHz		30			30			30		nV/√Hz
INPUT CURRENT NOISE										
f = 1 kHz		1.8			1.8			1.8		fA/√Hz
FREQUENCY RESPONSE										
Unity Gain, Small Signal	0.8	1.0		0.8	1.0		0.8	1.0		MHz
Full Power Response		30			30			30		kHz
Slew Rate, Unity Gain	1.0	1.8		1.0	1.8		1.0	1.8		V/µs
Settling Time to ±0.01%		8			8			8		µs
OPEN LOOP GAIN										
V_O = ±10 V, R_L ≥ 10 kΩ	300	1000		300	1000		300	1000		V/mV
T_{MIN} to T_{MAX}, R_L ≥ 10 kΩ	300/300/300	700		300	700		300	700		V/mV
V_O = ±10 V, R_L ≥ 5 kΩ	150	500		150	500		150	500		V/mV
T_{MIN} to T_{MAX}, R_L ≥ 5 kΩ	150/150/150	300		150	300		150	300		V/mV
OUTPUT CHARACTERISTICS										
Voltage @ R_L ≥ 10 kΩ,	±12	±13		±12	±13		±12	±13		V
T_{MIN} to T_{MAX}	±12/±12/±12			±12			±12			
Voltage @ R_L ≥ 5 kΩ,	±11	±12.3		±11	±12.3		±11	±12.3		V
T_{MIN} to T_{MAX}	±11/±11/±11			±11			±11			
Short Circuit Current		15			15			15		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current		170	200		170	200		170	200	µA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0°C to +70°C)		AD548J			AD548K					
Industrial (–40°C to +85°C)		AD548A			AD548B			AD548C		
Military (–55°C to +125°C)		AD548S								
PACKAGE OPTIONS										
SOIC (R-8)	AD548JR			AD548KR, AD548BR						
Plastic (N-8)	AD548JN			AD548KN						
Cerdip (Q-8)	AD548AQ							AD548CQ		
Metal Can (H-08A)	AD548AH			AD548BH						
Tape and Reel	AD548JR-REEL			AD548KR-REEL, AD548BR-REEL						
Chips Available	AD548JCHIPS									

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.

[3]Defined as voltages between inputs, such that neither exceeds ±10 V from ground.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18 V
Internal Power Dissipation[2]	500 mW
Input Voltage[3]	±18 V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range (Q, H)	–65°C to +150°C
(N, R)	–65°C to +125°C
Operating Temperature Range	
AD548J/K	0°C to +70°C
AD548A/B/C	–40°C to +85°C
AD548S	–55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	+300°C

NOTES

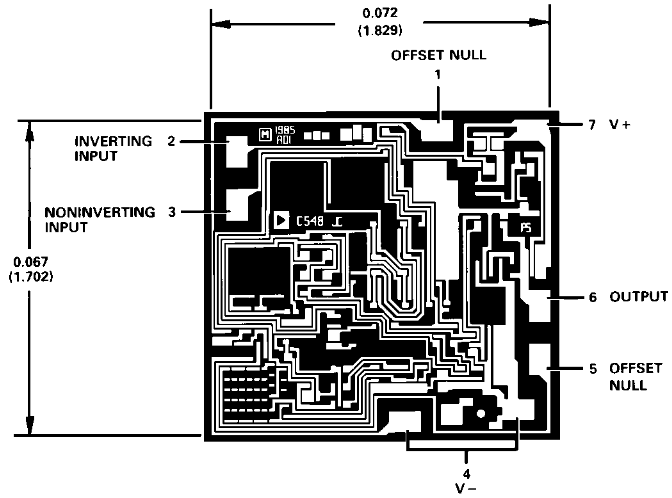
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics: 8-Pin SOIC Package: θ_{JA} = 160°C/W, θ_{JC} = 42°C/W; 8-Pin Plastic Package: θ_{JA} = 90°C/W; 8-Pin Cerdip Package: θ_{JC} = 22°C/W, θ_{JA} = 110°C/W; 8-Pin Metal Can Package: θ_{JC} = 65°C/W, θ_{JA} = 150°C/W.

[3]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions



Typical Characteristics

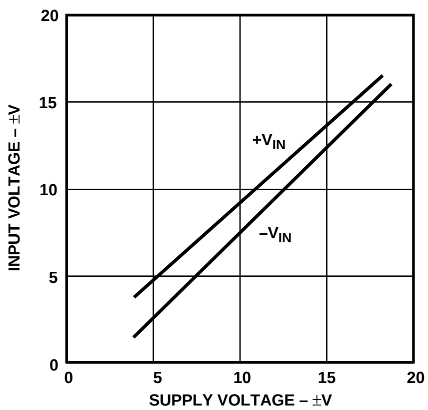


Figure 1. Input Voltage Range vs. Supply Voltage

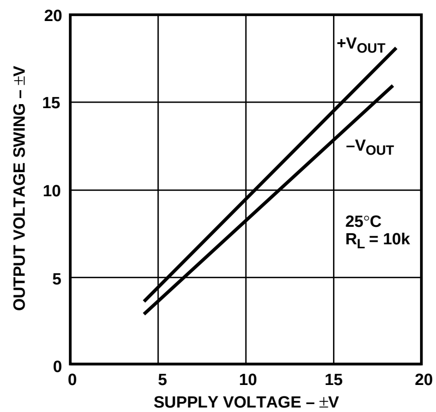


Figure 2. Output Voltage Swing vs. Supply Voltage

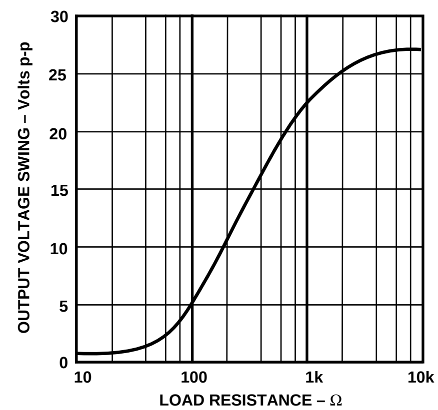


Figure 3. Output Voltage Swing vs. Load Resistance

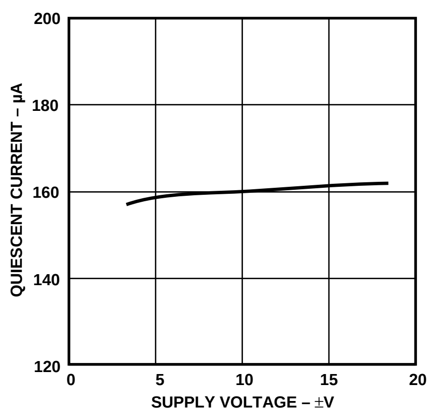


Figure 4. Quiescent Current vs. Supply Voltage

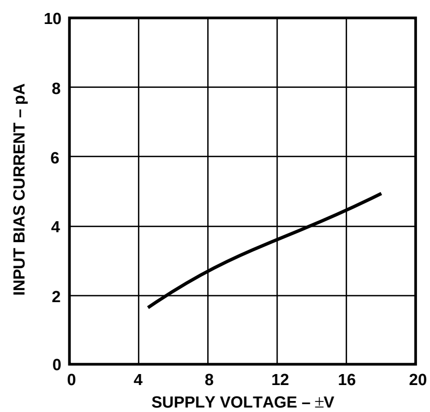


Figure 5. Input Bias Current vs. Supply Voltage

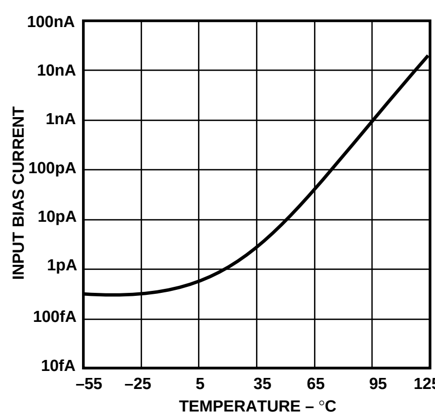


Figure 6. Input Bias Current vs. Temperature

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD548 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

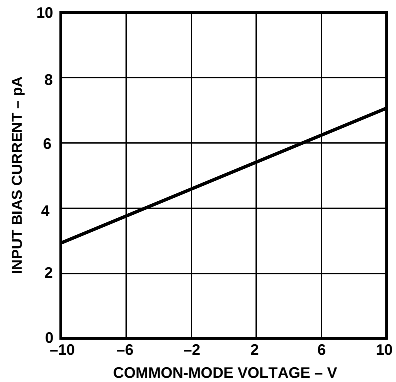


Figure 7. Input Bias Current vs. Common-Mode Voltage

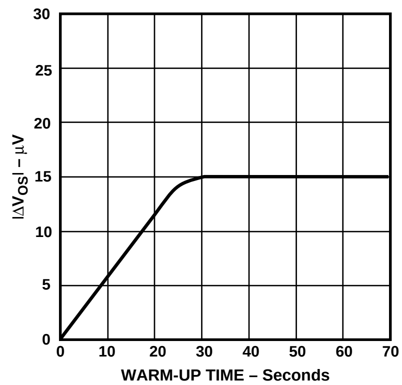


Figure 8. Change in Offset Voltage vs. Warm-Up Time

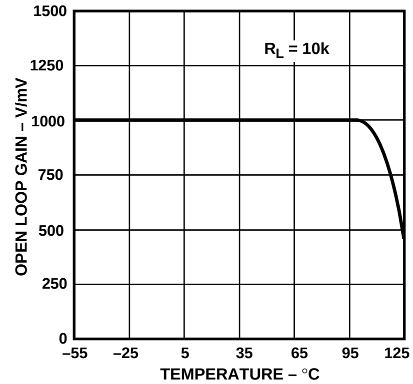


Figure 9. Open Loop Gain vs. Temperature

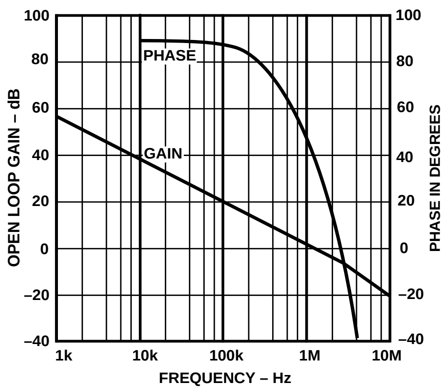


Figure 10. Open Loop Frequency Response

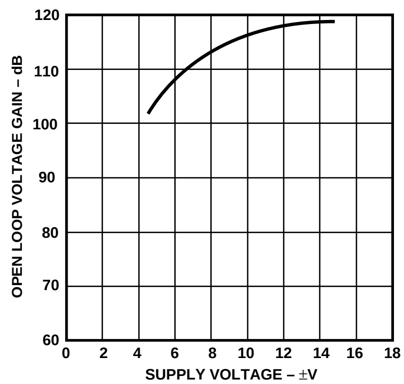


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

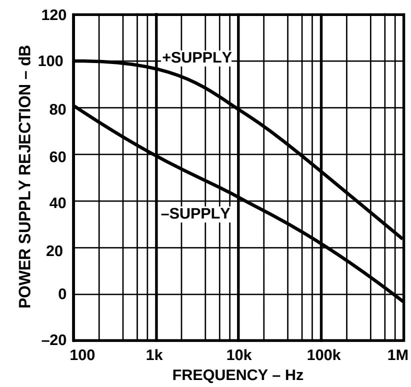


Figure 12. PSRR vs. Frequency

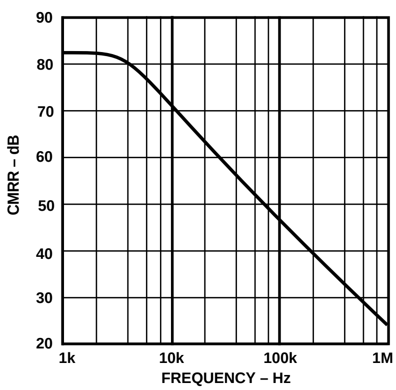


Figure 13. CMRR vs. Frequency

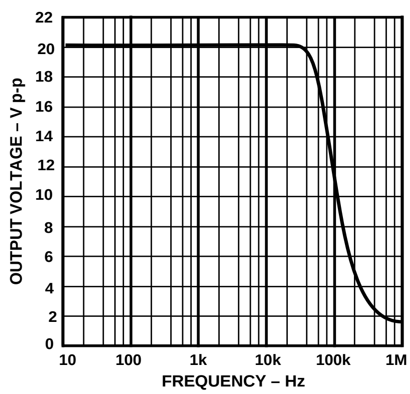


Figure 14. Large Signal Frequency Response

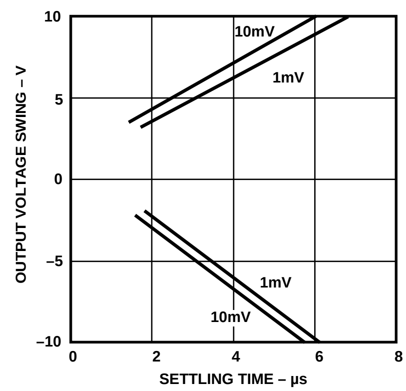


Figure 15. Output Swing and Error Voltage vs. Output Settling Time

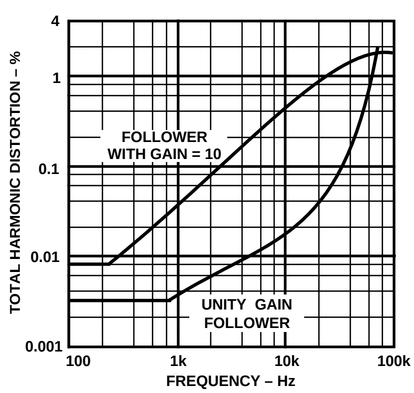


Figure 16. Total Harmonic Distortion vs. Frequency

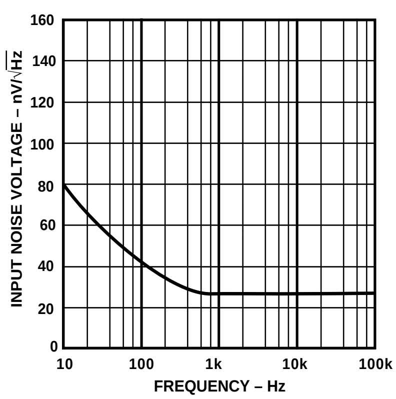


Figure 17. Input Noise Voltage Spectral Density

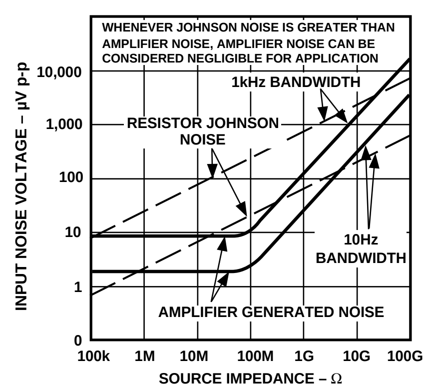


Figure 18. Total Noise vs. Source Impedance

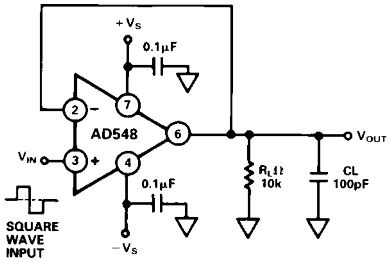


Figure 19a. Unity Gain Follower

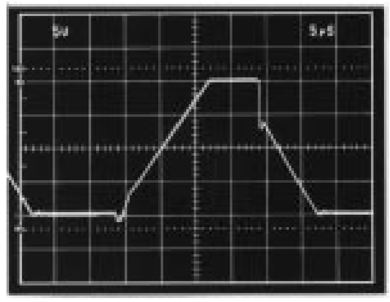


Figure 19b. Unity Gain Follower Pulse Response (Large Signal)

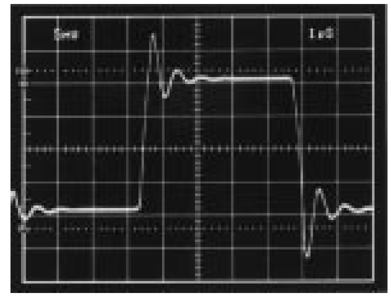


Figure 19c. Unity Gain Follower Pulse Response (Small Signal)

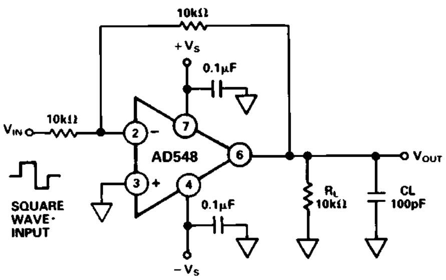


Figure 20a. Utility Gain Inverter

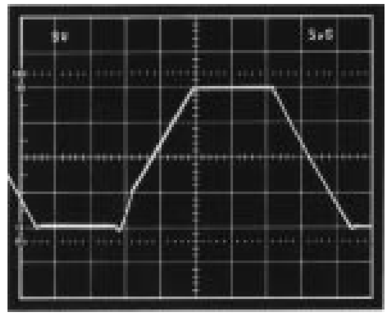


Figure 20b. Utility Gain Inverter Pulse Response (Large Signal)

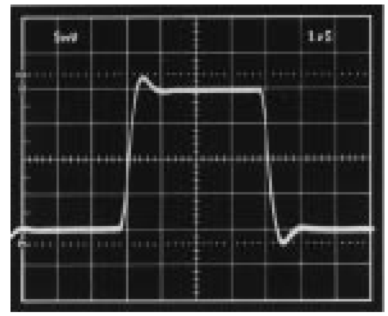


Figure 20c. Unity Gain Inverter Pulse Response (Small Signal)

APPLICATION NOTES

The AD548 is a JFET-input op amp with a guaranteed maximum I_B of less than 10 pA, and offset and drift laser-trimmed to 0.25 mV and 2 µV/°C respectively (AD548C). AC specs include 1 MHz bandwidth, 1.8 V/µs typical slew rate and 8 µs settling time for a 20 V step to ±0.01%—all at a supply current less than 200 µA. To capitalize on the device's performance, a number of error sources should be considered.

The minimal power drain and low offset drift of the AD548 reduce self-heating or "warm-up" effects on input offset voltage, making the AD548 ideal for on/off battery powered applications. The power dissipation due to the AD548's 200 µA supply current has a negligible effect on input current, but heavy output loading will raise the chip temperature. Since a JFET's input current doubles for every 10°C rise in chip temperature, this can be a noticeable effect.

The amplifier is designed to be functional with power supply voltages as low as ±4.5 V. It will exhibit a higher input offset voltage than at the rated supply voltage of ±15 V, due to power supply rejection effects. The common-mode range of the AD548 extends from 3 V more positive than the negative supply to 1 V more negative than the positive supply. Designed to cleanly drive up to 10 kΩ and 100 pF loads, the AD548 will drive a 2 kΩ load with reduced open loop gain.

OFFSET NULLING

Unlike bipolar input amplifiers, zeroing the input offset voltage of a BiFET op amp will not minimize offset drift. Using balance Pins 1 and 5 to adjust the input offset voltage as shown in Figure 21 will induce an added drift of 0.24 µV/°C per 100 µV of nulled offset. The low initial offset (0.25 mV) of the AD548C results in only 0.6 µV/°C of additional drift.

Applying the AD548

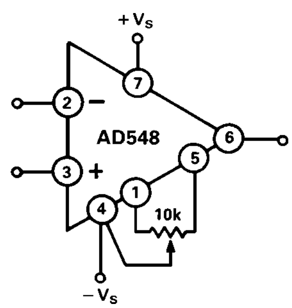


Figure 21. Offset Null Configuration

LAYOUT

To take full advantage of the AD548's 10 pA max input current, parasitic leakages must be kept below an acceptable level. The practical limit of the resistance of epoxy or phenolic circuit board material is between 1×10^{12} Ω and 3×10^{12} Ω. This can result in an additional leakage of 5 pA between an input of 0 V and a –15 V supply line. Teflon or a similar low leakage material (with a resistance exceeding 10^{17} Ω) should be used to isolate high impedance input lines from adjacent lines carrying high voltages. The insulator should be kept clean, since contaminants will degrade the surface resistance.

A metal guard completely surrounding the high impedance nodes and driven by a voltage near the common-mode input potential can also be used to reduce some parasitic leakages. The guarding pattern in Figure 22 will reduce parasitic leakage due to finite board surface resistance; but it will not compensate for a low volume resistivity board.

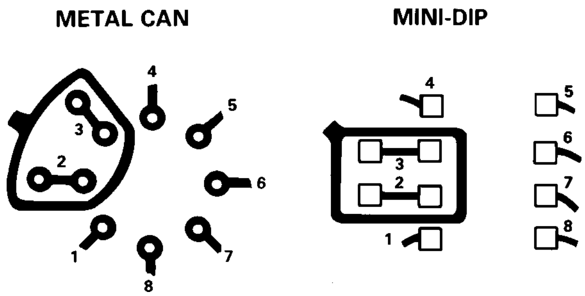


Figure 22. Board Layout for Guarding Inputs

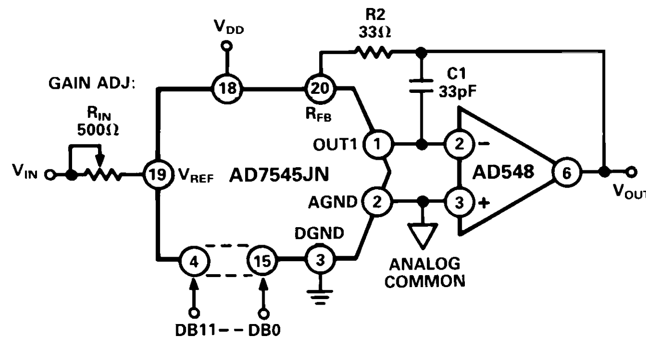


Figure 24. AD548 Used as DAC Output Amplifier

INPUT PROTECTION

The AD548 is guaranteed to withstand input voltages equal to the power supply potential. Exceeding the negative supply voltage on either input will forward bias the substrate junction of the chip. The induced current may destroy the amplifier due to excess heat.

Input protection is required in applications such as a flame detector in a gas chromatograph, where a very high potential may be applied to the input terminals during a sensor fault condition. Figure 23 shows a simple current limiting scheme that can be used. $R_{PROTECT}$ should be chosen such that the maximum overload current is 1.0 mA (l00 kΩ for a 100 V overload, for example).

Exceeding the negative common-mode range on either input terminal causes a phase reversal at the output, forcing the amplifier output to the corresponding high or low state. Exceeding the negative common-mode on both inputs simultaneously forces the output high. Exceeding the positive common-mode range on a single input doesn't cause a phase reversal, but if both inputs exceed the limit the output will be forced high. In all cases, normal amplifier operation is resumed when input voltages are brought back within the common-mode range.

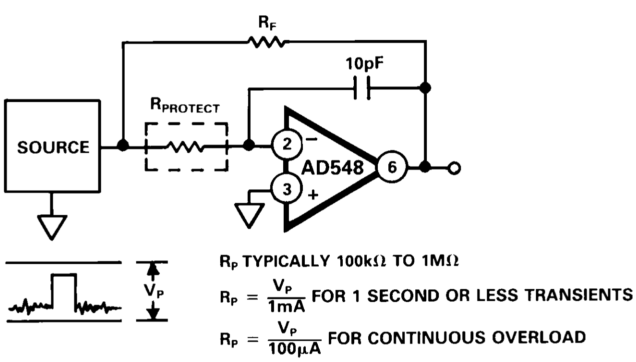


Figure 23. Input Protection of IV Converter

D/A CONVERTER OUTPUT BUFFER

The circuit in Figure 24 shows the AD548 and AD7545 12-bit CMOS D/A converter in a unipolar binary configuration. V_{OUT} will be equal to V_{REF} attenuated by a factor depending on the digital word. V_{REF} sets the full scale. Overall gain is trimmed by adjusting R_{IN}. The AD548's low input offset voltage, low drift and clean dynamics make it an attractive low power output buffer.

The input offset voltage of the AD548 output amplifier results in an output error voltage. This error voltage equals the input offset voltage of the op amp times the noise gain of the amplifier.

That is:

$$V_{OS}\ Output = V_{OS}\ Input\left(1+\frac{R_{FB}}{R_O}\right)$$

R_{FB} is the feedback resistor for the op amp, which is internal to the DAC. R_O is the DAC's R-2R ladder output resistance. The value of R_O is code dependent. This has the effect of changing the offset error voltage at the amplifier's output. An output amplifier with a sub millivolt input offset voltage is needed to preserve the linearity of the DAC's transfer function.

The AD548 in this configuration provides a 700 kHz small signal bandwidth and 1.8 V/µs typical slew rate. The 33 pF capacitor across the feedback resistor optimizes the circuit's response. The oscilloscope photos in Figures 25 and 26 show small and large signal outputs of the circuit in Figure 24. Upper traces show the input signal V_{IN}. Lower traces are the resulting output voltage with the DAC's digital input set to all 1s. The AD548 settles to ±0.01% for a 20 V input step in 14 µs.

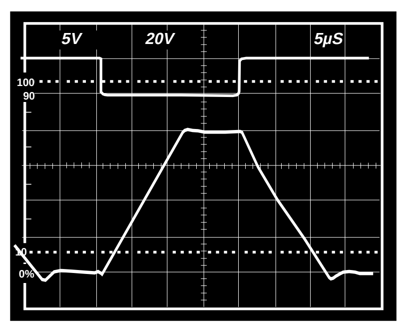


Figure 25. Response to ±20 V p-p Reference Square Wave

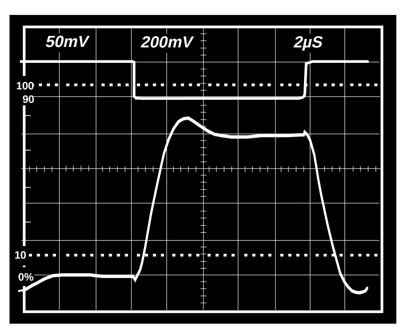


Figure 26. Response to ±100 mV p-p Reference Square Wave

PHOTODIODE PREAMP

The performance of the photodiode preamp shown in Figure 27 is enhanced by the AD548's low input current, input voltage offset and offset voltage drift. The photodiode sources a current proportional to the incident light power on its surface. R_F converts the photodiode current to an output voltage equal to $R_F \times I_S$.

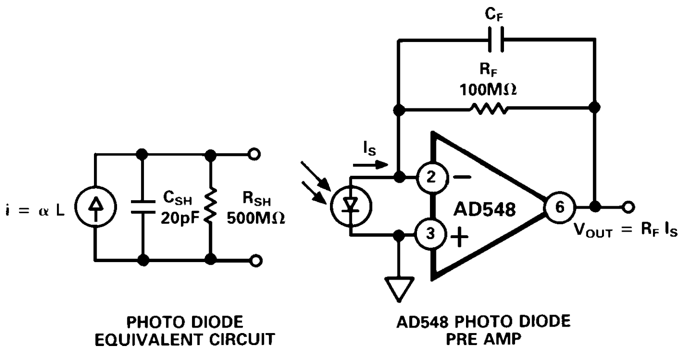


Figure 27.

An error budget illustrating the importance of low amplifier input current, voltage offset and offset voltage drift to minimize output voltage errors can be developed by considering the equivalent circuit for the small (0.2 mm^2 area) photodiode shown in Figure 27. The input current results in an error proportional to the feedback resistance used. The amplifier's offset will produce an error proportional to the preamp's noise gain ($I + R_F/R_{SH}$), where R_{SH} is the photodiode shunt resistance. The amplifier's input current will double with every 10°C rise in temperature, and the photodiode's shunt resistance halves with every 10°C rise. The error budget in Figure 28 assumes a room temperature photodiode R_{SH} of 500 MΩ, and the maximum input current and input offset voltage specs of an AD548C.

TEMP °C	R_{SH} (MΩ)	V_{OS} (μV)	(1+ R_F/R_{SH}) V_{OS}	I_B (pA)	$I_B R_F$	TOTAL
–25	15,970	150	151 μV	0.30	30 μV	181 μV
0	2,830	200	207 μV	2.26	262 μV	469 μV
+25	500	250	300 μV	10.00	1.0 mV	1.30 mV
+50	88.5	300	640 μV	56.6	5.6 mV	6.24 mV
+75	15.6	350	2.6 mV	320	32 mV	34.6 mV
+85	7.8	370	5.1 mV	640	64 mV	69.1 mV

Figure 28. Photo Diode Pre-Amp Errors Over Temperature

The capacitance at the amplifier's negative input (the sum of the photodiode's shunt capacitance, the op amp's differential input capacitance, stray capacitance due to wiring, etc.) will cause a rise in the preamp's noise gain over frequency. This can result in excess noise over the bandwidth of interest. C_F reduces the noise gain "peaking" at the expense of bandwidth.

INSTRUMENTATION AMPLIFIER

The AD548C's maximum input current of 10 pA makes it an excellent building block for the high input impedance instrumentation amplifier shown in Figure 29. Total current drain for this circuit is under 600 μA. This configuration is optimal for conditioning differential voltages from high impedance sources.

The overall gain of the circuit is controlled by R_G, resulting in the following transfer function:

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{(R_1 + R_2)}{R_G}$$

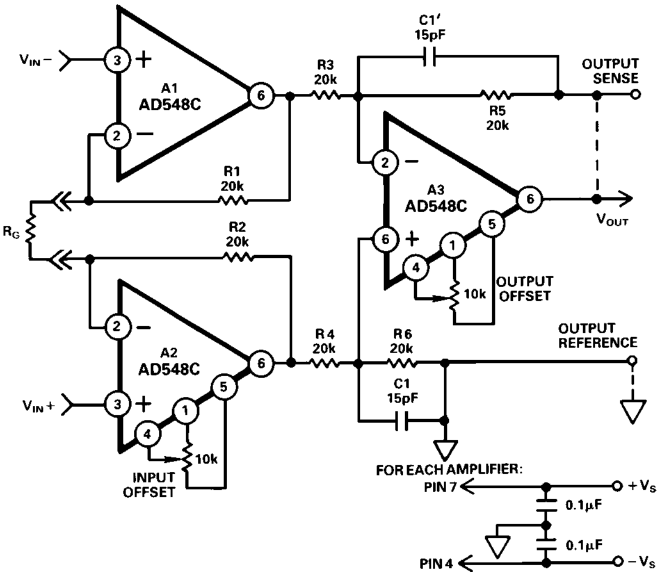


Figure 29. Low Power Instrumentation Amplifier

Gains of 1 to 100 can be accommodated with gain nonlinearities of less than 0.01%. Referred to input errors, which contribute an output error proportional to in amp gain, include a maximum untrimmed input offset voltage of 0.5 mV and an input offset voltage drift over temperature of 4 μV/°C. Output errors, which are independent of gain, will contribute an additional 0.5 mV offset and 4 μV/°C drift. The maximum input current is 15 pA over the common-mode range, with a common-mode impedance of over 1×10^{12} Ω. Resistor pairs R3/R5 and R4/R6 should be ratio matched to 0.01% to take full advantage of the AD548's high common-mode rejection. Capacitors C1 and C1′ compensate for peaking in the gain over frequency caused by input capacitance when gains of 1 to 3 are used.

The –3 dB small signal bandwidth for this low power instrumentation amplifier is 700 kHz for a gain of 1 and 10 kHz for a gain of 100. The typical output slew rate is 1.8 V/μs.

LOG RATIO AMPLIFIER

Log ratio amplifiers are useful for a variety of signal conditioning applications, such as linearizing exponential transducer outputs and compressing analog signals having a wide dynamic range. The AD548's picoamp level input current and low input offset voltage make it a good choice for the front-end amplifier of the log ratio circuit shown in Figure 30. This circuit produces an output voltage equal to the log base 10 of the ratio of the input currents I_1 and I_2. Resistive inputs R1 and R2 are provided for voltage inputs.

Input currents I_1 and I_2 set the collector currents of Q1 and Q2, a matched pair of logging transistors. Voltages at points A and B are developed according to the following familiar diode equation:

$$V_{BE} = (kT/q) \ln (I_C/I_{ES})$$

In this equation, k is Boltzmann's constant, T is absolute temperature, q is an electron charge, and I_{ES} is the reverse saturation current of the logging transistors. The difference of these two voltages is taken by the subtractor section and scaled by a factor of approximately 16 by resistors R9, R10, and R8. Temperature

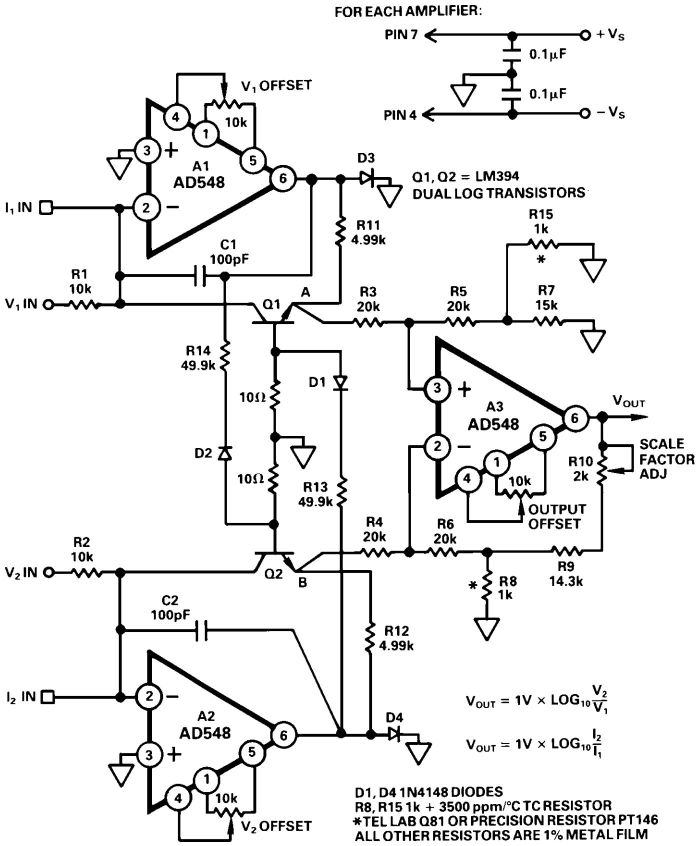


Figure 30. Log Ratio Amplifier

compensation is provided by resistors R8 and R15, which have a positive 3500 ppm/°C temperature coefficient. The transfer function for the output voltage is:

$$V_{OUT} = 1V \log_{10}(I_2/I_1)$$

Frequency compensation is provided by R11, R12, C1, and C2. Small signal bandwidth is approximately 300 kHz at input currents above 100 µA and will proportionally decrease with lower signal levels. D1, D2, R13, and R14 compensate for the effects of the two logging transistors' ohmic emitter resistance.

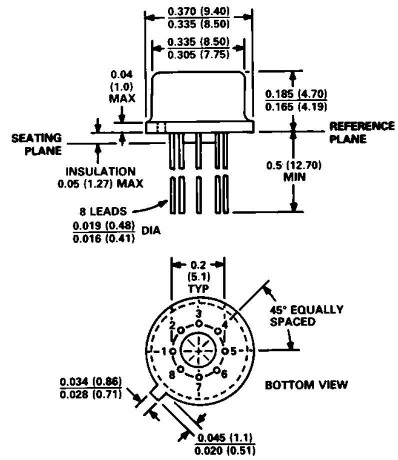
To trim this circuit, set the two input currents to 10 µA and adjust V_{OUT} to zero by adjusting the potentiometer on A3. Then set I_2 to 1 µA and adjust the scale factor such that the output voltage is 1 V by trimming potentiometer R10. Offset adjustment for A1 and A2 is provided to increase the accuracy of the voltage inputs.

This circuit ensures a 1% log conformance error over an input current range of 300 pA to 1 mA, with low level accuracy limited by the AD548's input current. The low level input voltage accuracy of this circuit is limited by the input offset voltage and drift of the AD548.

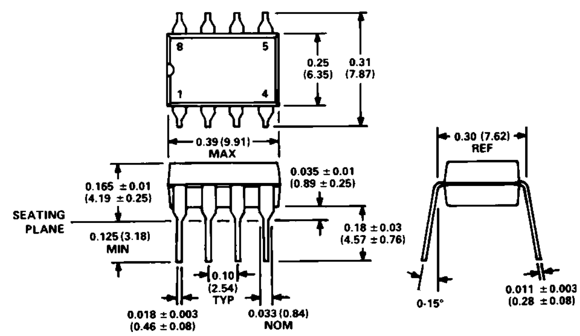
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

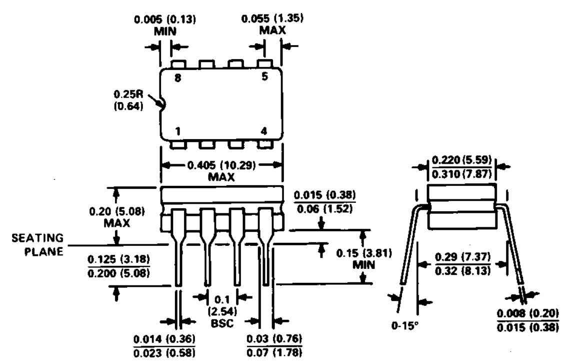
TO-99 (H) Package



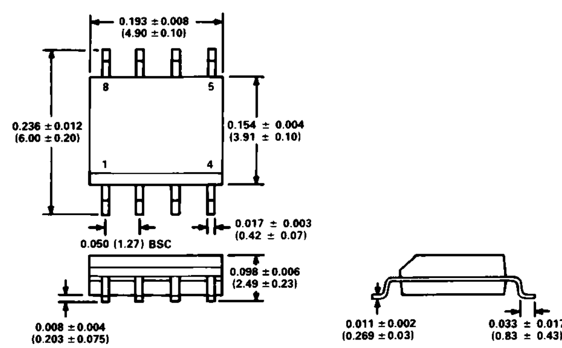
Plastic Mini-DIP (N) Package



Cerdip (Q) Package



SOIC (R) Package



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