S71NS-R Memory Subsystem Solutions

MirrorBit® 1.8 Volt-Only Simultaneous Read/Write, Burst Mode Multiplexed Flash Memory and Burst Mode pSRAM

512 Mb (32 Mb x 16-bit) and 256 Mb (16 Mb x 16-bit) Flash, 128 Mb (8 Mb x 16-bit) and 64 Mb (4 Mb x 16-bit) pSRAM

Data Sheet

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S71NS-R_00 **Revision** 09 **Issue Date** January 29, 2014

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Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

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Data Sheet

Features

- **Power supply voltage of 1.7V to 1.95V**
- **Burst Speed (Flash and pSRAM): 104 MHz**
- **MCP BGA Package**
  - 56 ball, 9.2 x 8.0 mm, 0.5 mm ball pitch
  - 56 ball, 7.7 x 6.2 mm, 0.5 mm ball pitch
- **Operating Temperature**
  - Wireless, –25°C to +85°C

General Description

The S71NS-R Series is a product line of stacked Multi-Chip Package (MCP) memory solutions and consists of the following items:

- One or more S29NS-R flash memory die
- One or more pSRAM

The products covered by this document are listed in the table below. For details about their specifications, please refer to their individual data sheet for further details.

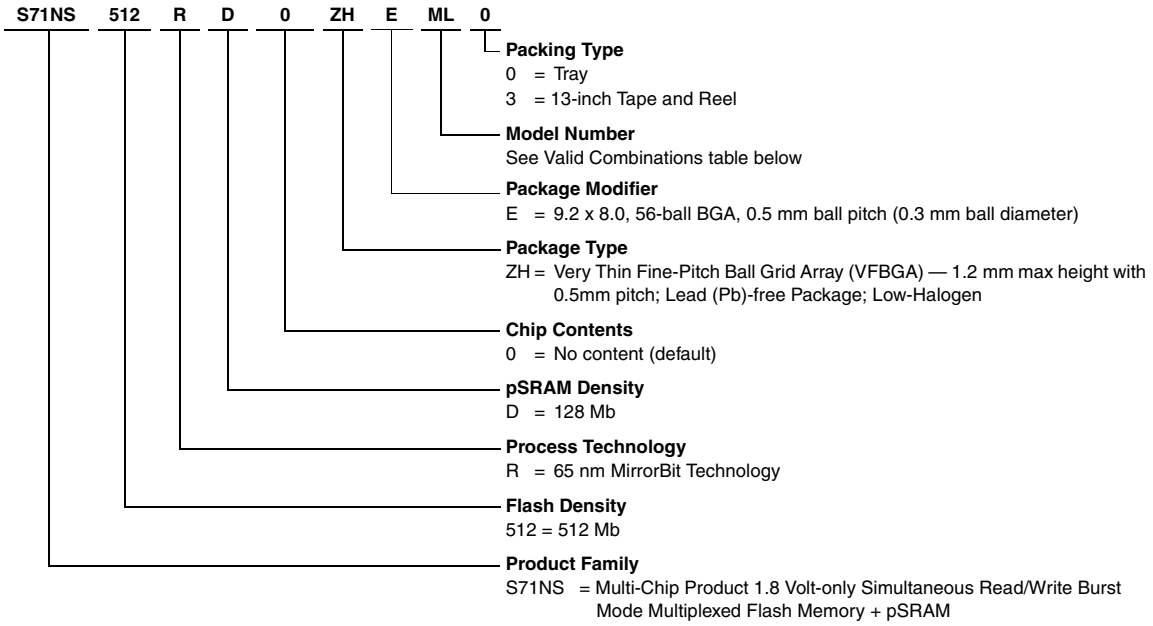
Flash Density	pSRAM Density	Product
512 Mb	128 Mb	S71NS512RD0

For detailed specifications, please refer to the individual data sheets:

Document	Publication Identification Number
S29NS-R	S29NS-R_00
128-Mb CellularRAM Address/Data Multiplexed	SWM128D108M1R

1. Ordering Information

The order number is formed by a valid combinations of the following:



1.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Base Ordering Part Number	Package	Model Number	Packing Type	pSRAM Type	MCP Speed	Boot	Package Type
S71NS512RD0	ZHE	UL	0, 3	SWM128D108M1R	104 MHz	Uniform	NLB056

2. Input/Output Descriptions

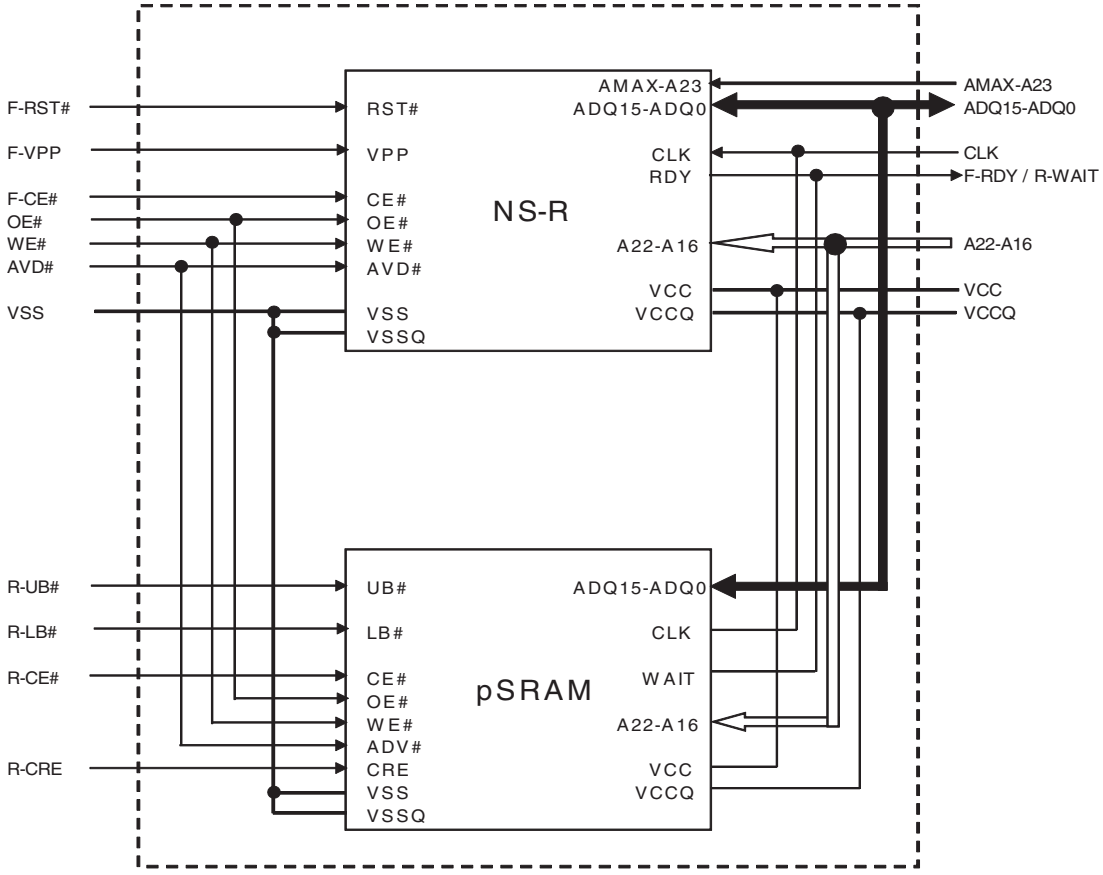
Table 2.1 identifies the input and output package connections provided on the device.

Table 2.1 Input/Output Descriptions

Symbol	Description	Flash	RAM
AMAX – A16	Address inputs	X	X
A/DQ15-A/DQ0	Multiplexed Address/Data	X	X
OE#	Output Enable input. Asynchronous relative to CLK for the Burst mode.	X	X
WE#	Write Enable input.	X	X
V_{SS}	Ground	X	X
V_{SSQ}	Input/Output Ground	X	X
F-RDY/R-WAIT	Ready output; indicates the status of the Burst read. Flash Memory RDY (using default “Active HIGH” configuration) V_{OL} = data invalid V_{OH} = data valid Note: The default polarity for the pSRAM WAIT signal is opposite the default polarity of the Flash RDY signal. pSRAM WAIT (using default “Active HIGH” configuration) V_{OL} = data valid V_{OH} = data invalid To match polarities, change bit 10 of the pSRAM Bus Configuration Register to 0 (Active LOW WAIT). Alternately, change bit 10 of the Flash Configuration Register to 0 (Active LOW RDY)	X	X
CLK	Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at V_{IL} or V_{IH} while in asynchronous mode	X	X
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs. Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched. High = device ignores address inputs	X	X
F-RST#	Hardware reset input. Low = device resets and returns to reading array data	X	
F-WP#	Hardware write protect input. At V_{IL}, disables program and erase functions in the four outermost sectors. Should be at V_{IH} for all other conditions.	X	
F-V_{PP}	Accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.	X	
R-CE#	Chip-enable input for pSRAM.		X
F-CE#	Chip-enable input for Flash. Asynchronous relative to CLK for Burst Mode.	X	
R-CRE	Control Register Enable (pSRAM).		X
V_{CC}	Flash and pSRAM 1.8 Volt-only single power supply.	X	X
V_{CCQ}	Flash and pSRAM Input/Output Power Supply	X	X
R-UB#	Upper Byte Control (pSRAM).		X
R-LB#	Lower Byte Control (pSRAM)		X
DNU	Do Not Use. A device internal signal may be connected to the package connector. The connection may be used by Spansion for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections.		
NC	Not Connected. No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB).		
RFU	Reserved For Future Use. No device internal signal is currently connected to the package connector but there is potential future use for the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.		

3. MCP Block Diagram

Figure 3.1 MCP Block Diagram



4. Connection Diagrams/Physical Dimensions

This section contains the I/O designations and package specifications for the S71NS-R.

4.1 Special Handling Instructions for FBGA Packages

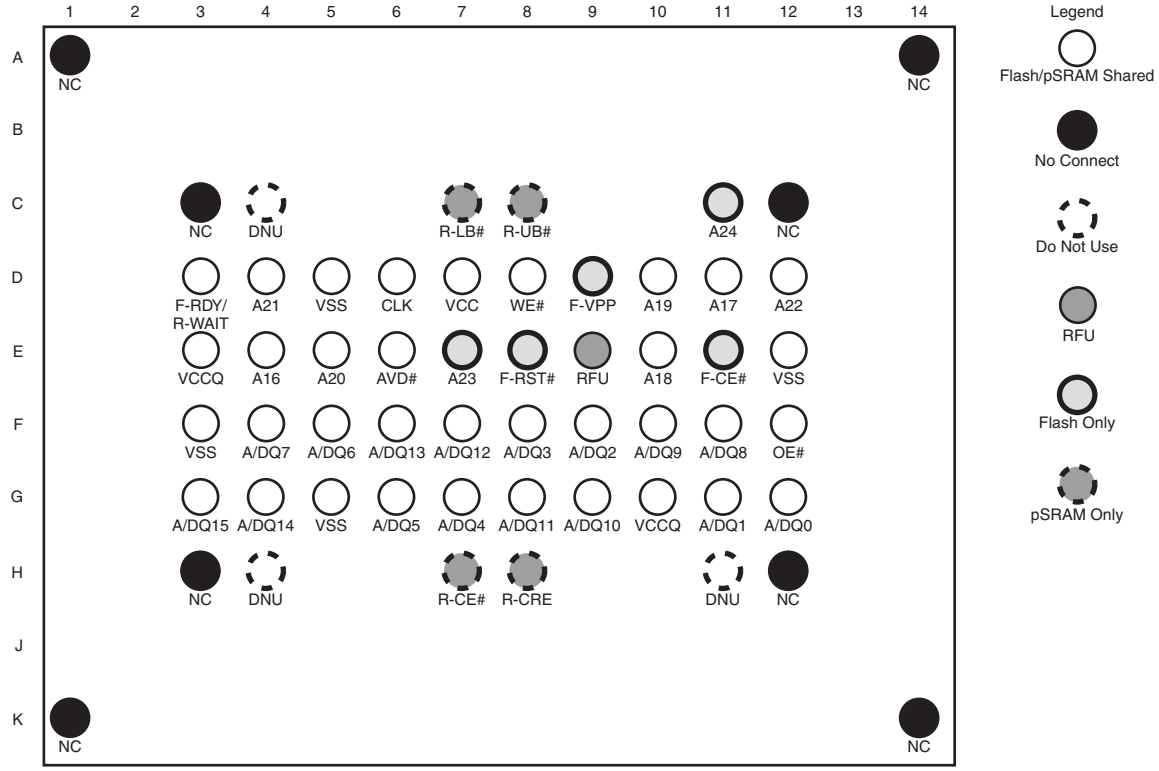
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

4.2 Connection Diagrams

Figure 4.1 56-ball Fine-Pitch Ball Grid Array

(Top View, Balls Facing Down)

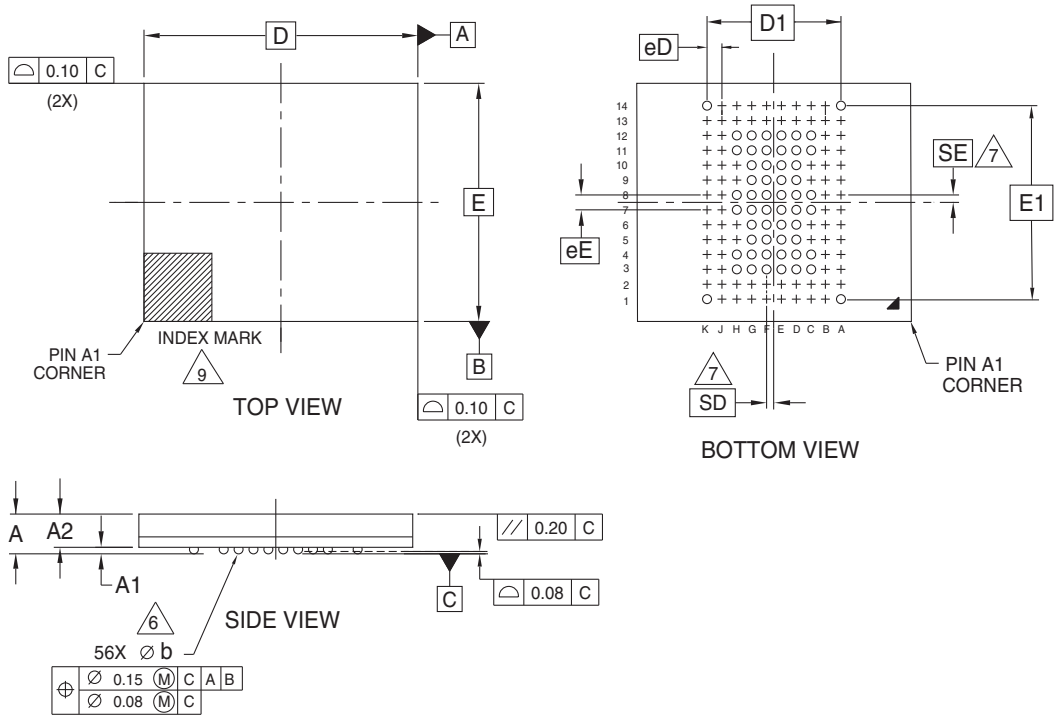


Note:
Addresses are shared between Flash and RAM depending on the density of the pSRAM.

MCP	Flash-Only Addresses	Shared Addresses	Shared ADQ Pins
S71NS512RD0	A24-A23	A22-A16	A/DQ15-A/DQ0

4.3 Physical Dimensions

Figure 4.2 NLB056—56-ball VFBGA 9.2 x 8.0 mm



PACKAGE	NLB 056			
JEDEC	N/A			
D x E	9.20 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.85	---	0.97	BODY THICKNESS
D	9.20 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	4.50 BSC.			MATRIX FOOTPRINT
E1	6.50 BSC.			MATRIX FOOTPRINT
MD	10			MATRIX SIZE D DIRECTION
ME	14			MATRIX SIZE E DIRECTION
n	56			BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
eE	0.50 BSC.			BALL PITCH
eD	0.50 BSC			BALL PITCH
SD / SE	0.25 BSC.			SOLDER BALL PLACEMENT
	A2 – A13,B1 – B14 C1,C2,C5,C6,C9,C10,C13,C14 D1,D2,D13,D14,E1,E2,E13,E14,F1,F2,F13,F14 G1,G2,G13,G14,H1,H2,H5,H6,H9,H10,H13,H14 J1 – J14, K2 – K13			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

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5. Revision History

Section	Description
Revision 01 (January 14, 2008)	
	Initial release
Revision 02 (February 11, 2008)	
Global	Added OPN S71NS256RC0ZHKJL
Revision 03 (September 10, 2008)	
Global	Added OPN S71NS512RD0ZHEKL
Revision 04 (October 6, 2008)	
Global	Removed OPNs S71NS256RC0ZHKJL, S71NS256RD0ZHEJL, and S71NS512RD0ZHEJL
Physical Dimensions	Removed packages NLD056 and NSB056
Revision 05 (April 9, 2009)	
Physical Dimensions	Updated package drawing for NLB056
Revision 06 (July 23, 2009)	
Global	Added OPN S71NS256RD0AHKKL0, S71NS256RC0AHKJL0
General Description	Added 256 Mb Flash and 64 Mb pSRAM
Valid Combinations	Added Package Type to table
Physical Dimensions	Added figure RSD056—56-ball VFBGA 7.7 x 6.2 mm
Revision 07 (August 3, 2010)	
General Description	Updated MUX pSRAM Type 3 to SWM064D108M1N Added reference for SWM128D133M1R
Ordering Information	Removed 7 inch Tape and Reel option
Valid Combinations	Added OPN S71NS512RD0ZHEML Updated MUX pSRAM Type 3 entries to SWM064D108M1N
Input/Output Descriptions	Refreshed DNU, NC, RFU definitions
MCP Block Diagram	Updated MCP Block Diagram
Connection Diagrams	Updated 56-ball Fine-Pitch Ball Grid Array
Revision 08 (May 17, 2011)	
General Description	Updated SWM064D108M1N reference to SWM064D108M1R
Valid Combinations	Added OPN S71NS256RC0AHKKL, Removed OPN S71NS256RC0AHKJL
Physical Dimensions	Added figure RLA056—56-ball VFBGA 7.7 x 6.2 mm
Revision 09 (January 29, 2014)	
General Description	Removed: 256Mb Flash + 64Mb pSRAM and 256Mb Flash + 128Mb psRAM Removed: SWM064D108M1R and MUX pSRAM Type 5 from Documents Table
Valid Combinations	Removed S71NS256RC0AHKKL, S71NS256RD0AHK, S71NS512RD0ZHEKL, S71NS512RD0ZHEML Added: S71NS512RD0ZHEUL
Connection Diagrams	Figure 4.1 ‘56-ball Fine-Pitch Ball Grid Array’: Removed S71NS256RD0 and S71NS256RC0 from associated table Removed Figure RSD056 - 56ball VFBGA 7.7 x 6.2 mm Removed Figure RLA056 - 56ball VFBGA 7.7 x 6.2 mm

Colophon

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