120 Watt, GaN Flange Mount MMIC Power Amplifier, 2.7 GHz to 3.8 GHz

Preliminary Technical Data

HMC7327

FEATURES

High P_{SAT}: 51 dBm
Power gain at P_{SAT}: 20 dB
Small signal gain: 26 dB
Supply Voltage
  V_{DD} = 32 V at 1400 mA
50 Ω matched input and output
10-lead flange package

APPLICATIONS

Test instrumentation
General communications
Radar

GENERAL DESCRIPTION

The HMC7327 is a 120 W gallium nitride (GaN), MMIC power amplifier that operates between 2.7 GHz and 3.8 GHz, packaged in a 10-lead flange mount package.

The amplifier typically provides 26 dB of small signal gain and 51 dBm saturated output power. The amplifier draws 1400 mA quiescent current from a 32 V dc supply. For ease of use, the RF input/outputs are dc blocked and matched to 50 Ω.

FUNCTIONAL BLOCK DIAGRAM

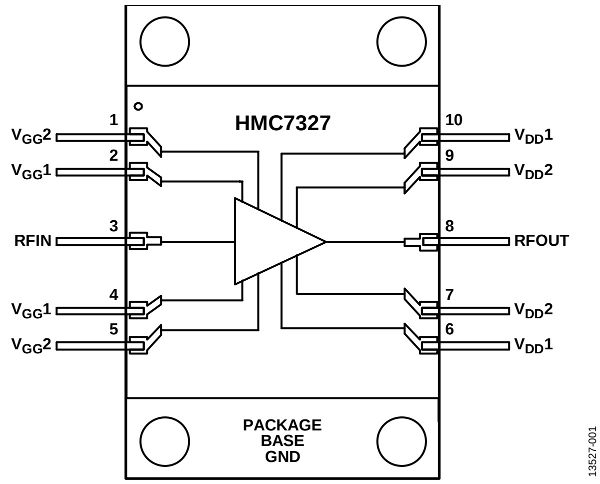

Figure 1.

Rev. PrA Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support **www.analog.com**

HMC7327* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMC7327 Evaluation Board

DOCUMENTATION

Data Sheet

- HMC7327: 120 Watt, GaN Flange Mount MMIC Power Amplifier, 2.7 GHz to 3.8 GHz Preliminary Data Sheet

DESIGN RESOURCES

- HMC7327 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMC7327 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, V_{DD} = 32 V, I_{DD} = 1400 mA, PW = 100 µs, duty cycle = 10, frequency range = 2.7 GHz to 3.2 GHz.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		2.7		3.2	GHz	
GAIN						Measured continuous wave (CW)
Small Signal Gain		24	26		dB	
Gain Flatness			±0.5		dB	
Gain Variation over Temperature			0.03		dB/°C	
RETURN LOSS						Measured CW
Input			25		dB	
Output			22		dB	
POWER						
Output Power for 4 dB Compression	P4dB		45		dBm	
Power Gain for P4dB			24		dB	
Saturated Output Power	P_{SAT}		51		dBm	P_{SAT} is defined as the output power at P_{IN} = 31 dBm at 25°C
Power Gain for P_{SAT}			20		dB	P_{SAT} is defined as the output power at P_{IN} = 31 dBm at 25°C
Power Added Efficiency	PAE		49		%	PAE at P_{SAT} is defined as the output power at P_{IN} = 31 dBm at 25°C
TOTAL SUPPLY CURRENT	I_{DD}		1400		mA	Adjust the gate bias voltage (V_{GGx}) between −8 V and 0 V to achieve an I_{DD} = 1400 mA, typical

T_A = 25°C, V_{DD} = 32 V, I_{DD} = 1400 mA, PW = 100 µs, duty cycle= 10, frequency range = 3.2 GHz to 3.8 GHz.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		3.2		3.8	GHz	
GAIN						Measured CW
Small Signal Gain		24	26		dB	
Gain Flatness			±0.5		dB	
Gain Variation over Temperature			0.03		dB/°C	
RETURN LOSS						Measured CW
Input			30		dB	
Output			18		dB	
POWER						
Output Power for 4 dB Compression	P4dB		47.5		dBm	
Power Gain for P4dB			24		dB	
Saturated Output Power	P_{SAT}		50.5		dBm	P_{SAT} is defined as the output power at P_{IN} = 31 dBm at 25°C
Power Gain for P_{SAT}			19.5		dB	P_{SAT} is defined as the output power at P_{IN} = 31 dBm at 25°C
Power Added Efficiency	PAE		49		%	PAE at P_{SAT} is defined as the output power at P_{IN} = 31 dBm at 25°C
TOTAL SUPPLY CURRENT	I_{DD}		1400		mA	Adjust the gate bias voltage (V_{GGx}) between −8 V and 0 V to achieve an I_{DD} = 1400 mA, typical

TOTAL SUPPLY CURRENT BY V_{DD}

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT	I_{DD}					Adjust the gate bias voltage (V_{GGx}) between −8 V and 0 V to achieve an I_{DD} = 1400 mA, typical
V_{DD} = 24 V			1400		mA	
V_{DD} = 28 V			1400		mA	
V_{DD} = 32 V			1400		mA	

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Drain Bias Voltage (V_{DDx})	36 V
Gate Bias Voltage (V_{GGx})	−8 V to 0 V
RF Input Power (RFIN)	34 dBm
Channel Temperature	225°C
Continuous P_{DISS} (T = 85°C) (Derate TBD mw/°C above 85°C)	143 W
Thermal Resistance[1] (Channel to Die Bottom)	0.98°C/W
Maximum Voltage Standing Wave Ratio (VSWR)[2]	TBD
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C

[1] Junction to back of package. Continuous wave (CW) operation.
[2] Restricted by maximum power dissipation.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

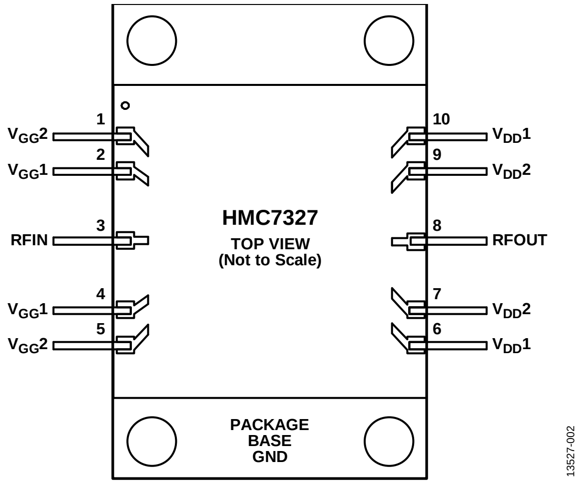

Figure 2. Pin Configuration

Table 5. Pad Function Descriptions

Pad No.	Mnemonic	Description
1, 5	V_{GG2}	Gate Control Voltage for Second Stage. See Figure 3 for the V_{GG2} interface schematic.
2, 4	V_{GG1}	Gate Control Voltage for First Stage. See Figure 4 for the V_{GG1} interface schematic.
3	RFIN	RF Input. This pin is dc-coupled and matched to 50 Ω. See Figure 5 for the RFIN interface schematic.
6, 10	V_{DD1}	Drain Bias for First Stage. See Figure 6 for the V_{DD1} interface schematic.
7, 9	V_{DD2}	Drain Bias for Second Stage. See Figure 7 for the V_{DD2} interface schematic.
8	RFOUT	RF Output. This pad is RF-coupled and matched to 50 Ω. See Figure 8 for the RFOUT interface schematic.

INTERFACE SCHEMATICS

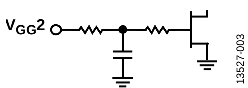

Figure 3. V_{GG2} Interface

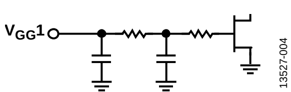

Figure 4. V_{GG1} Interface

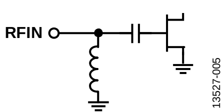

Figure 5. RFIN Interface

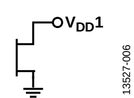

Figure 6. V_{DD1} Interface

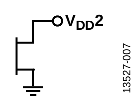

Figure 7. V_{DD2} Interface

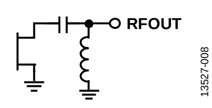

Figure 8. RFOUT Interface

TYPICAL PERFORMANCE CHARACTERISTICS

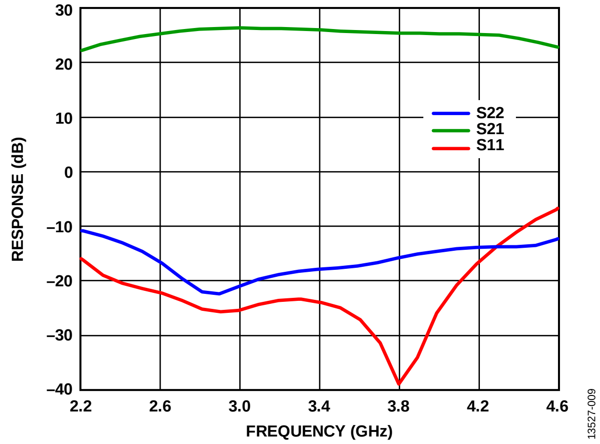

Figure 9. Gain and Return Loss, Measured CW

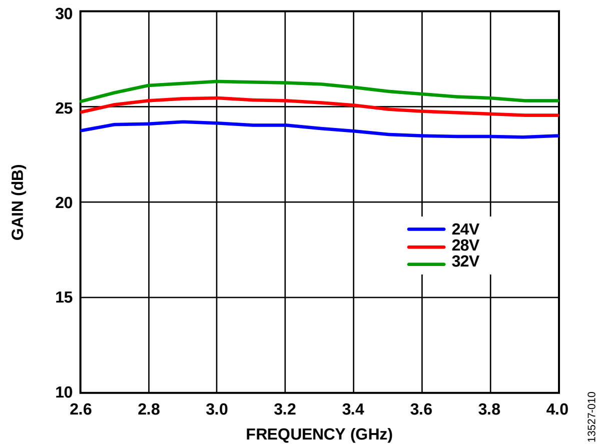

Figure 10. Gain vs. Frequency at Various V_{DD}, Measured CW

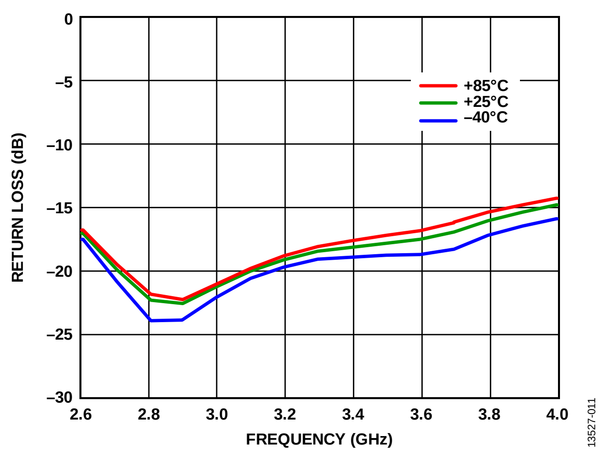

Figure 11. Output Return Loss vs. Frequency at Various Temperatures, Measured CW

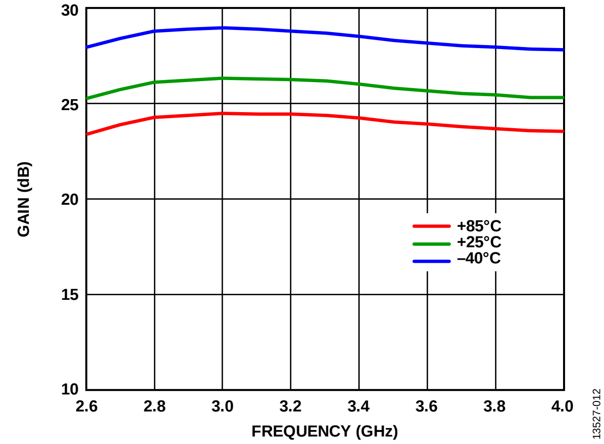

Figure 12. Gain vs. Frequency at Various Temperatures, Measured CW

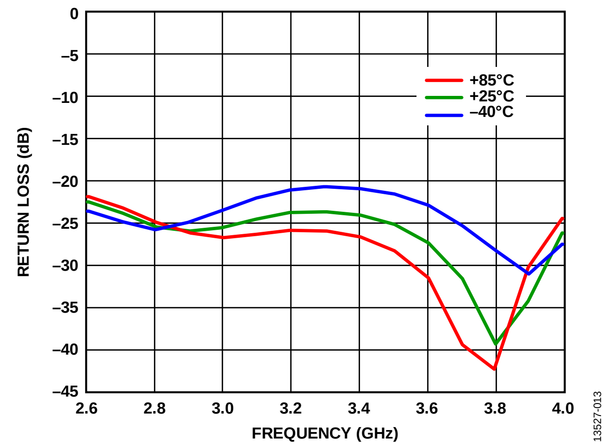

Figure 13. Input Return Loss vs. Frequency at Various Temperatures, Measured CW

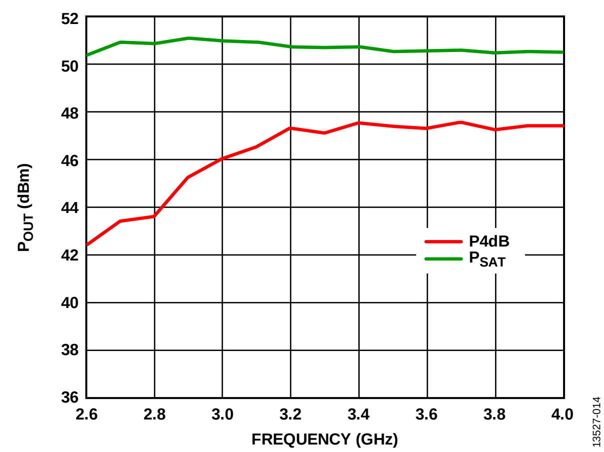

Figure 14. P_{OUT} vs. Frequency, P_{SAT} is Output Power at P_{IN} = 31 dBm at 25°C

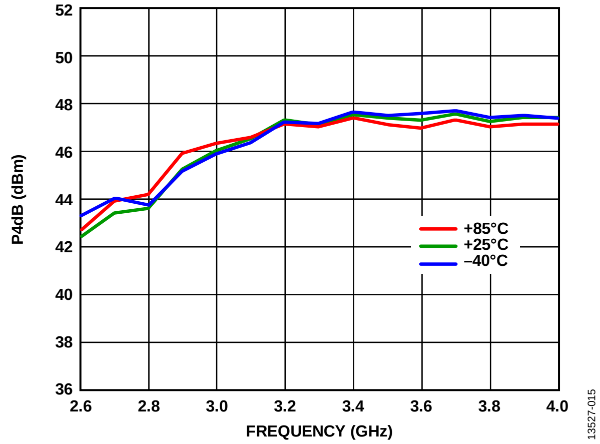

Figure 15. P4dB vs. Frequency at Various Temperatures

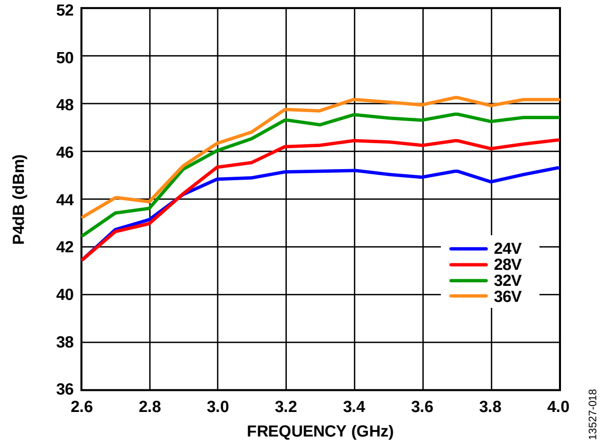

Figure 18. P4dB vs. Frequency at Various Supply Voltages

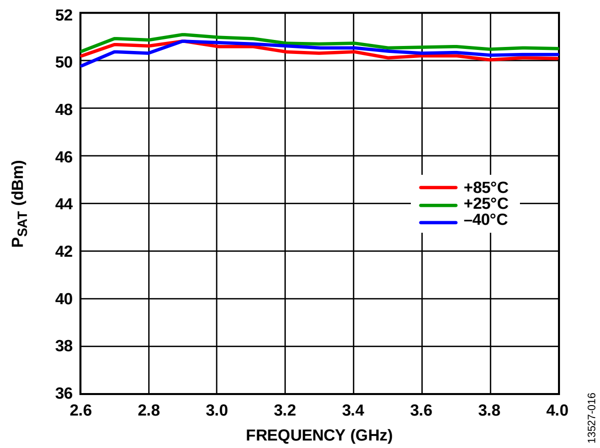

Figure 16. P_{SAT} vs. Frequency at Various Temperatures, P_{SAT} Defined as Output Power at P_{IN} = 31 dBm at +25°C, P_{IN} = 32 dBm at +85°C, P_{IN} = 29 dBm at −40°C

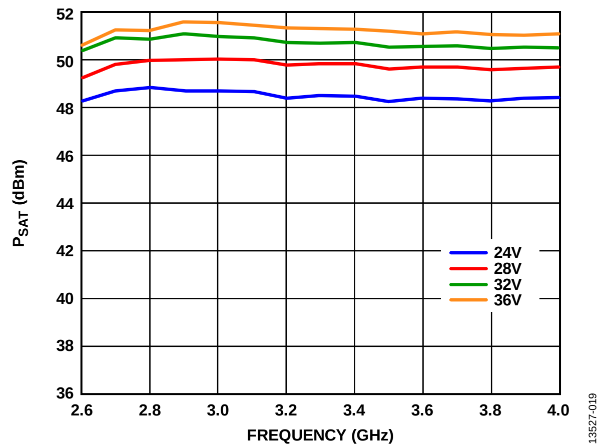

Figure 19. P_{SAT} vs. Frequency at Various Supply Voltages, P_{SAT} Defined as Output Power at P_{IN} = 31 dBm at 25°C

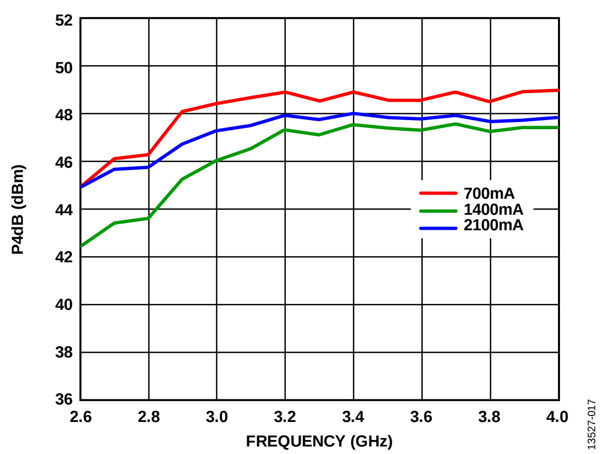

Figure 17. P4dB vs. Frequency at Various Quiescent Currents

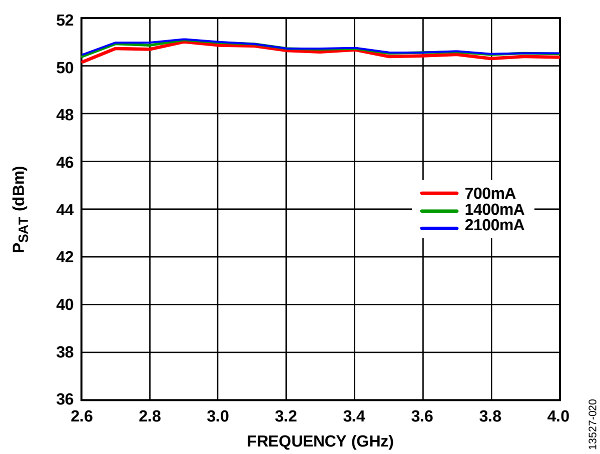

Figure 20. P_{SAT} vs. Frequency at Various Quiescent Currents, P_{SAT} Defined as Output Power at P_{IN} = 31 dBm at 25°C

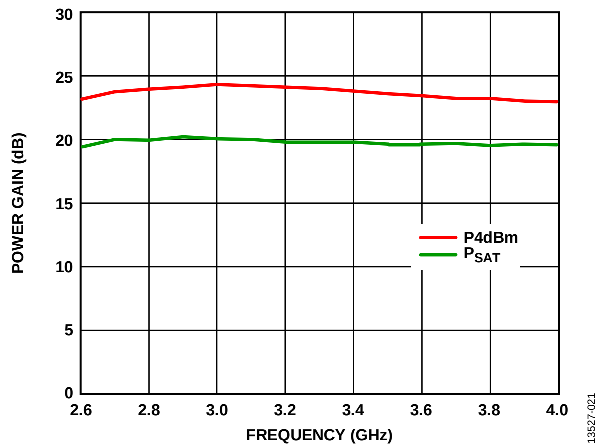

Figure 21. Power Gain vs. Frequency, Power Gain at P_{SAT} Defined as Output Power at P_{IN} = 31 dBm at 25°C

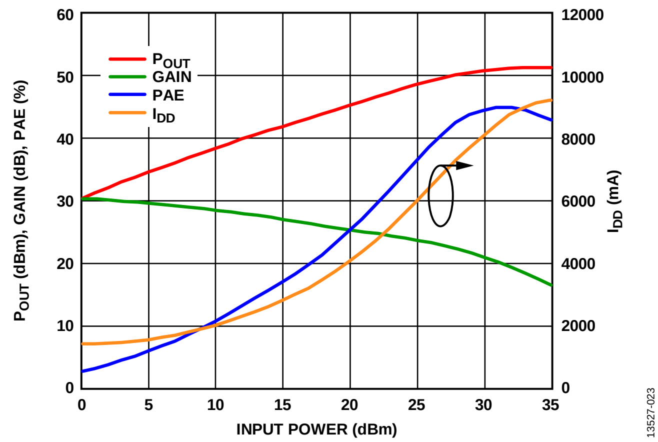

Figure 24. Power Compression at 2.7 GHz

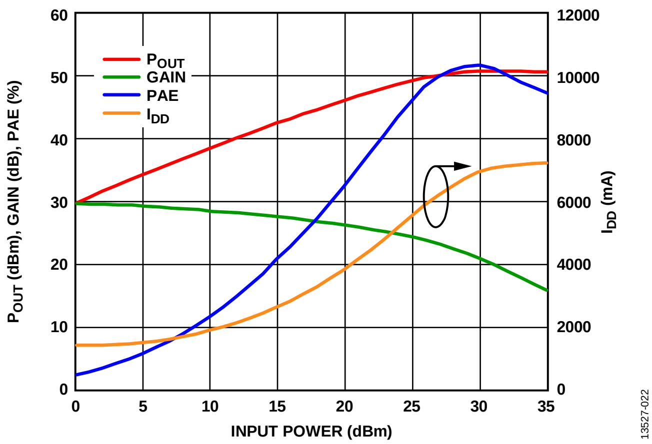

Figure 22. Power Compression at 3.2 GHz

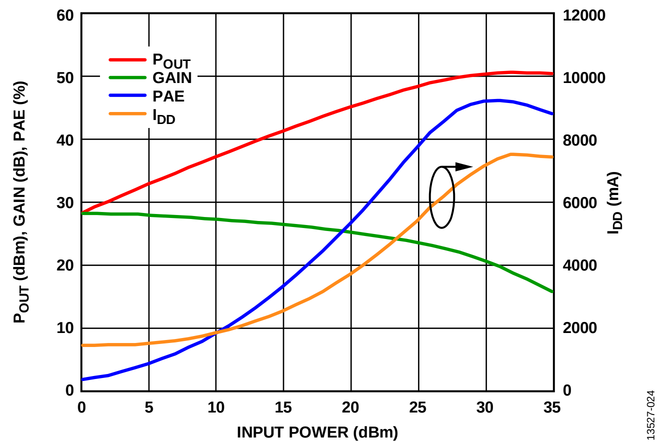

Figure 25. Power Compression at 3.8 GHz

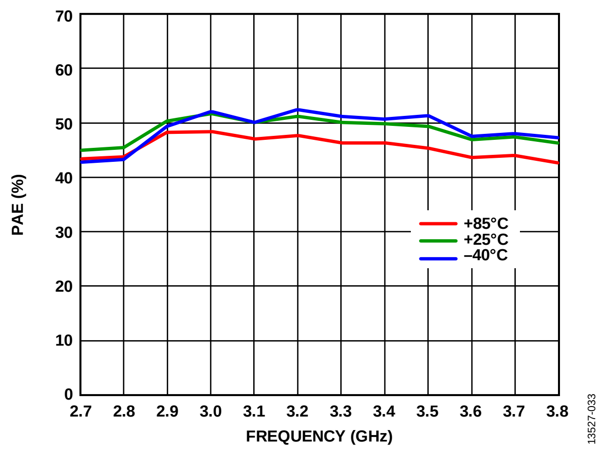

Figure 23. PAE vs. Frequency at Various Temperatures, PAE at P_{SAT} Defined as Output Power at P_{IN} = 31 dBm at 25°C, P_{IN} = 32 dBm at 85°C, and P_{IN} = 29 dBm at −40°C

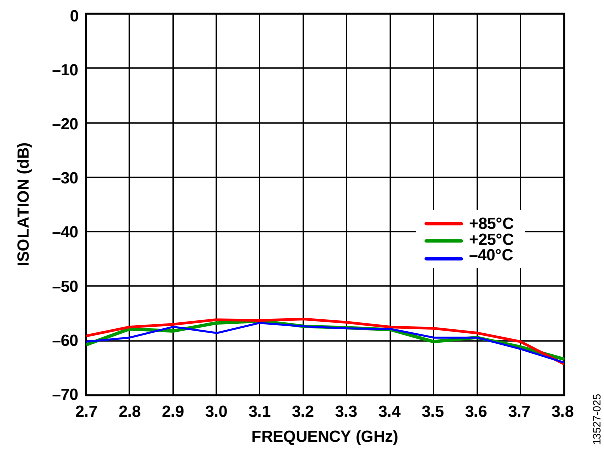

Figure 26. Reverse Isolation vs. Frequency at Various Temperatures, Measured CW

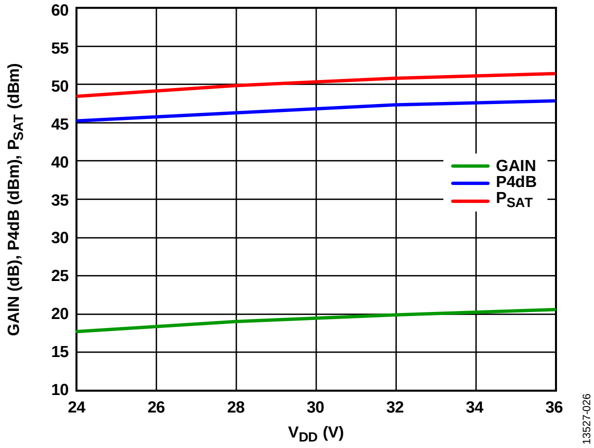

Figure 27. Gain and Power vs. Supply Voltage at 3.2 GHz, P_{SAT} Defined as Output Power at P_{IN} = 31 dBm at 25°C

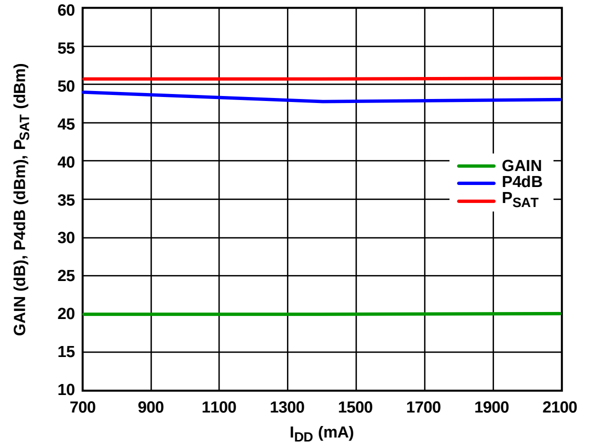

Figure 30. Gain and Power vs. Supply Current at 3.2 GHz, P_{SAT} Defined as Output Power at P_{IN} = 31 dBm at 25°C

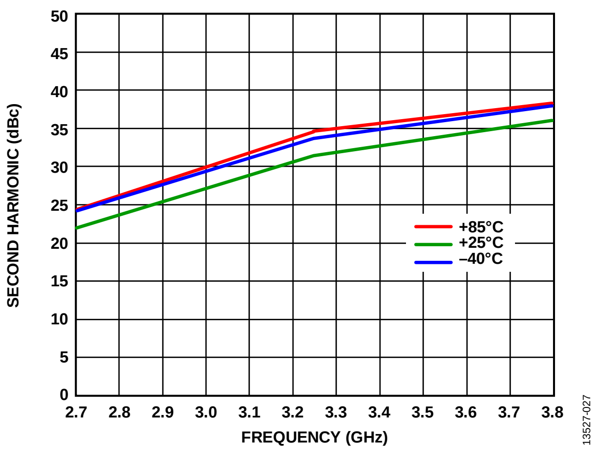

Figure 28. Second Harmonics vs. Frequency at Various Temperatures, P_{OUT} = 35 dBm

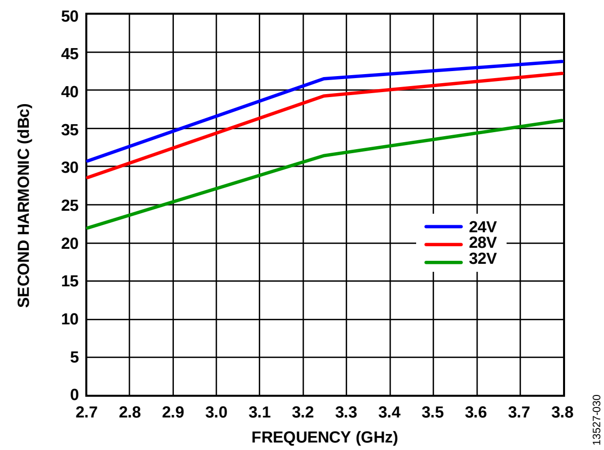

Figure 31. Second Harmonics vs. Frequency at Various Supply Voltages, P_{OUT} = 35 dBm

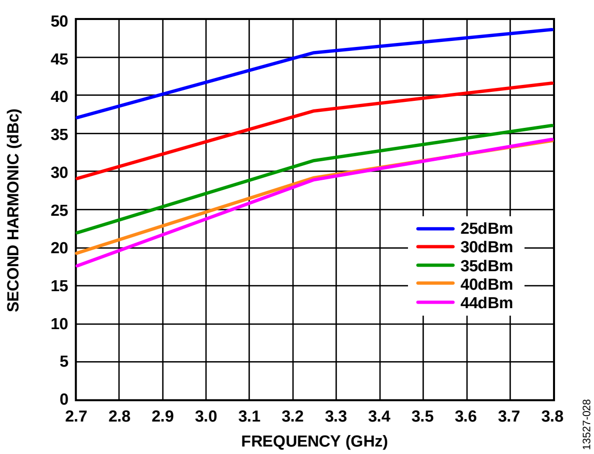

Figure 29. Second Harmonics vs. Frequency at Various P_{OUT} Levels

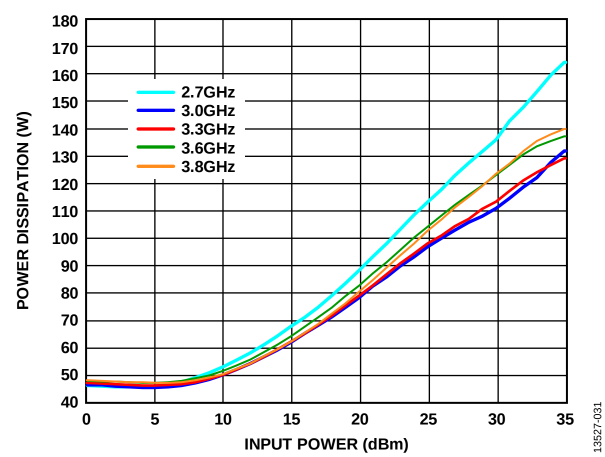

Figure 32. Power Dissipation at 85°C

APPLICATIONS INFORMATION

APPLICATION CIRCUIT

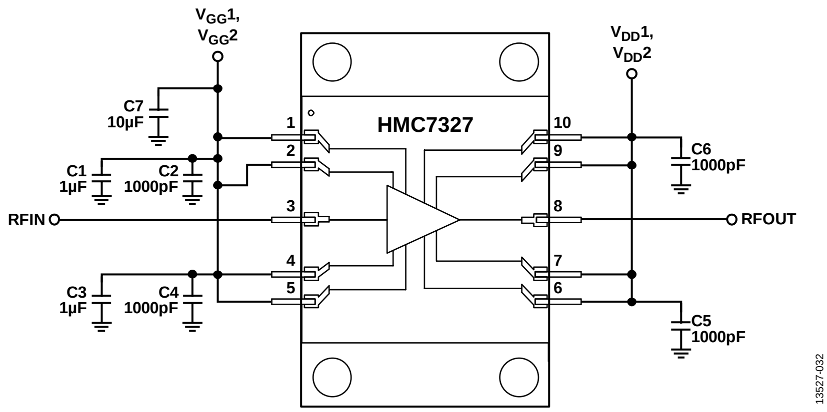

Figure 33. Typical Application Circuit

EVALUATION PRINTED CIRCUIT BOARD (PCB)

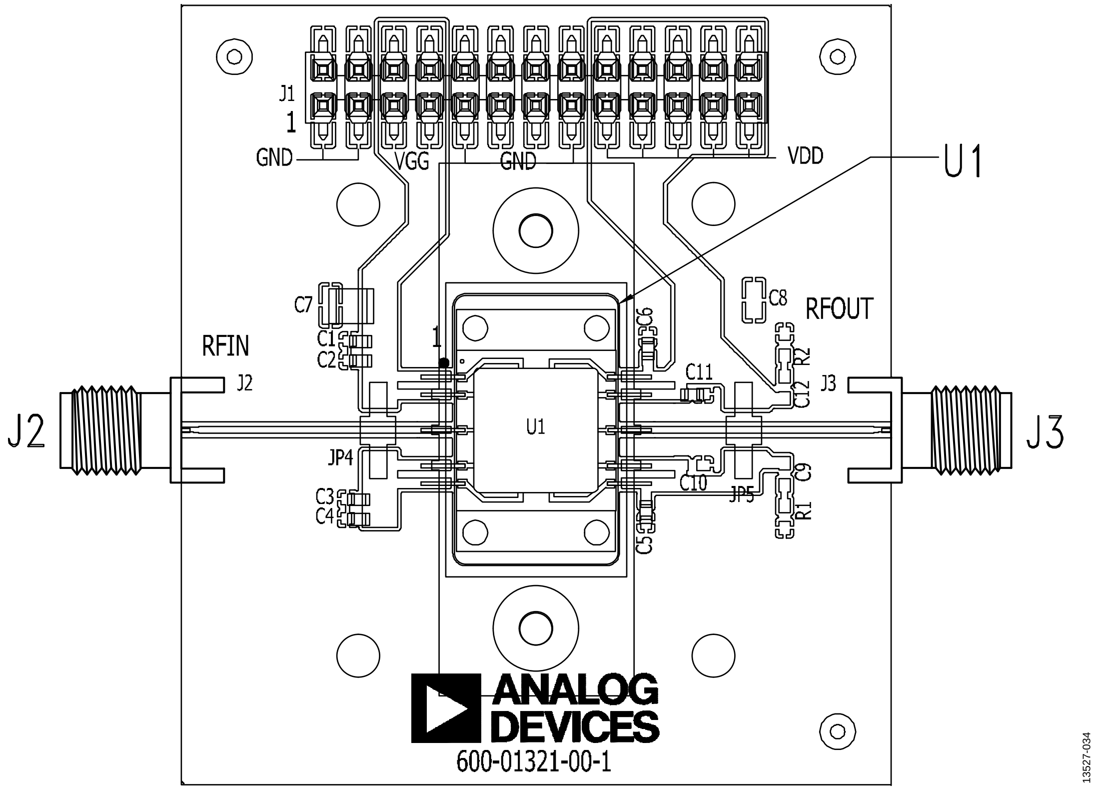

Figure 34. Evaluation PCB

BILL OF MATERIALS

Use RF circuit design techniques for the circuit board used in the application. Provide 50 Ω impedance for the signal lines and connect the package ground leads and exposed paddle directly to the ground plane, similar to that shown in Figure 34. Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board shown is available from Analog Devices, Inc., upon request.

Table 6. Bill of Materials for Evaluation PCB EVAL01-HMC7327F10A

Item	Description
J2, J3	SRI K connector.
J1	DC pins.
JP4, JP5	Preform jumpers.
C1, C3	1 µF capacitors, 0603 package.
C2, C4, C5, C6	1000 pF capacitors, 0603 package.
C7	10 µF capacitor, 1210 package.
U1	HMC7327F10A.
PCB	600-01312-00 evaluation PCB. Circuit board material: Rogers 4350 or Arlon 25FR.

OUTLINE DIMENSIONS

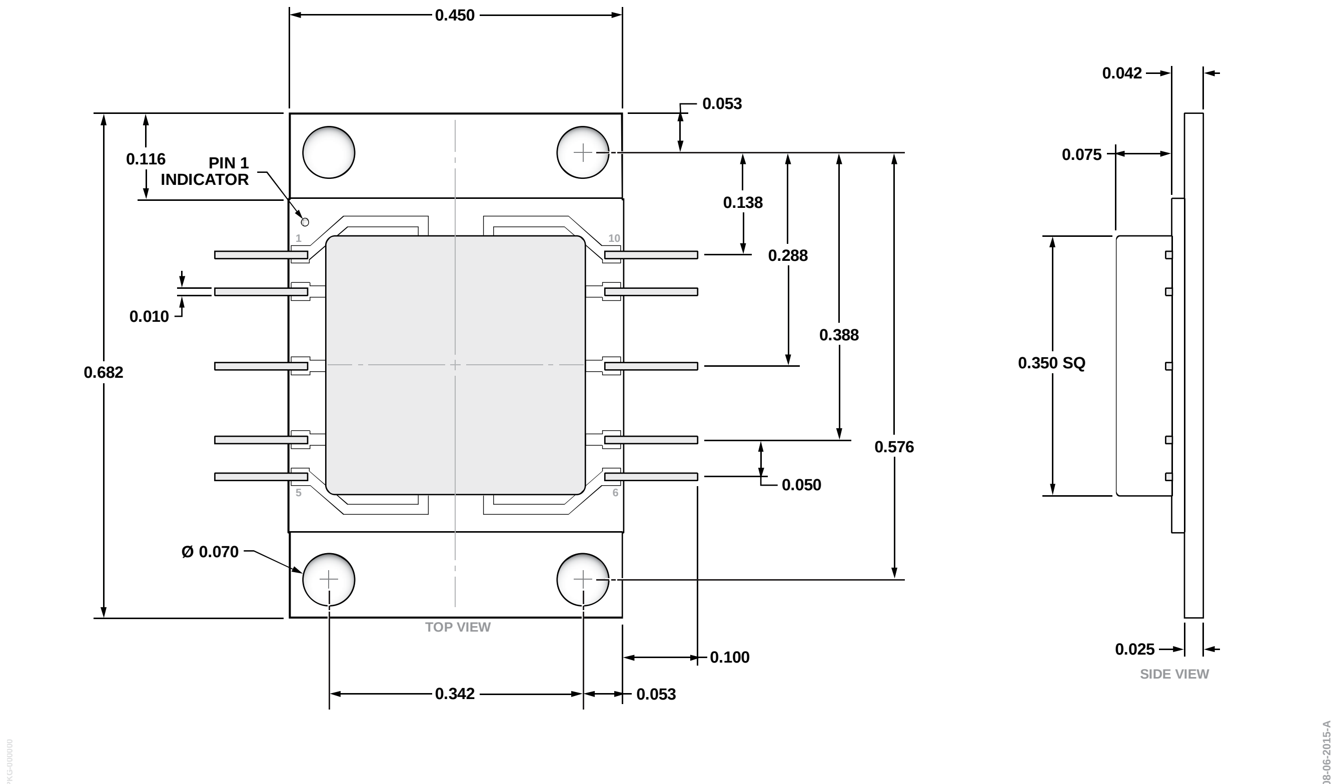

Figure 35. 10-Lead Module with Flange Heat Sink [CFMP]
(MF-10-1)
Dimensions shown in inches

ORDERING GUIDE

Model[1, 2]	Temperature	Description[3]	Package Option	Package Marking[4]
HMC7327F10A	−40°C to +85°C	10-Lead Module with Flange Heat Sink [CFMP]	MF-10-1	H7327 XXXX
EVAL01-HMC7327F10A		Evaluation fixture only		

[1] When ordering the evaluation fixture only, reference the model number, EVAL01-HMC7327F10A.
[2] The HMC7327F10A and the EVAL01-HMC7327F10A are not in production; for samples, contact an Analog Devices, Inc., sales representative.
[3] HMC7327F10A lead finish is NiAu and the package is Copper 15 Tungston 85.
[4] HMC7327F10A 4-digit lot number is represented by XXXX.

PR13527-0-9/15(PrA)