# VCO Rider Board with Loop Filter 

## DESCRIPTIOn

Demonstration circuit 2664A is a VCO Rider Board with Loop Filter that supports the popular $0.5^{\prime \prime} \times 0.5$ " VCO package footprint.

The DC2664A expedites evaluation of Phase-Locked Loop (PLL) devices requiring an external Voltage Controlled Oscillator (VCO). Without the DC2664A, each VCO and PLL combination requires a unique loop filter design, resulting in several PLL demo board modifications to evaluate each VCO. These board modifications are time consuming and often result in damage to either the PLL or the VCO.

The DC2664A integrates the VCO and loop filter allowing these unique designs to reside on multiple DC2664As. The DC2664A RFOUT and VTUNE SMA connections allow the user to quickly evaluate a PLL with multiple VCOs without risk of damage from multiple board modifications.

VCOs are notoriously sensitive to power supply noise and spurs. The DC2664A resolves the concern of locating a low noise and low spurious lab supply by powering the VCO with an onboard ultralow noise and ultrahigh PSRR LDO, the LT ${ }^{\circledR} 3042$. A second LT3042 LDO is available on the DC2664A to power an active loop filter. Both LDOs are powered from a single supply, simplifying the number of lab supplies required to evaluate a VCO and PLL combination.

The DC2664A was designed to mate directly with the LTC ${ }^{\circledR} 6955$ (DC2611A) and LTC6952 (DC2609A) demo boards. Examples are provided on the following pages.

## Design files for this circuit board are available.

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Figure 1. DC2664A Connections

## DEMO MANUAL DC2664A

## PUICK START PROCEDURE

## DC2664A Configuration

1. Select and install desired VCO (U4).
2. Set U1 output voltage (V_VCO) equal to the VCO's (U4) data sheet recommended supply voltage. This is accomplished by calculating the R9 value:

$$
\begin{equation*}
R 9=\frac{V_{-} V C O}{100 \mu \mathrm{~A}} \tag{1}
\end{equation*}
$$

Install R9 if different than factory default value. DC2664A arrives from the factory with $\mathrm{R} 9=49.9 \mathrm{k} \Omega$ (V_VCO = 5V). The LT3042 (U1) limits the V_VCO max supply voltage to 15 V .
3. Design and install loop filter. Analog Devices provides a loop filter design tool for all Analog Devices' PLLs. Download the appropriate loop filter design tool from the PLL product web page.
4. If an active loop filter is required, set U2's output voltage (V_OA) equal to the VCO's (U4) data sheet max

VTUNE voltage. This is accomplished by calculating the R11 value:

$$
\begin{equation*}
\mathrm{R} 11=\frac{\mathrm{V} \_0 \mathrm{~A}}{100 \mu \mathrm{~A}} \tag{2}
\end{equation*}
$$

Install R11 if different than factory default value.
DC2664A arrives from the factory with $\mathrm{R} 11=80.6 \mathrm{k} \Omega$ ( V _OA $=8 \mathrm{~V}$ ). The LT3042 (U2) limits the V_OA max supply voltage to 15 V . For V _OA $>15$, uninstall R5 and supply V_OA voltage directly to E4 turret.
5. Connect J 4 to a supply voltage and J 5 to GND.

$$
\begin{equation*}
\mathrm{V}_{\mathrm{J} 4}>\operatorname{Max}\left(\mathrm{V} \_\mathrm{VCO}, \mathrm{~V} \_\mathrm{OA}\right)+1 \mathrm{~V} \tag{3}
\end{equation*}
$$

$V_{\mathrm{J} 4}$ should not exceed 20V. The two green power supply LEDs (D1, D2) should illuminate after Step 5.
6. Connect J1 or J2 to PLL's Charge Pump (CP) output.
7. Connect J3 to PLL's VCO input.

## DEMO MANUAL DC2664A

## PUICK START PROCEDURE

STEP 5:


Figure 2. DC2664A Configuration

## DEMO MANUAL DC2664A

## EXAMPLE 1: LTC6952 (DC2664A, DC2609A)

Example 1 demonstrates the direct connect capability of the DC2664A and the DC2609A (LTC6952). The VCO and all loop filter components may reside on the DC2664A. However, to minimize the LTC6952 PFD
spurs, it is recommended to leave the C2 loop filter capacitor on the DC2609A demo board. Table 1 provides the recommended DC2609A modifications made to produce Figure 3.

Table 1. DC2609A Board Modifications

| UNINSTALL | INSTALL | CONNECTIONS |
| :--- | :--- | :--- |
| C81, R51 | C14 $=0.1 \mu \mathrm{~F}$ | DC2609A J31 connects to DC2664A J1 |
|  | R1 $=0 \Omega$ | DC2609A J28 connects to DC2664A J3 |
|  | C2 $=$ See loop filter design tool |  |



Figure 3. DC2664A and DC2609A Direct Connect

## DEMO MANUAL DC2664A

## EXAmPLE 2: LTC6952 AnD LTC6955 (DC2664A, DC2609A, DC2611A)

Example 2 demonstrates the direct connect capability of the DC2664A, the DC2611A (LTC6955), and the DC2609A (LTC6952). The VCO and all loop filter components can reside on the DC2664A. However, to minimize the LTC6952 PFD spurs, it is recommended to leave the C2 loop filter capacitor on the DC2609A demo board.

The DC2611A calibration path is used to pass the DC VTUNE voltage from the DC2609A to the DC2664A. To allow the VTUNE voltage to reach the DC2664A, replace the DC2611A's AC-coupling capacitors with $0 \Omega$ resistors. Table 2 and Table 3 provide the recommended DC2609A and DC2611A modifications made to produce Figure 3.

Table 2. DC2609A Board Modifications

| UNINSTALL | INSTALL | CONNECTIONS |
| :--- | :--- | :--- |
| C81, R18, R22, R51 | C14 $=$ C16 $=0.1 \mu \mathrm{~F}$ | DC2609A J31 connects to DC211A J23 |
|  | R20 $=160 \Omega$, R1 $=0 \Omega$ | DC2609A J28 connects to DC2611A J1 |
|  | C2 $=$ See loop filter design tool | DC2609A J29 connects to DC2611A J2 |

Table 3. DC2611A Board Modifications

| UNINSTALL (*) | INSTALL (*) | CONNECTIONS |
| :--- | :--- | :--- |
|  | C56 = C57 $=0 \Omega$ | DC2611A J24 connects to DC2664A J2 |
|  |  | DC2611A J25 connects to DC2664A J3 |

(*) Refer to DC2611A demo manual for correct input termination network for specific frequencies.


Figure 4. DC2664A, DC2609A and DC2611A Direct Connect

## DEMO MANUAL DC2664A

## TYPICAL DC2664A REQUIREMENTS AND CHAßACTERISTICS

Table 4.

| PARAMETER | INPUT/OUTPUT | PHYSICAL LOCATION | DETAILS |
| :---: | :---: | :---: | :---: |
| 6 V to 20V Power Supply | Input | J4 Banana Jack | Powers the onboard VCO and onboard active loop filter. To determine input voltage, refer to Equation 3. |
| GND | Output | J5 Banana Jack | Pair with J4 |
| V_VCO | Output/Input | E3 Turret | Output (Default): Connected to LT3042 (U1) output and VCO (U4) supply pin. Max 15 V . Input: For VCOs requiring >15V supplies, uninstall R4 and connect an external supply directly to E3. |
| V_OA | Output/Input | E4 Turret | Output (Default): Connected to LT3042 (U2) output and active loop filter's amplifier (U3) supply pin. Max 15 V . <br> Input: For VCO VTUNE pins requiring $>15 \mathrm{~V}$, uninstall R5 and connect an external supply directly to E4. |
| V_OA | Input | JP1 Header | Option to power on/off V_OA LDO (U2) |
| VTUNE_ALT | Input | J1 SMA Connector | Connect PLL Charge Pump output to either VTUNE or VTUNE_ALT. |
| VTUNE | Input | J2 SMA Connector | VTUNE_ALT is designed to direct connect to the DC2609A's (LTC6952 demo board) VTUNE SMA. Refer to Example 1. <br> VTUNE is designed to direct connect to the DC2611A's (LTC6955 demo board) CAL_IN SMA. Refer to Example 2. |
| OUT | Output | J3 SMA Connector | VCO's RF output |

ASSEMBLY OPTIONS

Table 5. DC2664A Options

## ASSEMBLY VERSION

DC2664A

## DEMO MANUAL DC2664A

## LAYOUT TOP LAYEß



## DEMO MANUAL DC2664A

## PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER | MANUFACTURER/PART NUMBER |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 2 | C1, C19 |  | AVX | 08055C104KAT2A |
| 2 | 0 | $\begin{aligned} & \text { C2, C2_ALT, C3, Cl1_A, } \\ & \text { Cl1_P, CP_A, CP_P } \end{aligned}$ | CAP., OPTION, 0603 |  |  |
| 3 | 2 | C4, C20 | CAP., 47 ${ }^{\text {F, TANT, 35V, 10\%, } 7361 ~}$ | AVX | TAJV476K035RNJ |
| 4 | 3 | C5, C12, C15 | CAP., $0.1 \mu \mathrm{~F}, \mathrm{X7R}, 10 \mathrm{~V}, 10 \%, 0402$ | MURATA | GRM155R71A104KA01D |
| 5 | 2 | C6, C16 | CAP., 10ヶF, TANT, 50V, 20\%, 7343 | AVX | TPSE106M050R0500 |
| 6 | 2 | C7, C17 | CAP., 4.7山F, X7R, 50V, 10\%, 1206 | AVX | 12065C475KAT2A |
| 7 | 2 | C8, C14 |  | MURATA | GRM155R71H104KE14D |
| 8 | 4 | C9, C11, C18, C21 | CAP., 4.7 F , X7R, 25V, 5\%, 1206 | KEMET | C1206C475J3RACTU |
| 9 | 1 | C10 | CAP., 22 $\mu \mathrm{F}$, TANT, 50V, 20\%, 7343 | KEMET | T521X226M050ATE075 |
| 10 | 1 | C13 | CAP., 47 ${ }^{\text {F, TANT, 20V, 20\%, } 7343}$ | AVX | TAJD476M020RNJ |
| 11 | 0 | Cl2_A, Cl2_P | CAP., OPTION, 1206 |  |  |
| 12 | 2 | D1, D2 | LED, GREEN, DIFFUSED, 0805 | BROADCOM LIMITED | HSMG-C170 |
| 13 | 1 | D3 | DIODE, ZENER, 5.6V, 200mW, SOD-323, AEC-Q101 | DIODES, INC. | BZT52C5V6S-7-F |
| 14 | 4 | E1-E4 | TEST POINT, TURRET, 0.064", MTG. HOLE | MILL-MAX | 2308-2-00-80-00-00-07-0 |
| 15 | 3 | J1-J3 | CONN., SMA, JACK, RCPT, END LAUNCH, STR, $50 \Omega$ | CINCH/ BEL | 142-0701-851 |
| 16 | 2 | J4, J5 | CONN., BANANA JACK, FEMALE, THT, NONINSULATED, SWAGE | KEYSTONE | 575-4 |
| 17 | 1 | JP1 | CONN., HDR., MALE, $1 \mathrm{~mm} \times 3.2 \mathrm{~mm}$, THT, STR | SULLINS CONNECTOR SOLUTIONS | NRPN031PAEN-RC |
| 18 | 4 | L1, L1_ALT, R4, R5 | RES., $0 \Omega, 1 / 8 \mathrm{~W}, 0805$ | VISHAY | CRCW08050000Z0EA |
| 19 | 2 | L2, L3 | IND.,330 @ @ 100MHz, FERRITE BEAD, 25\%, 0.8A, $0.21 \Omega, 0603$ | TAIYO YUDEN | FBMH1608HL331-T |
| 20 | 4 | MP1-MP4 | STANDOFF, NYLON, SNAP-ON, 0.50" | KEYSTONE | 8833 |
| 21 | 1 | PCB1 | PCB, DC2664A REV01 | MAO BANG | 600-DC2664A |
| 22 | 0 | R1_A, R2_A, RZ_A,RZ_P | RES., OPTION, 0603 |  |  |
| 23 | 2 | R1_P, R2_P | RES., 0 2 , 1/10W, 0603 | PANASONIC | ERJ3GEYOROOV |
| 24 | 1 | R2 | RES., 240 $2,1 \%, 1 / 16 \mathrm{~W}, 0402$ | VISHAY | CRCW0402240RFKED |
| 25 | 1 | R3 | RES., 2k,1\%, 1/16W, 0402 | VISHAY | CRCW04022K00FKED |
| 26 | 2 | R7, R8 | RES., 3.01k, 1\%, 1/8W, 0805 | VISHAY | CRCW08053K01FKEA |
| 27 | 1 | R9 | RES., 49.9k, 1\%, 1/10W, 0603 | VISHAY | CRCW060349K9FKEA |
| 28 | 1 | R10 | RES., 1k, 1\%, 1/16W, 0402 | VISHAY | CRCW04021K00FKED |
| 29 | 1 | R11 | RES., 80.6k, 1\%, 1/10W, 0603 | NIC | NRC06F8062TRF |
| 30 | 2 | U1, U2 | IC, PSRR RF LINEAR REGULATOR, DFN-10 (DD) | ANALOG DEVICES | LT3042EDD\#PBF |
| 31 | 1 | U3 | IC, DUAL/QUAD LOW NOISE OP AMPS, S0-8 | ANALOG DEVICES | LT1678IS8\#PBF |
| 32 | 0 | U4 | IC, VCO, 4340MHz to 4540MHz, OPTION | MINI-CIRCUITS | ROS-4540-119+ |
| 33 | 1 | XJP1 | CONN., SHUNT, FEMALE, 2 POS, 2mm | SAMTEC | 2SN-BK-G |

## SCHEMATIC DIAGRAM




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