

ADM809-5S/L

FEATURES

Specified over Temperature
Low Power Consumption (17 μ A)
Precision Voltage Monitor: 3 V, 5 V Options
Reset Assertion Down to 1 V V_{CC}
30 ms Min Power-On Reset
Logic Low $\overline{\text{RESET}}$ Output
Available in SOT-23 and SC70 Packages

APPLICATIONS

Microprocessor Systems
Computers
Controllers
Intelligent Instruments
Automotive Systems

GENERAL DESCRIPTION

The ADM809-5S/L supervisory circuit monitors the power supply voltage in microprocessor systems. It provides a reset output during power-up, power-down, and brownout conditions. On power-up, an internal timer holds reset asserted for 55 ms. This holds the microprocessor in a reset state until conditions have stabilized. The $\overline{\text{RESET}}$ output remains operational with V_{CC} as low as 1 V. The ADM809-5S/L provides an active low reset signal ($\overline{\text{RESET}}$).

The reset comparator features built-in glitch immunity, making it immune to fast transients on V_{CC} .

The ADM809-5S/L consumes only 17 μ A, making it suitable for low power portable equipment.

FUNCTIONAL BLOCK DIAGRAM

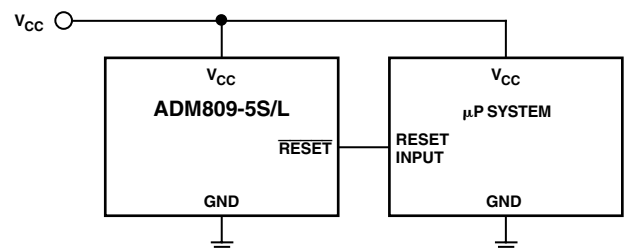
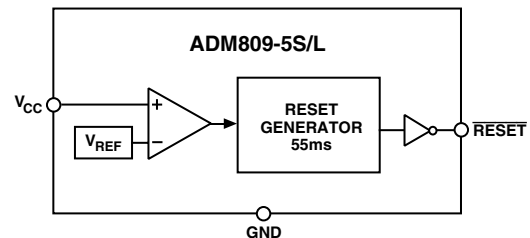


Figure 1. Typical Operating Circuit

REV. A

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ADM809-5S/L—SPECIFICATIONS (V_{CC} = Full Operating Range, T_A = T_{MIN} to T_{MAX}, V_{CC} typ = 5 V for L, 3.3 V for S Models, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
V _{CC} Operating Voltage Range	1.0	3.3	5.5	V	T _A = 0°C to 150°C with 100 kΩ Pull-Down on Output (Figure 3)
	1.2	3.3	5.5	V	T _A = -40°C to +150°C with 22 kΩ External Pull-Up on Output (Figure 6)
Supply Current		24	60	μA	V _{CC} < 5.5 V, ADM8_L, T _A = -40°C to +150°C
		17	50	μA	V _{CC} < 3.6 V, ADM8_S, T _A = -40°C to +150°C
RESET THRESHOLD					
Reset Voltage Threshold					
ADM809-5L	4.5		4.75	V	T _A = -40°C to +85°C
ADM809-5L	4.40		4.86	V	T _A = 85°C to 150°C
ADM809-5S	2.85		3.00	V	T _A = -40°C to +85°C
ADM809-5S	2.78		3.08	V	T _A = 85°C to 150°C
Reset Threshold Temperature Coefficient		30		ppm/°C	
V _{CC} to Reset Delay		20		μs	V _{CC} = V _{TH} to (V _{TH} - 100 mV)
Reset Active Timeout Period	30	55	80	ms	T _A = -40°C to +150°C
$\overline{\text{RESET}}$ Output Voltage Low			0.3	V	V _{CC} = V _{TH} min, I _{SINK} = 1.2 mA, ADM809-5S
			0.4	V	V _{CC} = V _{TH} min, I _{SINK} = 3.2 mA, ADM809-5L
			0.3	V	V _{CC} > 1.0 V, I _{SINK} = 50 μA, T _A = 0°C to 150°C
					V _{CC} > 1.2 V, I _{SINK} = 50 μA, T _A = -40°C to +150°C
$\overline{\text{RESET}}$ Output Voltage High	0.8 V _{CC}			V	V _{CC} > V _{TH} max, I _{SOURCE} = 500 μA
	V _{CC} - 1.5			V	V _{CC} > V _{TH} max, I _{SOURCE} = 800 μA
JUNCTION TEMPERATURE	-40		+150	°C	

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted.)

V _{CC}	-0.3 V to +6 V
RESET, $\overline{\text{RESET}}$	-0.3 V to V _{CC} + 0.5 V
Input Current	
V _{CC}	20 mA
Output Current	
RESET, $\overline{\text{RESET}}$	20 mA
Rate of Rise, V _{CC}	100 V/μs
θ _{JA} Thermal Impedance, SOT-23	270°C/W
θ _{JA} Thermal Impedance, SC70	146°C/W

Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Storage Temperature Range	-65°C to +150°C

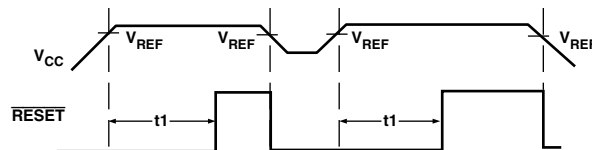
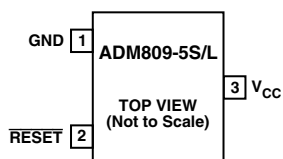
*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM809-5S/L features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION



$t_1 = \overline{\text{RESET}} \text{ TIME} = 55\text{ms TYP.}$
 $V_{\text{REF}} = \overline{\text{RESET}} \text{ VOLTAGE THRESHOLD}$

Figure 2. Power Fail $\overline{\text{RESET}}$ Timing

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	GND	0 V. Ground reference for all signals.
2	$\overline{\text{RESET}}$	Active Low Logic Output. $\overline{\text{RESET}}$ remains low while V_{CC} is below the reset threshold, and remains low for 55 ms (typ) after V_{CC} rises above the reset threshold.
3	V_{CC}	Supply Voltage Being Monitored.

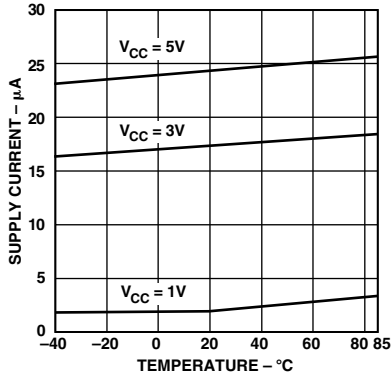
Table I. $\overline{\text{RESET}}$ Threshold Options

Model	$\overline{\text{RESET}}$ Threshold (V)
ADM809-5L	4.63
ADM809-5S	2.93

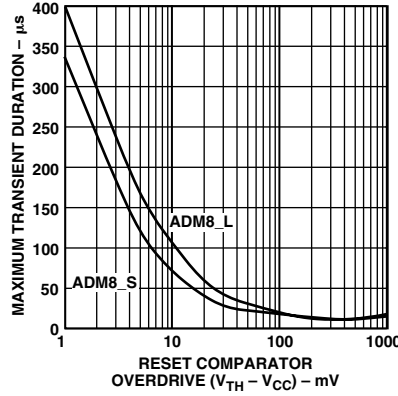
ORDERING GUIDE

Model	Reset Threshold (V)	Temperature Range	Branding Information	Quantity (K)	Package Type
ADM809-5LART-REEL	4.63	-40°C to +150°C	M9L	10	3-Lead SOT-23
ADM809-5LART-REEL-7	4.63	-40°C to +150°C	M9L	3	3-Lead SOT-23
ADM809-5LAKS-REEL	4.63	-40°C to +150°C	M9L	10	3-Lead SC70
ADM809-5LAKS-REEL-7	4.63	-40°C to +150°C	M9L	3	3-Lead SC70
ADM809-5SART-REEL	2.93	-40°C to +150°C	M9S	10	3-Lead SOT-23
ADM809-5SART-REEL-7	2.93	-40°C to +150°C	M9S	3	3-Lead SOT-23
ADM809-5SAKS-REEL	2.93	-40°C to +150°C	M9S	10	3-Lead SC70
ADM809-5SAKS-REEL-7	2.93	-40°C to +150°C	M9S	3	3-Lead SC70
ADM809-5SCHIPS	2.93	-40°C to +150°C	NA	1 Wafer	

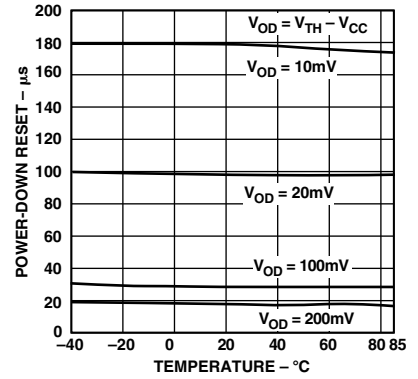
ADM809-5S/L – Typical Performance Characteristics



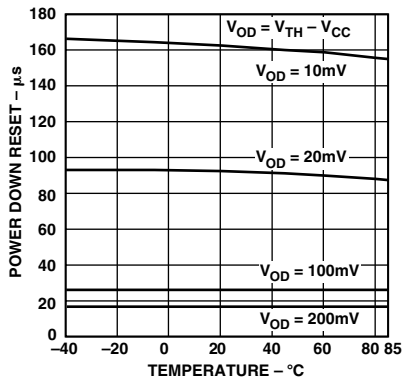
TPC 1. Supply Current vs. Temperature (No Load)



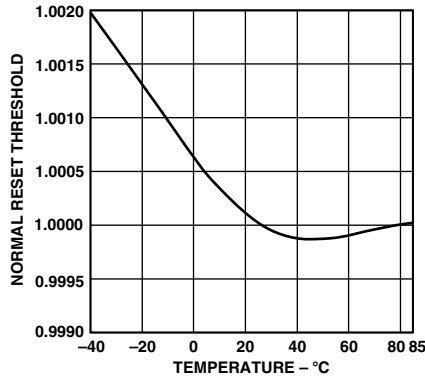
TPC 2. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive



TPC 3. Power-Down Reset Delay vs. Temperature ADM809-5L



TPC 4. Power-Down Reset Delay vs. Temperature ADM809-5S



TPC 5. Normalized Reset Voltage Threshold vs. Temperature

INTERFACING TO OTHER DEVICES' OUTPUT

The ADM809-5S/L is designed to integrate with as many devices as possible and therefore has an output dependent on V_{CC} . Because of this design approach, interfacing this device to other devices is simplified.

ENSURING A VALID RESET OUTPUT DOWN TO $V_{CC} = 0$ V

When V_{CC} falls below 0.8 V, ADM809-5S/L's \overline{RESET} no longer sinks current. A high impedance CMOS logic input connected to \overline{RESET} may, therefore, drift to undetermined logic levels. To eliminate this problem, a 100 k Ω resistor should be connected from \overline{RESET} to ground.

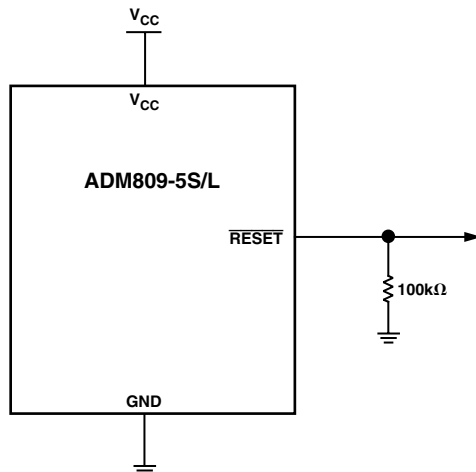


Figure 3. Ensuring a Valid \overline{RESET} Output Down to $V_{CC} = 0$ V

BENEFITS OF A VERY ACCURATE \overline{RESET} THRESHOLD

In other microprocessor supervisory circuits, tolerances in supply voltages lead to an overall increase in \overline{RESET} tolerance levels due to the deterioration of the microprocessor \overline{RESET} circuit's power supply. The possibility of a malfunction during a power failure is greatly reduced because the ADM809-5S/L series can operate effectively even when there are large degradations of the supply voltages. Another advantage of the ADM809-5S/L series is its very accurate internal voltage reference circuit. These benefits combine to produce an exceptionally reliable voltage monitor circuit.

INTERFACING TO MICROPROCESSORS WITH MULTIPLE INTERRUPTS

In a number of cases, it is necessary to interface many interrupts from different devices (i.e., thermal, attitude, and velocity sensors). The ADM809-5S/L can easily be integrated into existing interrupt-handling circuits (Figure 6) or used as a standalone device.

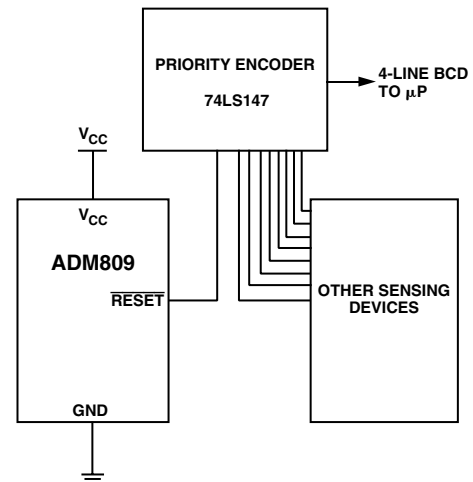


Figure 4. Interfacing to Microprocessors with Multiple Interrupts

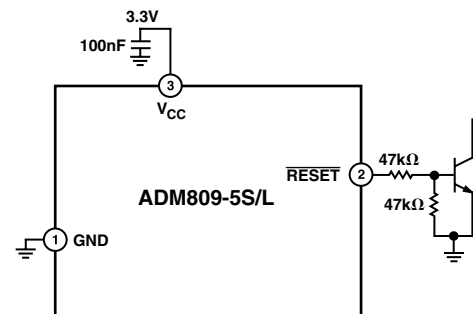


Figure 5. Alternative Application Circuit with Extra Decoupling

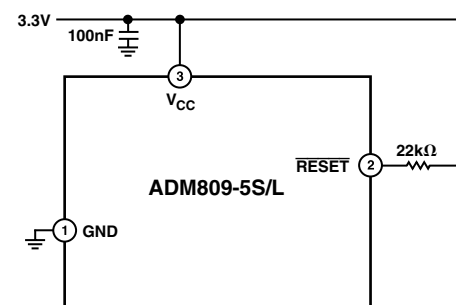
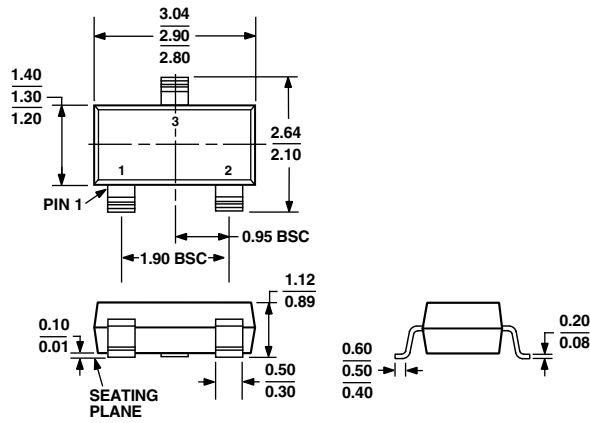


Figure 6. Additional Decoupling Can Be Achieved Using a 100 nF Capacitor between V_{CC} and Ground

OUTLINE DIMENSIONS

3-Lead Small Outline Transistor Package [SOT-23] (RT-3)

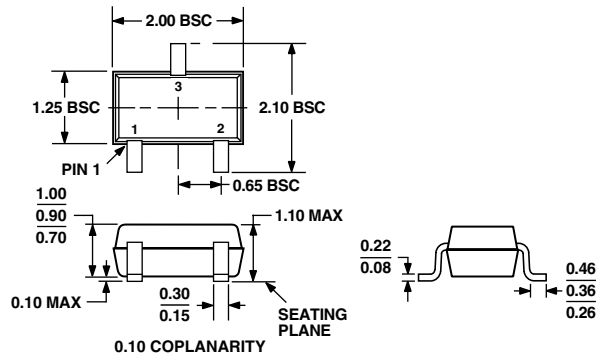
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS TO-236AB

3-Lead Thin Shrink Small Outline Transistor Package [SC70] (KS-3)

Dimensions shown in millimeters



Revision History

Location	Page
3/03—Data Sheet changed from REV. 0 to REV. A.	
Added SC70 Package	Universal
Changes to FEATURES	1
Changes to SPECIFICATIONS	2
Changes to ABSOLUTE MAXIMUM RATINGS	2
Changes to Table I	3
Changes to ORDERING GUIDE	3
Changes to TPC 2	4
Updated OUTLINE DIMENSIONS	6

