Multisupply Supervisor/Sequencer with ADC and Temperature Monitoring

Data Sheet

ADM1063-EP

FEATURES

- Complete supervisory and sequencing solution for up to 10 supplies
- Extended temperature range: −40°C to +105°C
- 10 supply fault detectors enable supervision of supplies to
  - <0.5% accuracy at all voltages at 25°C
  - <1.0% accuracy across all voltages and temperatures
- 5 selectable input attenuators allow supervision of supplies to
  - 14.4 V on VH
  - 6 V on VP1 to VP4 (VPx)
- 5 dual-function inputs, VX1 to VX5 (VXx)
  - High impedance input to supply fault detector with thresholds between 0.573 V and 1.375 V
  - General-purpose logic input
- 10 programmable driver outputs, PDO1 to PDO10 (PDOx)
  - Open-collector with external pull-up
  - Push/pull output, driven to VDDCAP or VPx
  - Open collector with weak pull-up to VDDCAP or VPx
  - Internally charge-pumped high drive for use with external N-FET (PDO1 to PDO6 only)
- Sequencing engine (SE) implements state machine control of PDOx outputs
  - State changes conditional on input events
  - Enables complex control of boards
  - Power-up and power-down sequence control
  - Fault event handling
  - Interrupt generation on warnings
  - Watchdog function can be integrated in SE
  - Program software control of sequencing through SMBus
- Complete voltage margining solution for 6 voltage rails
- 12-bit ADC for readback of all supervised voltages
- 1 internal and 2 external temperature sensors
- Reference input (REFIN) has 2 input options
  - Driven directly from 2.048 V (±0.25%) REFOUT pin
  - More accurate external reference for improved ADC performance
- Device powered by the highest of VPx, VH for improved redundancy
- User EEPROM: 256 bytes
- Industry-standard, 2-wire bus interface (SMBus)
- Guaranteed PDO low with VH, VPx = 1.2 V
- Available in 40-lead, 6 mm × 6 mm LFCSP package

For more information about the ADM1063 register map, refer to the AN-698 Application Note at www.analog.com.

FUNCTIONAL BLOCK DIAGRAM

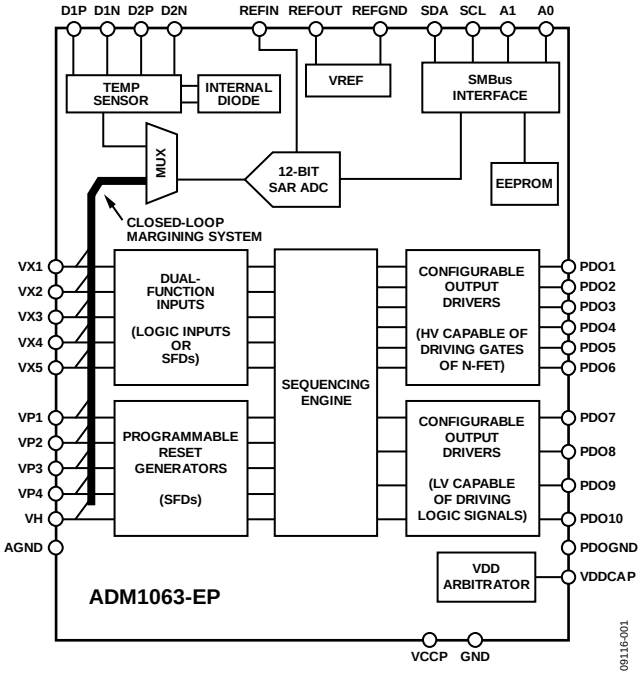

Figure 1.

APPLICATIONS

- Central office systems
- Servers/routers
- Multivoltage system line cards
- DSP/FPGA supply sequencing
- In-circuit testing of margined supplies

GENERAL DESCRIPTION

The ADM1063-EP is a configurable supervisory/sequencing device that offers a single-chip solution for supply monitoring and sequencing in multiple supply systems. In addition to these functions, the ADM1063-EP integrates a 12-bit ADC that can be used to accurately read back up to 12 separate voltages.

The device also provides up to 10 programmable inputs for monitoring undervoltage faults, overvoltage faults, or out-of-window faults on up to 10 supplies. In addition, 10 programmable outputs can be used as logic enables. Six of these programmable outputs can provide up to a 12 V output for driving the gate of an N-FET that can be placed in the path of a supply.

Rev. A
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

8/13—Rev. 0 to Rev. A

Changes to Serial Bus Timing Parameters; Table 1 6
Updated Outline Dimensions 12

5/10—Revision 0: Initial Version

Temperature measurement is possible with the ADM1063-EP. The device contains one internal temperature sensor and two pairs of differential inputs for remote thermal diodes. These are measured by the 12-bit ADC.

The logical core of the device is a sequencing engine. This state-machine-based construction provides up to 63 different states. This design enables very flexible sequencing of the outputs based on the condition of the inputs.

The device is controlled via configuration data that can be programmed into an EEPROM. The entire configuration can be programmed using an intuitive GUI-based software package provided by Analog Devices, Inc.

Full details about this enhanced product are available in the ADM1063 data sheet, which should be consulted in conjunction with this data sheet.

DETAILED BLOCK DIAGRAM

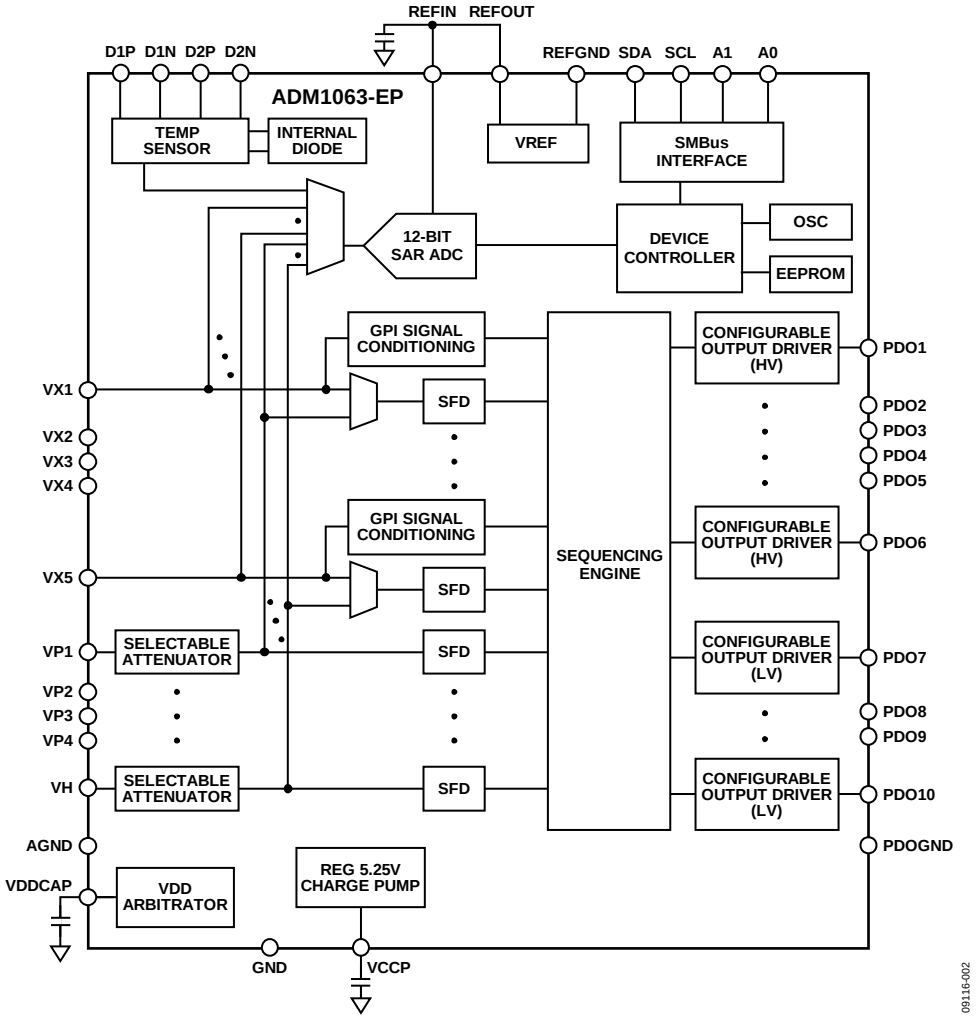

Figure 2.

SPECIFICATIONS

VH = 3.0 V to 14.4 V[1], VPx = 3.0 V to 6.0 V[1], T_A = −40°C to +105°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY ARBITRATION					
VH, VPx	3.0			V	Minimum supply required on one of VH, VPx
VPx			6.0	V	Maximum VDDCAP = 5.1 V, typical
VH			14.4	V	VDDCAP = 4.75 V
VDDCAP	2.7	4.75	5.4	V	Regulated LDO output
C_{VDDCAP}	10			µF	Minimum recommended decoupling capacitance
POWER SUPPLY					
Supply Current, I_{VH}, I_{VPx}		4.2	6	mA	VDDCAP = 4.75 V, PDO1 to PDO10 off, ADC off
Additional Currents					
All PDO FET Drivers On		1		mA	VDDCAP = 4.75 V, PDO1 to PDO6 loaded with 1 µA each, PDO7 to PDO10 off
Current Available from VDDCAP			2	mA	Maximum additional load that can be drawn from all PDO pull-ups to VDDCAP
ADC Supply Current		1		mA	Running round-robin loop
EEPROM Erase Current		10		mA	1 ms duration only, VDDCAP = 3 V
SUPPLY FAULT DETECTORS					
VH Pin					
Input Impedance		52		kΩ	
Input Attenuator Error		±0.05		%	Midrange and high range
Detection Ranges					
High Range	6		14.4	V	
Midrange	2.5		6	V	
VPx Pins					
Input Impedance		52		kΩ	
Input Attenuator Error		±0.05		%	Low range and midrange
Detection Ranges					
Midrange	2.5		6	V	
Low Range	1.25		3	V	
Ultralow Range	0.573		1.375	V	No input attenuation error
VXx Pins					
Input Impedance	1			MΩ	
Detection Range					
Ultralow Range	0.573		1.375	V	No input attenuation error
Absolute Accuracy			±1	%	VREF error + DAC nonlinearity + comparator offset error + input attenuation error
Threshold Resolution		8		Bits	
Digital Glitch Filter		0		µs	Minimum programmable filter length
		100		µs	Maximum programmable filter length

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG-TO-DIGITAL CONVERTER					
Signal Range	0		V_{REFIN}	V	The ADC can convert signals presented to the VH, VPx, and VXx pins; VPx and VH input signals are attenuated depending on the selected range; a signal at the pin corresponding to the selected range is from 0.573 V to 1.375 V at the ADC input
Input Reference Voltage on REFIN Pin, V_{REFIN}		2.048		V	
Resolution		12		Bits	
INL			±2.5	LSB	Endpoint corrected, V_{REFIN} = 2.048 V
Gain Error			±0.05	%	V_{REFIN} = 2.048 V
Conversion Time		0.44		ms	One conversion on one channel
		84		ms	All 12 channels selected, 16× averaging enabled
Offset Error			±2	LSB	V_{REFIN} = 2.048 V
Input Noise		0.25		LSB rms	Direct input (no attenuator)
TEMPERATURE SENSOR[2]					
Local Sensor Accuracy		±3		°C	VDDCAP = 4.75 V
Local Sensor Supply Voltage Coefficient		−1.7		°C/V	
Remote Sensor Accuracy		±3		°C	VDDCAP = 4.75 V
Remote Sensor Supply Voltage Coefficient		−3		°C	
Remote Sensor Current Source		200		µA	High level
		12		µA	Low level
Temperature for Code 0x800		0		°C	VDDCAP = 4.75 V
Temperature for Code 0xC00		128		°C	VDDCAP = 4.75 V
Temperature Resolution per Code		0.125		°C	
REFERENCE OUTPUT					
Reference Output Voltage	2.043	2.048	2.053	V	No load
Load Regulation		−0.25		mV	Sourcing current, $I_{DACxMAX}$ = −100 µA
		0.25		mV	Sinking current, $I_{DACxMAX}$ = 100 µA
Minimum Load Capacitance	1			µF	Capacitor required for decoupling, stability
PSRR		60		dB	DC
PROGRAMMABLE DRIVER OUTPUTS					
High Voltage (Charge Pump) Mode (PDO1 to PDO6)					
Output Impedance		500		kΩ	
V_{OH}	11	12.5	14	V	I_{OH} = 0 µA
	10.5	12	13.5	V	I_{OH} = 1 µA
I_{OUTAVG}		20		µA	2 V < V_{OH} < 7 V
Standard (Digital Output) Mode (PDO1 to PDO10)					
V_{OH}	2.4			V	V_{PU} (pull-up to VDDCAP or VPx) = 2.7 V, I_{OH} = 0.5 mA
			4.5	V	V_{PU} to VPx = 6.0 V, I_{OH} = 0 mA
	V_{PU} − 0.3			V	V_{PU} ≤ 2.7 V, I_{OH} = 0.5 mA
V_{OL}	0		0.50	V	I_{OL} = 20 mA
I_{OL}[3]			20	mA	Maximum sink current per PDOx pin
I_{SINK}[3]			60	mA	Maximum total sink for all PDOx pins
$R_{PULL-UP}$	19	20	29	kΩ	Internal pull-up
I_{SOURCE} (VPx)[3]			2	mA	Current load on any VPx pull-ups, that is, total source current available through any number of PDOx pull-up switches configured onto any one VPx pin
Three-State Output Leakage Current			10	µA	V_{PDO} = 14.4 V
Oscillator Frequency	90	100	110	kHz	All on-chip time delays derived from this clock

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUTS (VXx, A0, A1)					
Input High Voltage, V_{IH}	2.0			V	Maximum V_{IN} = 5.5 V
Input Low Voltage, V_{IL}			0.8	V	Maximum V_{IN} = 5.5 V
Input High Current, I_{IH}	−1			µA	V_{IN} = 5.5 V
Input Low Current, I_{IL}			1	µA	V_{IN} = 0 V
Input Capacitance		5		pF	
Programmable Pull-Down Current, $I_{PULL-DOWN}$		20		µA	VDDCAP = 4.75 V, T_A = 25°C if known logic state is required
SERIAL BUS DIGITAL INPUTS (SDA, SCL)					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}			0.8	V	
Output Low Voltage, V_{OL}[3]			0.4	V	I_{OUT} = −3.0 mA
SERIAL BUS TIMING[4]					
Clock Frequency, f_{SCLK}			400	kHz	
Bus Free Time, t_{BUF}	1.3			µs	
Start Setup Time, $t_{SU;STA}$	0.6			µs	
Stop Setup Time, $t_{SU;STO}$	0.6			µs	
Start Hold Time, $t_{HD;STA}$	0.6			µs	
SCL Low Time, t_{LOW}	1.3			µs	
SCL High Time, t_{HIGH}	0.6			µs	
SCL, SDA Rise Time, t_R			300	ns	
SCL, SDA Fall Time, t_F			300	ns	
Data Setup Time, $t_{SU;DAT}$	100			ns	
Data Hold Time, $t_{HD;DAT}$	5			ns	
Input Low Current, I_{IL}			1	µA	V_{IN} = 0 V
SEQUENCING ENGINE TIMING					
State Change Time		10		µs	

[1] At least one of the VH, VPx pins must be ≥3.0 V to maintain the device supply on VDDCAP.
[2] All temperature sensor measurements are taken with round-robin loop enabled and at least one other voltage input being measured.
[3] Specification is not production tested but is supported by characterization data at initial product release.
[4] Timing specifications are guaranteed by design and supported by characterization data.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltage on VH Pin	16 V
Voltage on VPx Pins	7 V
Voltage on VXx Pins	−0.3 V to +6.5 V
Voltage on A0, A1 Pins	−0.3 V to +7 V
Voltage on REFIN, REFOUT Pins	5 V
Voltage on VDDCAP, VCCP Pins	6.5 V
Voltage on PDOx Pins	16 V
Voltage on SDA, SCL Pins	7 V
Voltage on GND, AGND, PDOGND, REFGND Pins	−0.3 V to +0.3 V
Voltage on DxN, DxP Pins	−0.3 V to +5 V
Input Current at Any Pin	±5 mA
Package Input Current	±20 mA
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering Vapor Phase, 60 sec)	215°C
ESD Rating, All Pins	2000 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
40-Lead LFCSP	26.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

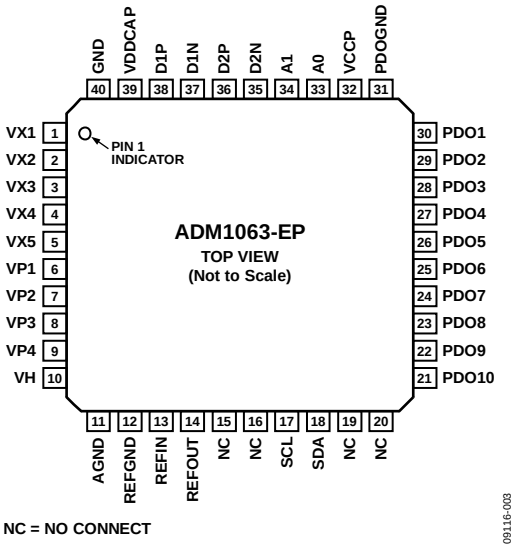

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic
1 to 5	VX1 to VX5 (VXx)
6 to 9	VP1 to VP4 (VPx)
10	VH
11	AGND (In a typical application, all ground pins are connected together.)
12	REFGND (In a typical application, all ground pins are connected together.)
13	REFIN
14	REFOUT
15, 16, 19, 20	NC
17	SCL
18	SDA
21 to 30	PDO10 to PDO1
31	PDOGND (In a typical application, all ground pins are connected together.)
32	VCCP
33	A0
34	A1
35	D2N
36	D2P
37	D1N
38	D1P
39	VDDCAP
40	GND (In a typical application, all ground pins are connected together.)
EPAD	Exposed pad. This pad is a no connect (NC). If possible, this pad should be soldered to the board for improved mechanical stability.

TYPICAL PERFORMANCE CHARACTERISTICS

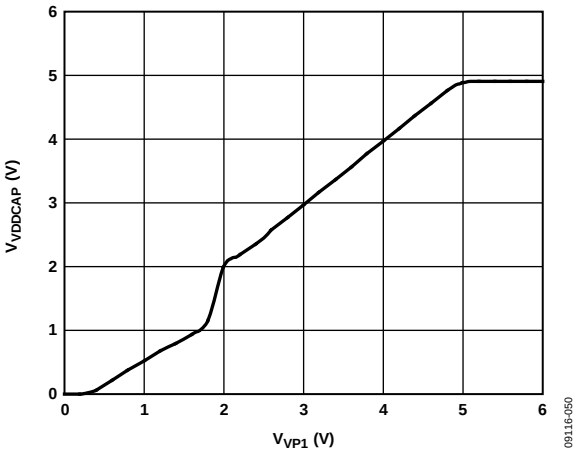

Figure 4. V_{VDDCAP} vs. V_{VP1}

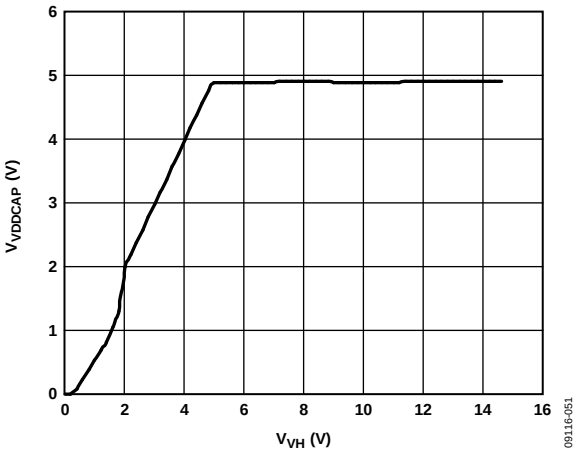

Figure 5. V_{VDDCAP} vs. V_{VH}

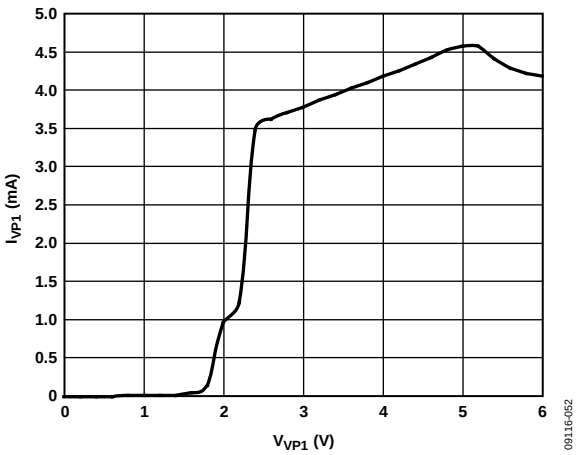

Figure 6. I_{VP1} vs. V_{VP1} (VP1 as Supply)

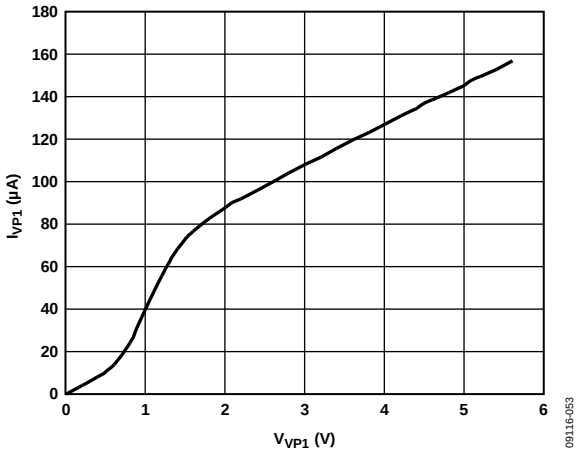

Figure 7. I_{VP1} vs. V_{VP1} (VP1 Not as Supply)

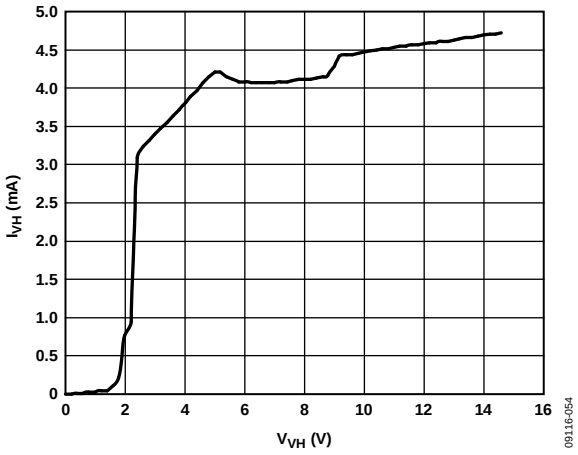

Figure 8. I_{VH} vs. V_{VH} (VH as Supply)

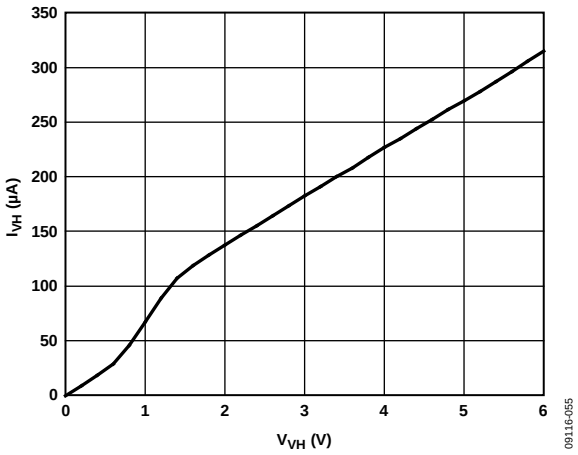

Figure 9. I_{VH} vs. V_{VH} (VH Not as Supply)

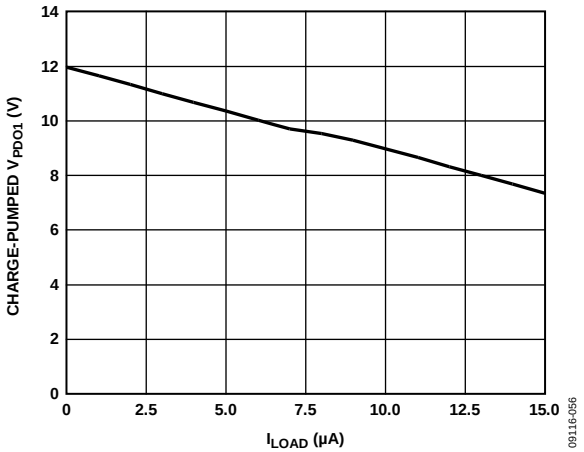

Figure 10. Charge-Pumped V_{PDO1} (FET Drive Mode) vs. I_{LOAD}

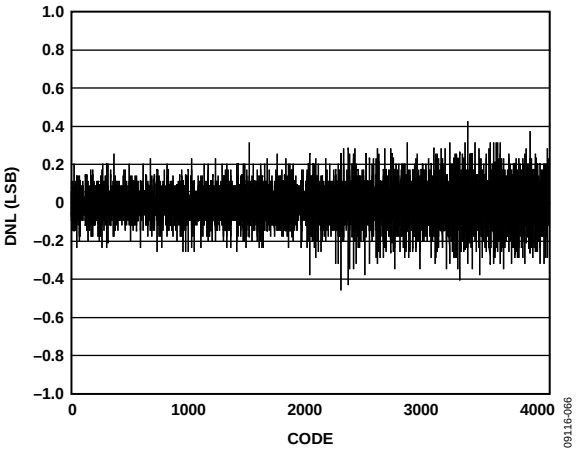

Figure 13. DNL for ADC

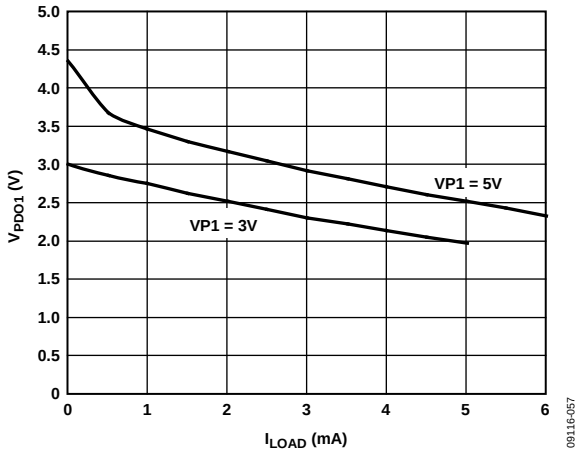

Figure 11. V_{PDO1} (Strong Pull-Up to VPx) vs. I_{LOAD}

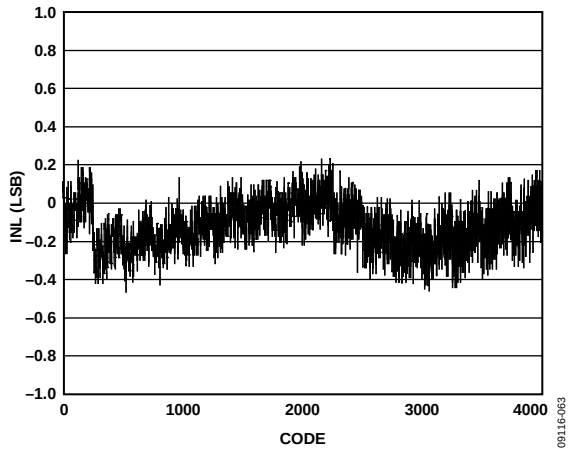

Figure 14. INL for ADC

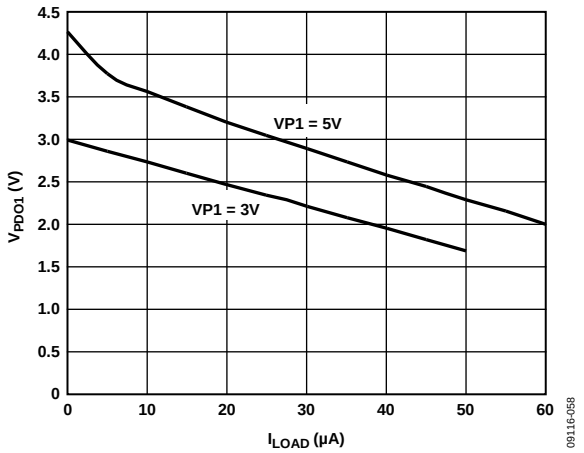

Figure 12. V_{PDO1} (Weak Pull-Up to VPx) vs. I_{LOAD}

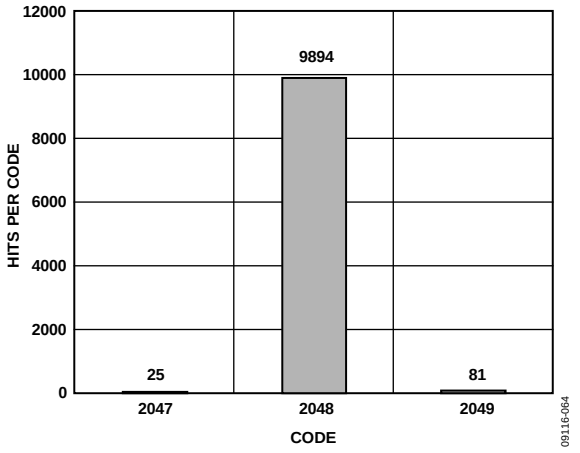

Figure 15. ADC Noise, Midcode Input, 10,000 Reads

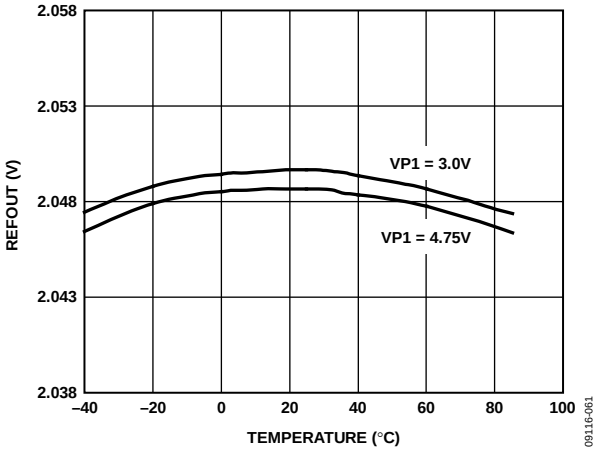

Figure 16. REFOUT vs. Temperature

OUTLINE DIMENSIONS

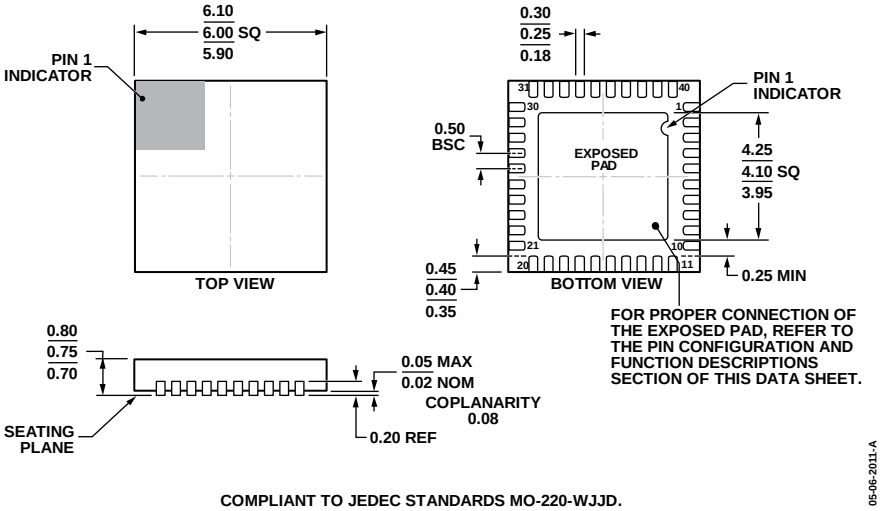

Figure 17. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Thin Quad
(CP-40-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM1063BCPZ-EP-RL7	−40°C to +105°C	40-Lead LFCSP_WQ	CP-40-9

[1] Z = RoHS Compliant Part.