

High Speed Multifrequency PLL Clock Buffer

Features

- 12–100 MHz (CY7B9930V), or 24–200 MHz (CY7B9940V) input/output operation
- Matched pair output skew < 200 ps
- Zero input-to-output delay
- 10 LVTTTL 50% duty-cycle outputs capable of driving 50Ω terminated lines
- Commercial temperature range with eight outputs at 200 MHz
- Industrial temperature range with eight outputs at 200 MHz
- 3.3V LVTTTL/LV differential (LVPECL), fault-tolerant and hot insertable reference inputs
- Multiply ratios of (1–6, 8, 10, 12)
- Operation up to 12x input frequency
- Individual output bank disable for aggressive power management and EMI reduction
- Output high impedance option for testing purposes
- Fully integrated PLL with lock indicator
- Low cycle-to-cycle jitter (<100 ps peak-peak)

- Single 3.3V ± 10% supply

- 44-pin TQFP package

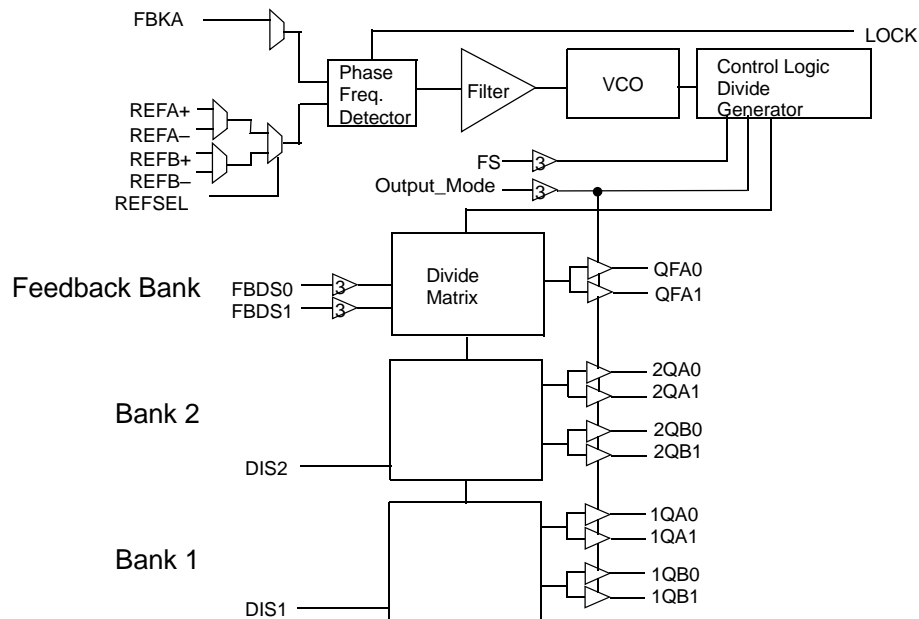
Functional Description

The CY7B9930V and CY7B9940V High-Speed Multifrequency PLL Clock Buffers offer user-selectable control over system clock functions. This multiple output clock driver provides the system integrator with functions necessary to optimize the timing of high performance computer or communication systems.

Ten configurable outputs can each drive terminated transmission lines with impedances as low as 50Ω while delivering minimal and specified output skews at LVTTTL levels. The outputs are arranged in three banks. The FB feedback bank consists of two outputs, which allows divide-by functionality from 1 to 12. Any one of these ten outputs can be connected to the feedback input as well as driving other inputs.

Selectable reference input is a fault tolerance feature that allows smooth change over to secondary clock source, when the primary clock source is not in operation. The reference inputs are configurable to accommodate both LVTTTL or differential (LVPECL) inputs. The completely integrated PLL reduces jitter and simplifies board layout.

Block Diagram



Block Diagram Description

Phase Frequency Detector and Filter

These two blocks accept signals from the REF inputs (REFA+, REFA-, REFB+ or REFB-) and the FB input (FBKA). Correction information is then generated to control the frequency of the Voltage Controlled Oscillator (VCO). These two blocks, along with the VCO, form a Phase-Locked Loop (PLL) that tracks the incoming REF signal.

The RoboClockII™ Junior has a flexible REF input scheme. These inputs allow the use of either differential LVPECL or single ended LVTTTL inputs. To configure as single ended LVTTTL inputs, leave the complementary pin to 1.5V), then use the other input pin as an LVTTTL input. The REF inputs are also tolerant to hot insertion.

The REF inputs can be changed dynamically. When changing from one reference input to the other reference input of the same frequency, the PLL is optimized to ensure that the clock outputs period is not less than the calculated system budget ($t_{MIN} = t_{REF}$ (nominal reference clock period) - t_{CCJ} (cycle-to-cycle jitter) - t_{PDEV} (max. period deviation)) while reacquiring lock.

VCO, Control Logic, and Divide Generator

The VCO accepts analog control inputs from the PLL filter block. The FS control pin setting determines the nominal operational frequency range of the divide by one output (f_{NOM}) of the device. f_{NOM} is directly related to the VCO frequency. There are two versions of the RoboClockII Junior, a low speed device (CY7B9930V) where f_{NOM} ranges from 12 MHz to 100 MHz, and a high speed device (CY7B9940V), which ranges from 24 MHz to 200 MHz. The FS setting for each device is shown in Table 1. The f_{NOM} frequency is seen on “divide-by-one” outputs.

Table 1. Frequency Range Select

| FS ^[1] | CY7B9930V | | CY7B9940V | |
|-------------------|------------------------|------|------------------------|--------------------|
| | f _{NOM} (MHz) | | f _{NOM} (MHz) | |
| | Min. | Max. | Min. | Max. |
| LOW | 12 | 26 | 24 | 52 |
| MID | 24 | 52 | 48 | 100 |
| HIGH | 48 | 100 | 96 | 200 ^[2] |

Notes

- The level to be set on FS is determined by the “nominal” operating frequency (f_{NOM}) of the VCO. f_{NOM} always appears on an output when the output is operating in the undivided mode. The REF and FB are at f_{NOM} when the output connected to FB is undivided.
- The maximum output frequency is 200 MHz.

Divide Matrix

The Divide Matrix is comprised of three independent banks: two banks of clock outputs and one bank for feedback. Each clock output bank has two pairs of low-skew, high fanout output buffers ([1:2]Q[A:B][0:1]), and an output disable (DIS[1:2]).

The feedback bank has one pair of low-skew, high fanout output buffers (QFA[0:1]). One of these outputs may connect to the selected feedback input (FBKA+). This feedback bank also has two divider function selects FBDS[0:1].

The divide capabilities for each bank are shown in Table 2.

Table 2. Output Divider Function

| Function Selects | | Output Divider Function | | |
|------------------|-------|-------------------------|--------|---------------|
| FBDS1 | FBDS0 | Bank 1 | Bank 2 | Feedback Bank |
| LOW | LOW | /1 | /1 | /1 |
| LOW | MID | /1 | /1 | /2 |
| LOW | HIGH | /1 | /1 | /3 |
| MID | LOW | /1 | /1 | /4 |
| MID | MID | /1 | /1 | /5 |
| MID | HIGH | /1 | /1 | /6 |
| HIGH | LOW | /1 | /1 | /8 |
| HIGH | MID | /1 | /1 | /10 |
| HIGH | HIGH | /1 | /1 | /12 |

Output Disable Description

The outputs of Bank 1 and Bank 2 can be independently put into a HOLD OFF or high impedance state. The combination of the Output_Mode and DIS[1:2] inputs determines the clock outputs' state for each bank. When the DIS[1:2] is LOW, the outputs of the corresponding bank are enabled. When the DIS[1:2] is HIGH, the outputs for that bank are disabled to a high impedance (HI-Z) or HOLD OFF state depending on the Output_Mode input. Table 3 defines the disabled output functions.

The HOLD OFF state is designed as a power saving feature. An output bank is disabled to the HOLD OFF state in a maximum of six output clock cycles from the time when the disable input (DIS[1:2]) is HIGH. When disabled to the HOLD OFF state, outputs are driven to a logic LOW state on its falling edge. This ensures the output clocks are stopped without glitch. When a bank of outputs is disabled to HI-Z state, the respective bank of outputs go HI-Z immediately.

Table 3. DIS[1:2] Pin Functionality

| OUTPUT_MODE | DIS[1:2]/FBDIS | Output Mode |
|-------------|----------------|--------------|
| HIGH/LOW | LOW | ENABLED |
| HIGH | HIGH | HI-Z |
| LOW | HIGH | HOLD-OFF |
| MID | X | FACTORY TEST |

Lock Detect Output Description

The LOCK detect output indicates the lock condition of the integrated PLL. Lock detection is accomplished by comparing the phase difference between the reference and feedback inputs. Phase error is declared when the phase difference between the two inputs is greater than the specified device propagation delay limit (t_{PD}).

When in the locked state, after four or more consecutive feedback clock cycles with phase errors, the LOCK output is forced LOW to indicate out-of-lock state.

When in the out-of-lock state, 32 consecutive phase errorless feedback clock cycles are required to allow the LOCK output to indicate lock condition (LOCK = HIGH).

If the feedback clock is removed after LOCK has gone HIGH, a Watchdog circuit is implemented to indicate the out-of-lock condition after a timeout period by deasserting LOCK LOW. This timeout period is based upon a divided down reference clock.

This assumes that there is activity on the selected REF input. If there is no activity on the selected REF input then the LOCK detect pin may not accurately reflect the state of the internal PLL.

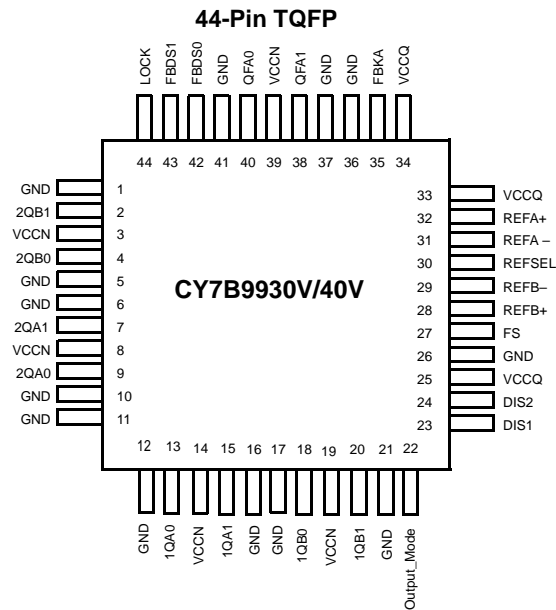
Factory Test Mode Description

The device enters factory test mode when the OUTPUT_MODE is driven to MID. In factory test mode, the device operates with its internal PLL disconnected; the input level supplied to the reference input is used in place of the PLL output. In TEST mode the selected FB input must be tied LOW. All functions of the device remain operational in factory test mode except the internal PLL and output bank disables. The OUTPUT_MODE input is designed as a static input. Dynamically toggling this input from LOW to HIGH may temporarily cause the device to go into factory test mode (when passing through the MID state).

Factory Test Reset

When in factory test mode (OUTPUT_MODE = MID), the device is reset to a deterministic state by driving the DIS2 input HIGH. When the DIS2 input is driven HIGH in factory test mode, all clock outputs go to HI-Z; after the selected reference clock pin has five positive transitions, all the internal finite state machines (FSM) are set to a deterministic state. The deterministic state of the state machines depends on the configurations of the divide selects and frequency select input. All clock outputs stay in high impedance mode and all FSMs stay in the deterministic state until DIS2 is deasserted. When DIS2 is deasserted (with OUTPUT_MODE still at MID), the device reenters factory test mode.

Pin Definitions



| Name | I/O | Type | Description |
|----------------------------|--------|-------------------|--|
| FBKA | Input | LVTTTL | Feedback Input. |
| REFA+, REFA-, REFB+, REFB- | Input | LVTTTL/ LVDIFF | Reference Inputs: These inputs operate as either differential PECL or single ended TTL reference inputs to the PLL. When operating as a single ended LVTTTL input, leave the complementary input must be left open. |
| REFSEL | Input | LVTTTL | Reference Select Input: The REFSEL input controls reference input configuration. When LOW, it uses the REFA pair as the reference input. When HIGH, it uses the REFB pair as the reference input. This input has an internal pull down. |
| FS ^[3] | Input | 3 Level Input | Frequency Select: Set this input according to the nominal frequency (f_{NOM}). See Table 1 . |
| FBDS[0:1] ^[3] | Input | 3 Level Input | Feedback Divider Function Select. These inputs determine the function of the QFA0 and QFA1 outputs. See Table 2 . |
| DIS[1:2] | Input | LVTTTL | Output Disable: Each input controls the state of the respective output bank. When HIGH, the output bank is disabled to the “HOLD OFF” or “HI-Z” state; the disable state is determined by OUTPUT_MODE. When LOW, the [1:4]Q[A:B][0:1] is enabled. See Table 3 . These inputs each have an internal pull down. |
| LOCK | Output | LVTTTL | PLL Lock Indicator: When HIGH, this output indicates that the internal PLL is locked to the reference signal. When LOW, the PLL is attempting to acquire lock. |
| Output_Mode ^[3] | Input | 3 Level Input | Output Mode: This pin determines the clock outputs’ disable state. When this input is HIGH, the clock outputs disable to high impedance (HI-Z). When this input is LOW, the clock outputs disables to “HOLD OFF” mode. When in MID, the device enters factory test mode. |
| QFA[0:1] | Output | LVTTTL | Clock Feedback Output: This pair of clock outputs connects to the FB input. These outputs have numerous divide options. The function is determined by the setting of the FBDS[0:1] pins. |
| [1:2]Q[A:B][0:1] | Output | LVTTTL | Clock Output. |
| VCCN | | PWR | Output Buffer Power: Power supply for each output pair. |
| VCCQ | | PWR | Internal Power: Power supply for the internal circuitry. |
| GND | | PWR | Device Ground. |

Note

3. For all tri-state inputs, HIGH indicates a connection to V_{CC} , LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.

Absolute Maximum Conditions

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -40°C to +125°C
 Ambient Temperature with power applied -40°C to +125°C
 Supply voltage to ground potential -0.5V to +4.6V
 DC input voltage -0.3V to $V_{CC}+0.5V$
 Output current into outputs (LOW) 40 mA

Static discharge voltage..... >2000V
 MIL-STD-883, Method 3015)

Latch up current..... >±200 mA

Operating Range

| Range | Ambient Temperature | V_{CC} |
|------------|---------------------|-----------|
| Commercial | 0°C to +70°C | 3.3V ±10% |
| Industrial | -40°C to +85°C | 3.3V ±10% |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Max. | Unit | |
|--|---------------------------------------|----------------------------|---|---------------------|---------------------|----|
| LVTTTL Compatible Output Pins (QFA[0:1], [1:4]Q[A:B][0:1], LOCK) | | | | | | |
| V_{OH} | LVTTTL HIGH voltage | QFA[0:1], [1:2]Q[A:B][0:1] | $V_{CC} = \text{Min.}, I_{OH} = -30 \text{ mA}$ | 2.4 | - | V |
| | | LOCK | $I_{OH} = -2 \text{ mA}, V_{CC} = \text{Min.}$ | 2.4 | - | V |
| V_{OL} | LVTTTL LOW voltage | QFA[0:1], [1:2]Q[A:B][0:1] | $V_{CC} = \text{Min.}, I_{OL} = 30 \text{ mA}$ | - | 0.5 | V |
| | | LOCK | $I_{OL} = 2 \text{ mA}, V_{CC} = \text{Min.}$ | - | 0.5 | V |
| I_{OZ} | High impedance state leakage current | | -100 | 100 | µA | |
| LVTTTL Compatible Input Pins (FBKA, REFA±, REFB±, REFSEL, DIS[1:2]) | | | | | | |
| V_{IH} | LVTTTL Input HIGH | FBKA+, REF[A:B]± | $\text{Min.} \leq V_{CC} \leq \text{Max.}$ | 2.0 | $V_{CC}+0.3$ | V |
| | | REFSEL, DIS[1:2] | | 2.0 | $V_{CC}+0.3$ | V |
| V_{IL} | LVTTTL Input LOW | FBKA+, REF[A:B]± | $\text{Min.} \leq V_{CC} \leq \text{Max.}$ | -0.3 | 0.8 | V |
| | | REFSEL, DIS[1:2] | | -0.3 | 0.8 | V |
| I_I | LVTTTL $V_{IN} > V_{CC}$ | FBKA+, REF[A:B]± | $V_{CC} = \text{GND}, V_{IN} = 3.63V$ | - | 100 | µA |
| I_{IH} | LVTTTL Input HIGH Current | FBKA+, REF[A:B]± | $V_{CC} = \text{Max.}, V_{IN} = V_{CC}$ | - | 500 | µA |
| | | REFSEL, DIS[1:2] | $V_{IN} = V_{CC}$ | - | 500 | µA |
| I_{IL} | LVTTTL Input LOW Current | FBKA+, REF[A:B]± | $V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ | -500 | - | µA |
| | | REFSEL, DIS[1:2] | | -500 | - | µA |
| 3-Level Input Pins (FBDS[0:1], FS, Output_Mode) | | | | | | |
| V_{IHH} | Three level input HIGH ^[4] | | $\text{Min.} \leq V_{CC} \leq \text{Max.}$ | $0.87 \cdot V_{CC}$ | - | V |
| V_{IMM} | Three level input MID ^[4] | | $\text{Min.} \leq V_{CC} \leq \text{Max.}$ | $0.47 \cdot V_{CC}$ | $0.53 \cdot V_{CC}$ | V |
| V_{ILL} | Three level input LOW ^[4] | | $\text{Min.} \leq V_{CC} \leq \text{Max.}$ | | $0.13 \cdot V_{CC}$ | V |
| I_{IHH} | Three level input HIGH current | Three level input pins | $V_{IN} = V_{CC}$ | - | 200 | µA |
| I_{IMM} | Three level input MID current | Three level input pins | $V_{IN} = V_{CC}/2$ | -50 | 50 | µA |
| I_{ILL} | Three level input LOW current | Three level input pins | $V_{IN} = \text{GND}$ | -200 | - | µA |
| LVDIFF Input Pins (REF[A:B]±) | | | | | | |
| V_{DIFF} | Input differential voltage | | | 400 | V_{CC} | mV |
| V_{IHHP} | Highest input HIGH voltage | | | 1.0 | V_{CC} | V |
| V_{ILLP} | Lowest input LOW voltage | | | GND | $V_{CC} - 0.4$ | V |
| V_{COM} | Common mode range (crossing voltage) | | | 0.8 | V_{CC} | V |

Note

4. These inputs are normally wired to V_{CC} , GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold the unconnected inputs at $V_{CC}/2$. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all data sheet limits are achieved.

Electrical Characteristics Over the Operating Range (continued)

| Parameter | Description | | Test Conditions | Min. | Max. | Unit |
|--------------------------|--|-----------|---|------|------|------|
| Operating Current | | | | | | |
| I _{CCI} | Internal operating current | CY7B9930V | V _{CC} = Max., f _{MAX} ^[5] | – | 200 | mA |
| | | CY7B9940V | | – | 200 | mA |
| I _{CCN} | Output current dissipation/pair ^[6] | CY7B9930V | V _{CC} = Max., C _{LOAD} = 25 pF, R _{LOAD} = 50Ω at V _{CC} /2, f _{MAX} | – | 40 | mA |
| | | CY7B9940V | | – | 50 | mA |

Capacitance

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|-----------------|-------------------|--|------|------|------|
| C _{IN} | Input capacitance | T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V | – | 5 | pF |

Switching Characteristics

Over the Operating Range^[7, 8, 9, 10, 11]

| Parameter | Description | | CY7B9930/40V-2 | | CY7B9930/40V-5 | | Unit |
|--------------------------------|---|-----------|----------------|------|----------------|------|--------------|
| | | | Min. | Max. | Min. | Max. | |
| f _{in} | Clock input frequency | CY7B9930V | 12 | 100 | 12 | 100 | MHz |
| | | CY7B9940V | 24 | 200 | 24 | 200 | MHz |
| f _{out} | Clock output frequency | CY7B9930V | 12 | 100 | 12 | 100 | MHz |
| | | CY7B9940V | 24 | 200 | 24 | 200 | MHz |
| t _{SKEWPR} | Matched pair skew ^[12, 13] | | – | 185 | – | 185 | ps |
| t _{SKEWBNK} | Intrabank skew ^[12, 13] | | – | 200 | – | 250 | ps |
| t _{SKEW0} | Output-Output skew (same frequency and phase, rise to rise, fall to fall) ^[12, 13] | | – | 250 | – | 550 | ps |
| t _{SKEW1} | Output-Output skew (same frequency and phase, other banks at different frequency, rise to rise, fall to fall) ^[12, 13] | | – | 250 | – | 650 | ps |
| t _{CCJ1-3} | Cycle-to-cycle jitter (divide by 1 output frequency, FB = divide by 1, 2, 3) | | – | 150 | – | 150 | ps Peak-Peak |
| t _{CCJ4-12} | Cycle-to-cycle jitter (divide by 1 output frequency, FB = divide by 4, 5, 6, 8, 10, 12) | | – | 100 | – | 100 | ps Peak-Peak |
| t _{PD} | Propagation delay, REF to FB Rise | | –250 | 250 | –500 | 500 | ps |
| t _{PDELTA} | Propagation delay difference between two devices ^[14] | | – | 200 | | 200 | ps |
| t _{REFpwh} | REF input (pulse width HIGH) ^[15] | | 2.0 | – | 2.0 | – | ns |
| t _{REFpwl} | REF input (pulse width LOW) ^[15] | | 2.0 | – | 2.0 | – | ns |
| t _r /t _f | Output rise/fall time ^[16] | | 0.15 | 2.0 | 0.15 | 2.0 | ns |

Notes

5. I_{CCI} measurement is performed with Bank1 and FB Bank configured to run at maximum frequency (f_{NOM} = 100 MHz for CY7B9930V, f_{NOM} = 200 MHz for CY7B9940V), and all other clock output banks to run at half the maximum frequency. FS and OUTPUT_MODE are asserted to the HIGH state.
6. This is dependent upon frequency and number of outputs of a bank being loaded. The value indicates maximum I_{CCN} at maximum frequency and maximum load of 25 pF terminated to 50Ω at V_{CC}/2.
7. This is for non-three level inputs.
8. Assumes 25 pF Max. Load Capacitance up to 185 Mhz. At 200 MHz the max load is 10 pF.
9. Both outputs of pair must be terminated, even if only one is being used.
10. Each package must be properly decoupled.
11. AC parameters are measured at 1.5V, unless otherwise indicated.
12. Test Load C_L = 25 pF, terminated to V_{CC}/2 with 50Ω.
13. SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same phase delay has been selected when all outputs are loaded with 25 pF and properly terminated up to 185 MHz. At 200 MHz the max load is 10 pF.
14. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
15. Tested initially and after any design or process changes that may affect these parameters.
16. Rise and fall times are measured between 2.0V and 0.8V.

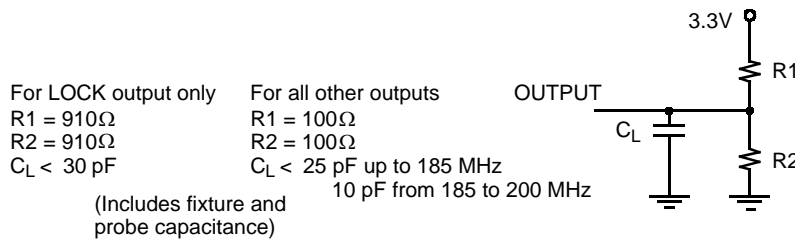
Switching Characteristics

Over the Operating Range^[7, 8, 9, 10, 11] (continued)

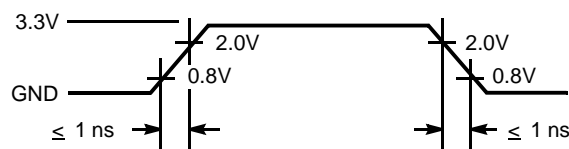
| Parameter | Description | CY7B9930/40V-2 | | CY7B9930/40V-5 | | Unit |
|----------------------|--|----------------|-------|----------------|-------|---------------|
| | | Min. | Max. | Min. | Max. | |
| t_{LOCK} | PLL lock time from power up | – | 10 | – | 10 | ms |
| t_{RELOCK1} | PLL relock time (from same frequency, different phase) with stable power supply | – | 500 | – | 500 | μs |
| t_{RELOCK2} | PLL Relock Time (from different frequency, different phase) with Stable Power Supply ^[17] | – | 1000 | – | 1000 | μs |
| t_{ODCV} | Output duty cycle deviation from 50% ^[11] | –1.0 | 1.0 | –1.0 | 1.0 | ns |
| t_{PWH} | Output HIGH time deviation from 50% ^[18] | – | 1.5 | – | 1.5 | ns |
| t_{PWL} | Output LOW time deviation from 50% ^[18] | – | 2.0 | – | 2.0 | ns |
| t_{PDEV} | Period deviation when changing from reference to reference ^[19] | – | 0.025 | – | 0.025 | UI |
| t_{OAZ} | DIS[1:2] HIGH to output high impedance from ACTIVE ^[12, 20] | 1.0 | 10 | 1.0 | 10 | ns |
| t_{OZA} | DIS[1:2] LOW to output ACTIVE from output is high impedance ^[20, 21] | 0.5 | 14 | 0.5 | 14 | ns |

AC Test Loads and Waveform

See note. [22]



(a) LVTTTL AC Test Load



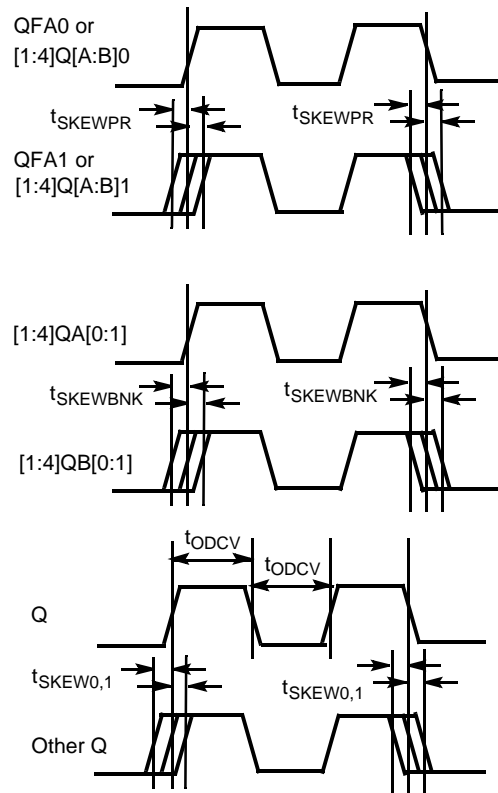
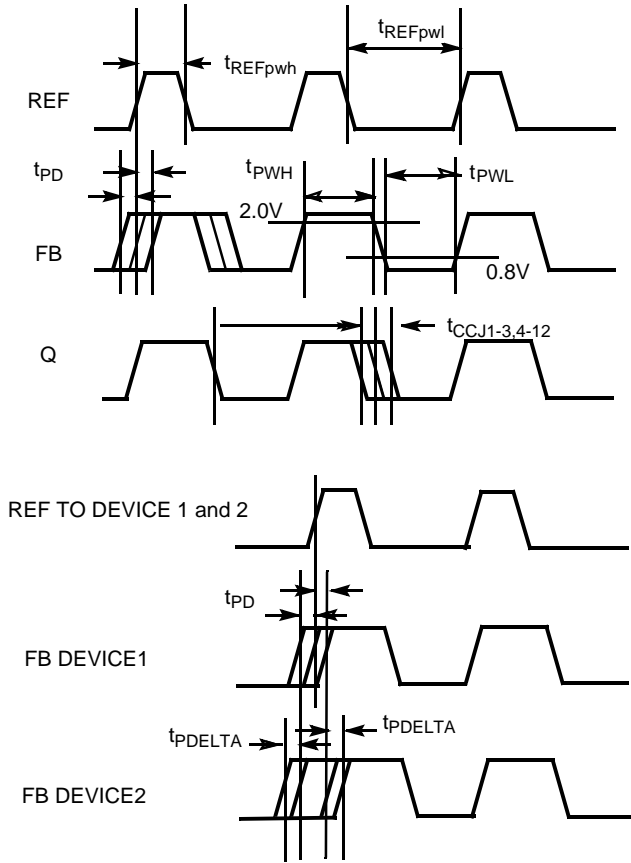
(b) TTL Input Test Waveform

Notes

17. f_{NOM} must be within the frequency range defined by the same FS state.
18. t_{PWH} is measured at 2.0V. t_{PWL} is measured at 0.8V.
19. UI = Unit Interval. Examples: 1 UI is a full period. 0.1 UI is 10% of period.
20. Measured at 0.5V deviation from starting voltage.
21. For t_{OZA} minimum, $C_L = 0$ pF. For t_{OZA} maximum, $C_L = 25$ pF to 18 MHz, 10 pF from 185 to 200 MHz.
22. These figures are for illustration only. The actual ATE loads may vary.

AC Timing Diagrams

See note. [11]



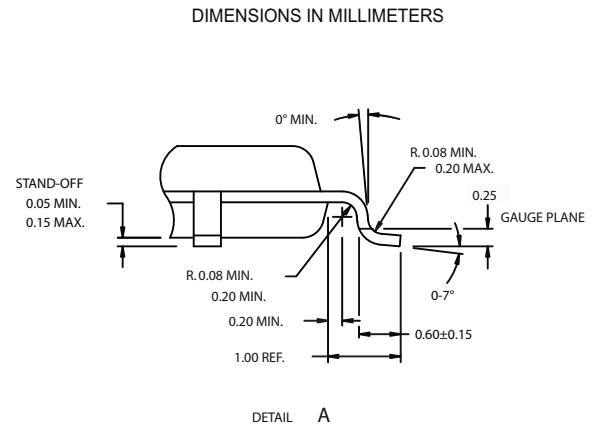
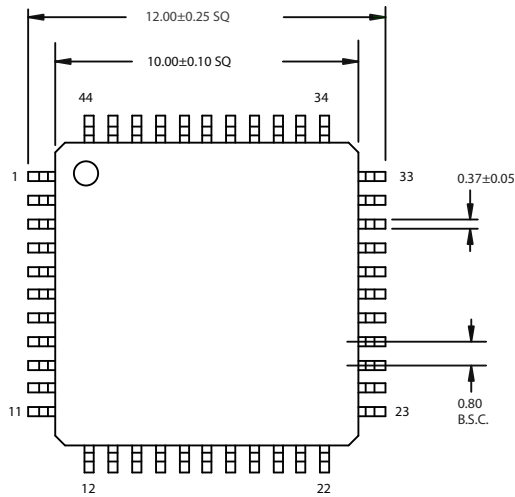
Ordering Information

| Propagation Delay (ps) | Max. Speed (MHz) | Ordering Code | Package Type | Operating Range |
|------------------------|------------------|-------------------------------|---|-----------------|
| 500 | 100 | CY7B9930V-5AC ^[23] | 44-Lead Thin Quad Flat Pack | Commercial |
| 500 | 100 | CY7B9930V-5AI ^[23] | 44-Lead Thin Quad Flat Pack | Industrial |
| 500 | 200 | CY7B9940V-5AC | 44-Lead Thin Quad Flat Pack | Commercial |
| 500 | 200 | CY7B9940V-5AI ^[23] | 44-Lead Thin Quad Flat Pack | Industrial |
| 250 | 100 | CY7B9930V-2AC ^[23] | 44-Lead Thin Quad Flat Pack | Commercial |
| 250 | 200 | CY7B9940V-2AC | 44-Lead Thin Quad Flat Pack | |
| 250 | 100 | CY7B9930V-2AI ^[23] | 44-Lead Thin Quad Flat Pack | Industrial |
| 250 | 200 | CY7B9940V-2AI ^[23] | 44-Lead Thin Quad Flat Pack | |
| Pb-free | | | | |
| 500 | 100 | CY7B9930V-5AXC | 44-Lead Thin Quad Flat Pack | Commercial |
| 500 | 100 | CY7B9930V-5AXCT | 44-Lead Thin Quad Flat Pack–Tape and Reel | Commercial |
| 500 | 200 | CY7B9940V-5AXC | 44-Lead Thin Quad Flat Pack | Commercial |
| 500 | 200 | CY7B9940V-5AXCT | 44-Lead Thin Quad Flat Pack–Tape and Reel | |
| 500 | 200 | CY7B9940V-5AXI | 44-Lead Thin Quad Flat Pack | Industrial |
| 500 | 200 | CY7B9940V-5AXIT | 44-Lead Thin Quad Flat Pack–Tape and Reel | |
| 250 | 200 | CY7B9940V-2AXC | 44-Lead Thin Quad Flat Pack | Commercial |
| 250 | 200 | CY7B9940V-2AXCT | 44-Lead Thin Quad Flat Pack–Tape and Reel | |
| 250 | 200 | CY7B9940V-2AXI | 44-Lead Thin Quad Flat Pack | Industrial |
| 250 | 200 | CY7B9940V-2AXIT | 44-Lead Thin Quad Flat Pack–Tape and Reel | |

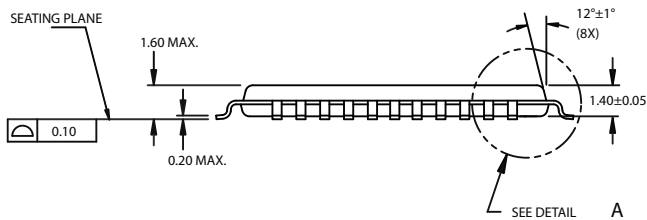
Note
23. It is an obsolete device.

Package Diagrams

44 Lead Thin Plastic Quad Flatpack 10 X 10 X 1.4mm



51-85064- *C



RoboClockII is a trademark of Cypress Semiconductor.

Document History Page

| Document Title: RoboClockII™ Junior, CY7B9930V, CY7B9940V High Speed Multifrequency PLL Clock Buffer | | | | |
|--|---------|------------|-----------------|---|
| Document Number: 38-07271 | | | | |
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 110536 | 12/02/01 | SZV | Change from Spec number: 38-01141 |
| *A | 115109 | 7/03/02 | HWT | Add 44TQFP package for both CY7B9930/40V – Industrial Operating Range |
| *B | 128463 | 7/29/03 | RGL | Added clock input frequency (f_{in}) specifications in the switching characteristics table. Added Min. values for the clock output frequency (f_{out}) in the switching characteristics table. |
| *C | 1346903 | 8/8/07 | WWZ/VED/ ARI | Update the ordering info to reflect the current status and Pb-free part numbers. Implemented new template. Updated the package diagram. |

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