# Monolithic Fixed-Output 400mA Buck Regulator with Dual 150mA LDOs in 2mm × 2mm DFN

## FEATURES

- **Triple Output Supply From a Single 2.9V to 5.5V Input**
- **Buck DC/DC: Fixed 1.2V Output, Up to 400mA**
- **LDO1: Fixed 2.8V Output, Up to 150mA**
- **LDO2: Fixed 1.8V Output, Up to 150mA**
- **±2.5% Reference Accuracy**
- **Constant-Frequency 2.25MHz Operation**
- Minimum External Component Count
- Current Mode Operation for Excellent Line and Load Transient Response
- Internal Soft-Start for Each Output
- Single Enable Pin Turns On/Shuts Down All Three Outputs
- Tiny 2mm × 2mm × 0.75mm DFN Package

## APPLICATIONS

- DMB and DVB-H Cellphones
- Handheld Products (PDA, PMP, GPS)
- Multivoltage Power for Digital Logic, I/O, FPGAs, CPLDs, ASICs, CPUs, and RF Chipsets

## DESCRIPTION

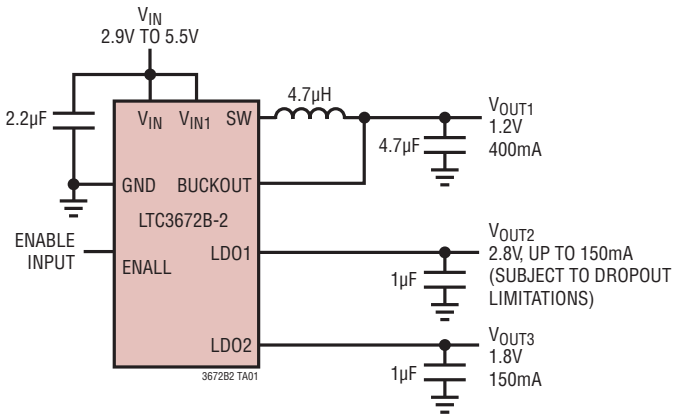
The LTC®3672B-2 is a triple power supply composed of a 400mA synchronous buck regulator and two 150mA low-dropout linear regulators (LDOs). Constant-frequency 2.25MHz operation is maintained down to very light loads. The input supply range of 2.9V to 5.5V is especially well-suited for single-cell Lithium-Ion and Lithium-Polymer applications, and for powering low voltage ASICs from 3.3V or 5V rails.

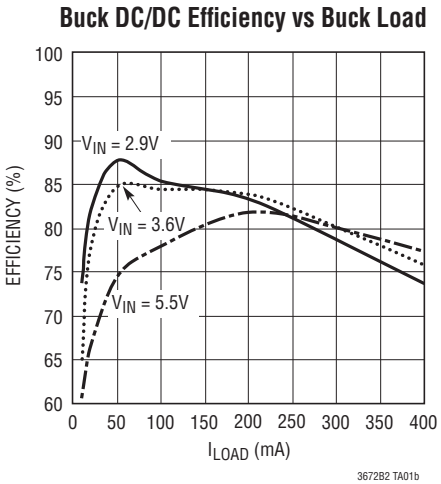
The LTC3672B-2 regulates 1.2V at the buck output, 2.8V at the LDO1 output, and 1.8V at the LDO2 output. External component count is minimal—all that is needed is a single inductor, an input capacitor, and output capacitors for each of the three outputs. Control loop compensation is internal to the LTC3672B-2.

The LTC3672B-2 is available in a 2mm × 2mm × 0.75mm 8-Lead DFN package.



## TYPICAL APPLICATION



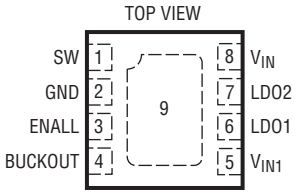



## ABSOLUTE MAXIMUM RATINGS

**(Notes 1, 3)**

$V_{IN}$ ..... –0.3V to 6V
$V_{IN1}$, BUCKOUT, ENALL, SW,
LDO2 .....–0.3V to the Lesser of ($V_{IN}$ + 0.3V) or 6V
LDO1 .....–0.3V to the Lesser of ($V_{IN1}$ + 0.3V) or 6V
Junction Temperature ..... 125°C
Operating Temperature Range (Note 2).....–40 to 85°C
Storage Temperature Range.....–65 to 125°C

## PIN CONFIGURATION




DC PACKAGE
8-LEAD (2mm × 2mm) PLASTIC DFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 102°C/W, $\theta_{JC}$ = 20°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC3672BEDC-2#PBF | LTC3672BEDC-2#TRPBF | LDBH | 8-Lead (2mm × 2mm) Plastic DFN | –40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = $V_{IN1}$ = 3.6V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input Voltage Range | | ● | 2.9 | | 5.5 | V |
| $V_{UVLO}$ | $V_{IN}$ Undervoltage Lockout Threshold | $V_{IN}$ Rising | | | 1.7 | 2 | V |
| | Undervoltage Lockout Hysteresis | | | | 12 | 100 | mV |
| $I_{Q,VIN}$ | $V_{IN}$ Quiescent Current<br>All Outputs Enabled, No Load<br>Shutdown | (Note 4)<br>$V_{BUCKOUT}$ = 1.3V<br>$V_{ENALL}$ = 0V | | | 260 | 400<br>1 | µA<br>µA |
| $I_{Q,VIN1}$ | $V_{IN1}$ Quiescent Current<br>All Outputs Enabled, No Load<br>Shutdown | <br><br>$V_{ENALL}$ = 0V | | | 2.3 | 5<br>1 | µA<br>µA |
| $V_{IL}$ | ENALL Pin Logic Low Voltage | | ● | | | 0.4 | V |
| $V_{IH}$ | ENALL Pin Logic High Voltage | | ● | 1.2 | | | V |
| $R_{ENALL}$ | ENALL Pin Pulldown Resistance | | | | 5.5 | | MΩ |
| **Synchronous Buck Regulator** | | | | | | | |
| $f_{OSC}$ | Oscillator Frequency | | | 1.8 | 2.25 | 2.7 | MHz |
| $V_{BUCKOUT}$ | Regulated Output Voltage | | ● | 1.17 | 1.2 | 1.23 | V |
| $I_{MAXP}$ | PMOS Switch Maximum Peak Current (Note 5) | | | 550 | 800 | 1100 | mA |
| $I_{OUT,BUCK}$ | Available Output Current | | | 400 | | | mA |
| $R_{P,BUCK}$ | PMOS Switch On-Resistance | | | | 0.6 | | Ω |
| $R_{N,BUCK}$ | NMOS Switch On-Resistance | | | | 0.7 | | Ω |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = $V_{IN1}$ = 3.6V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $R_{PD,BUCKOUT}$ | BUCKOUT Pulldown Resistance in Shutdown | $V_{ENALL}$ = 0V | | | 10 | | kΩ |
| $R_{PD,SW}$ | SW Pulldown Resistance in Shutdown | $V_{ENALL}$ = 0V | | | 10 | | kΩ |
| $t_{SS,BUCK}$ | Soft-Start Time | | | | 0.2 | | ms |
| **LDO Regulator 1** | | | | | | | |
| $V_{LDO1}$ | Regulated Output Voltage | LDO1 Output, $I_{LDO1}$ = 1mA | ● | 2.73 | 2.8 | 2.87 | V |
| | Line Regulation with Respect to $V_{IN}$ | $I_{LDO1}$ = 1mA, $V_{IN}$ = $V_{IN1}$ = 2.9V to 5.5V | | | 1 | | mV/V |
| | Load Regulation | $I_{LDO1}$ = 1mA to 150mA | | | –0.1 | | mV/mA |
| | Available Output Current | | | 150 | | | mA |
| | Short-Circuit Output Current | | | | 440 | | mA |
| $V_{DROP1}$ | Dropout Voltage (Note 6) | $I_{LDO1}$ = 150mA | | | 135 | 250 | mV |
| $t_{SS,LDO1}$ | Soft-Start Time | | | | 0.1 | | ms |
| $R_{PD,LDO1}$ | Output Pulldown Resistance in Shutdown | | | | 10 | | kΩ |
| **LDO Regulator 2** | | | | | | | |
| $V_{LDO2}$ | Regulated Output Voltage | LDO2 Output, $I_{LDO2}$ = 1mA | ● | 1.755 | 1.8 | 1.845 | V |
| | Line Regulation with Respect to $V_{IN}$ | $I_{LDO2}$ = 1mA, $V_{IN}$ = 2.9V to 5.5V | | | 0.6 | | mV/V |
| | Load Regulation | $I_{LDO2}$ = 1mA to 150mA | | | –0.1 | | mV/mA |
| | Available Output Current | | | 150 | | | mA |
| | Short-Circuit Output Current | | | | 450 | | mA |
| $V_{DROP2}$ | Dropout Voltage (Note 6) | $I_{LDO2}$ = 150mA | | | 290 | 400 | mV |
| $t_{SS,LDO2}$ | Soft-Start Time | | | | 0.1 | | ms |
| $R_{PD,LDO2}$ | Output Pulldown Resistance in Shutdown | | | | 10 | | kΩ |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3672B-2 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 3:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

**Note 4:** Dynamic supply current is higher due to the gate charge delivered to the buck regulator's internal MOSFET switches at the switching frequency.

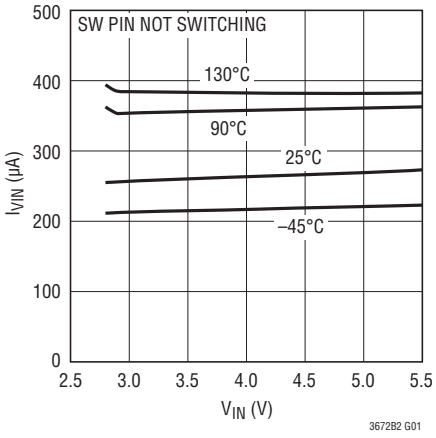
**Note 5:** The current limit features of this part are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the specified maximum specified pin current rating may result in device degradation or failure.

**Note 6:** Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. When LDO1 is in dropout, its output voltage will be equal to: $V_{IN1} – V_{DROP1}$. When LDO2 is in dropout, its output voltage will be equal to: $V_{IN} – V_{DROP2}$.

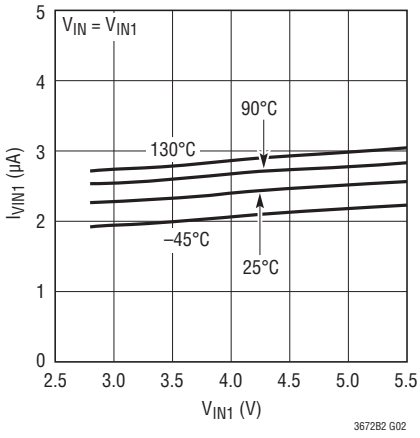
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C unless otherwise specified.

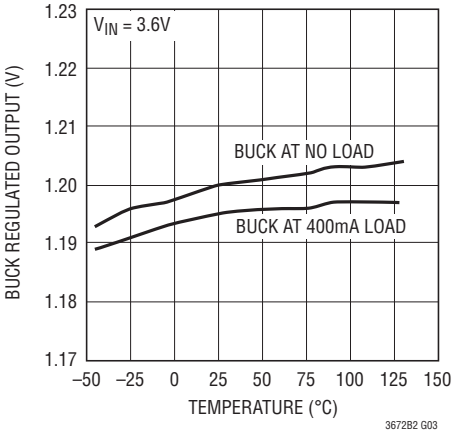
### $V_{IN}$ Quiescent Current vs $V_{IN}$ Voltage



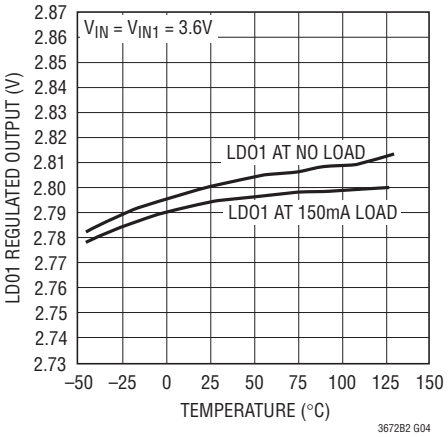

### $V_{IN1}$ Quiescent Current vs $V_{IN1}$ Voltage



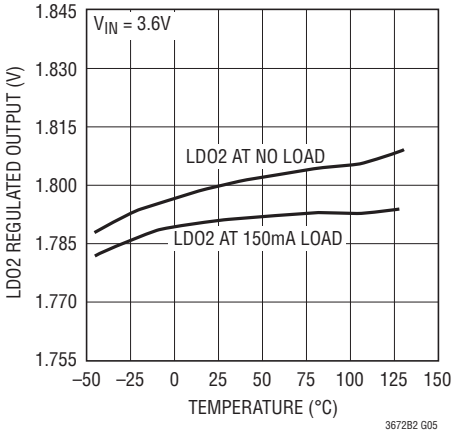

### Buck Regulated Output vs Temperature



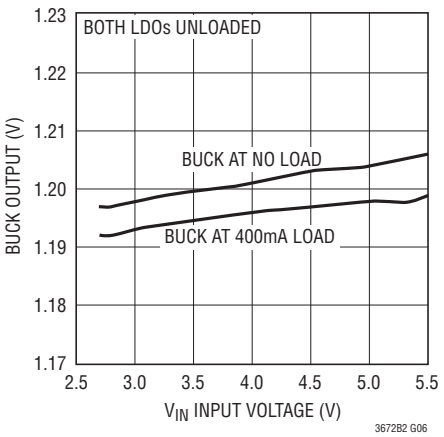

### LDO1 Regulated Output vs Temperature



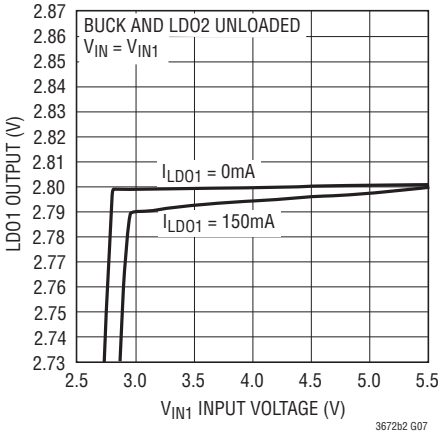

### LDO2 Regulated Output vs Temperature



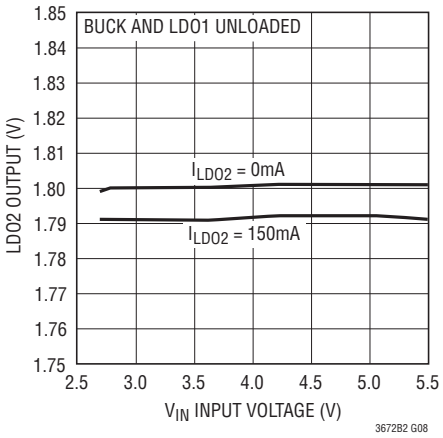

### Buck Regulated Output vs $V_{IN}$ Input Voltage




### LDO1 Regulated Output vs $V_{IN1}$ Input Voltage



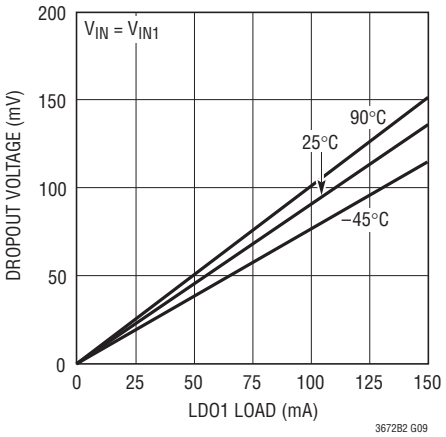

### LDO2 Regulated Output Voltage vs $V_{IN}$ Input Voltage



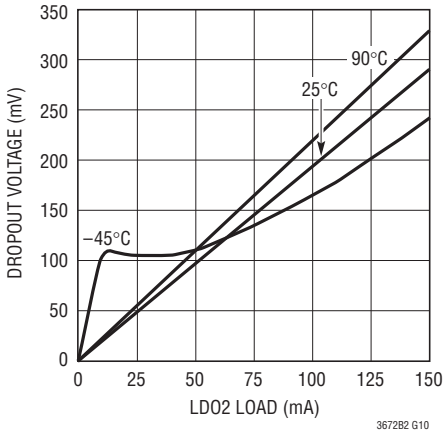
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C unless otherwise specified.

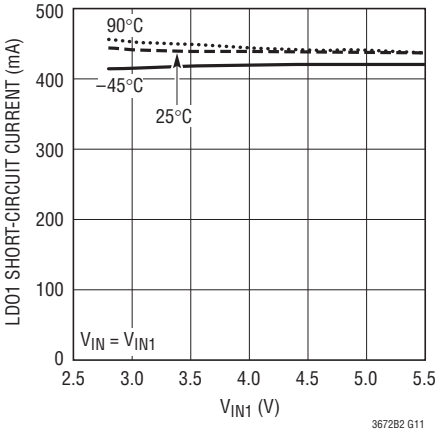
### $V_{IN1}$ – LDO1 Dropout Voltage vs Load



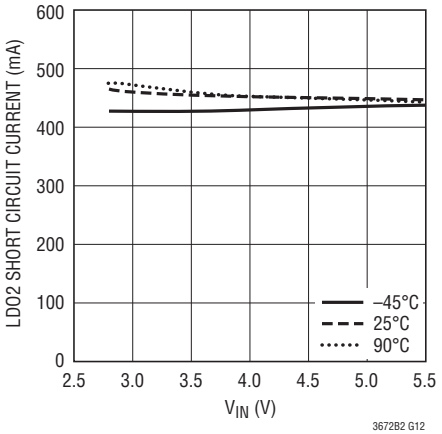

### $V_{IN}$ – LDO2 Dropout Voltage vs Load



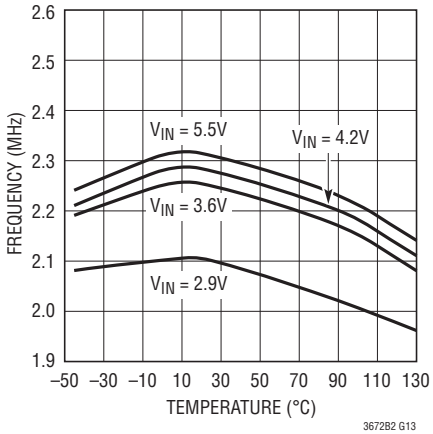

### LDO1 Short-Circuit Current vs $V_{IN1}$



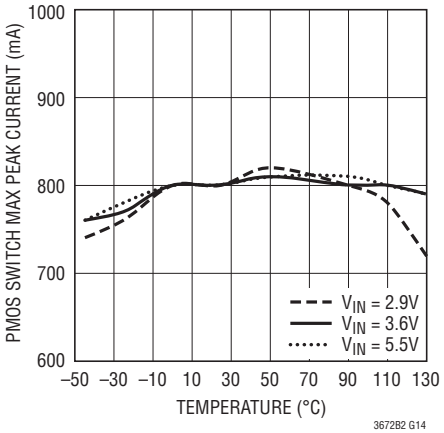

### LDO2 Short-Circuit Current vs $V_{IN}$



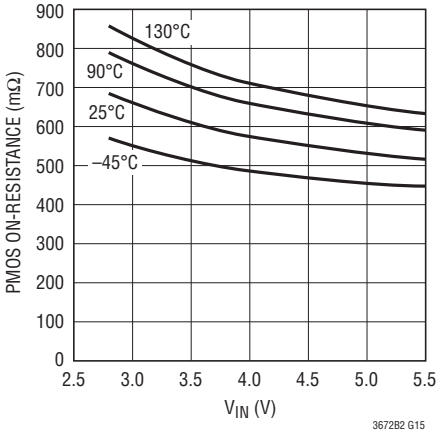

### Buck Oscillator Frequency vs Temperature




### PMOS Switch Maximum Peak Current vs Temperature




### Buck PMOS Switch On-Resistance vs Temperature



## PIN FUNCTIONS

**SW (Pin 1):** Switch Node Connection to Inductor. This pin connects to the drains of the buck regulator's main PMOS and synchronous NMOS switches.

**GND (Pin 2):** Ground.

**ENALL (Pin 3):** Enables all three outputs when high, shuts down the IC when low. This is a MOS gate input. An internal 5.5MΩ resistor pulls this pin to ground.

**BUCKOUT (Pin 4):** Output Voltage Sense Connection for the Buck Regulator.

**$V_{IN1}$ (Pin 5):** Power Input for the First Low Dropout Linear Regulator, LDO1. This pin may be connected to $V_{IN}$ (Pin 8), or to a voltage never exceeding $V_{IN}$.

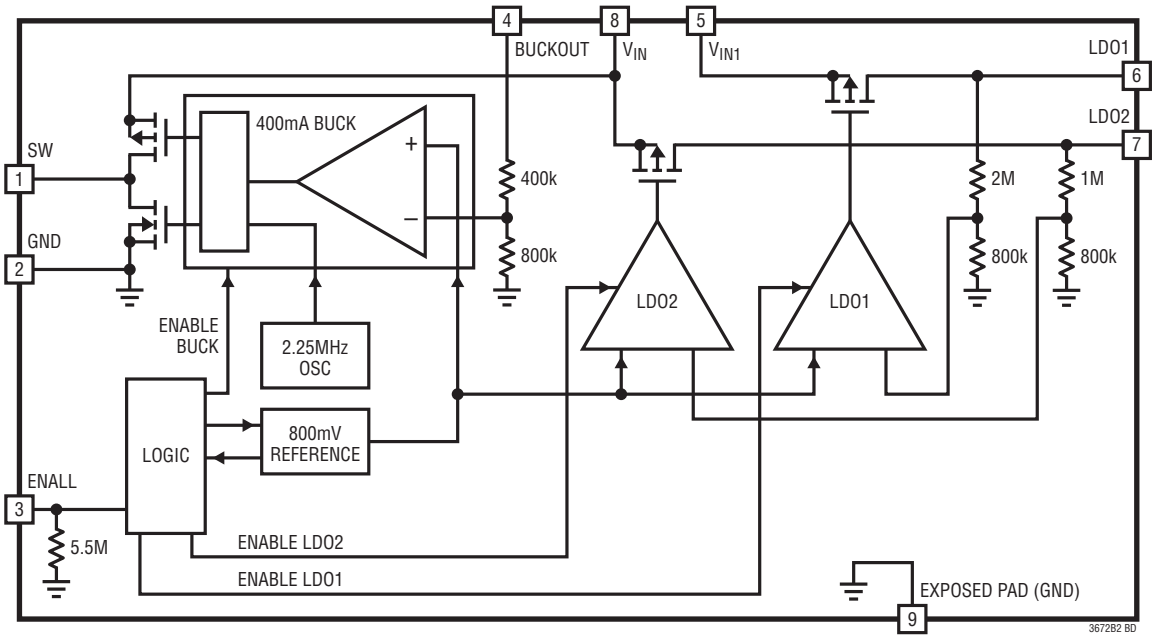
**LDO1 (Pin 6):** Output of the First Low Dropout Linear Regulator. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

**LDO2 (Pin 7):** Output of the Second Low Dropout Linear Regulator. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

**$V_{IN}$ (Pin 8):** Input Bias Supply for the IC, and Power Input for the Buck Regulator and LDO2. This pin should be bypassed to ground with a 2.2µF or greater ceramic capacitor.

**Exposed Pad (Pin 9):** Ground. The Exposed Pad must be soldered to PCB ground.

## BLOCK DIAGRAM



## OPERATION

### INTRODUCTION

The LTC3672B-2 combines a synchronous buck converter with two low dropout linear DC regulators (LDOs) to provide three low voltage outputs from a higher voltage input source. All outputs are enabled and disabled together through the ENALL pin. The output regulation voltages are set during manufacturing to 1.2V nominal for the buck, 2.8V nominal for LDO1, and 1.8V nominal for LDO2.

For versions of the IC with different output regulation voltages, consult the LTC factory.

### SYNCHRONOUS BUCK REGULATOR

The synchronous buck uses a constant-frequency current mode architecture, switching at 2.25MHz down to very light loads, and supports no-load operation by skipping cycles. When the input voltage drops very close to or falls below the target output voltage, the buck supports 100% duty cycle operation (low dropout mode). Soft-start circuitry limits inrush current when powering on. Output current is limited in the event of an output short-circuit. The switch node is slew-rate limited to reduce EMI radiation. The buck regulation control-loop compensation is internal to the IC, and requires no external components.

#### Main Control Loop

An error amplifier monitors the difference between an internal reference voltage and the voltage on the BUCKOUT pin. When the BUCKOUT voltage is below the reference, the error amplifier output voltage increases. When the BUCKOUT voltage exceeds the reference, the error amplifier output voltage decreases.

The error amplifier output controls the peak inductor current through the following mechanism: Paced by a free-running 2.25MHz oscillator, the main P-channel MOSFET switch is turned on at the start of the oscillator cycle. Current flows from the $V_{IN}$ supply through this PMOS switch, through the inductor via the SW pin, and into the output capacitor and load. When the current reaches the level programmed by the output of the error amplifier, the PMOS is shut off, and the N-channel MOSFET synchronous rectifier turns on. Energy stored in the inductor discharges into the load through this NMOS. The NMOS turns off at the end of the 2.25MHz cycle, or sooner, if the current through it drops to zero before the end of the cycle.

Through these mechanisms, the error amplifier adjusts the peak inductor current to deliver the required output power to regulate the output voltage as sensed by the BUCKOUT pin. All necessary control-loop compensation is internal to the step-down switching regulator, requiring only a single ceramic output capacitor for stability.

#### Light Load/No-Load Cycle-Skipping

At light loads, the inductor current may reach zero before the end of the oscillator cycle, which will turn off the NMOS synchronous rectifier. In this case, the SW pin goes high impedance and will show damped “ringing”. This is known as discontinuous operation, and is normal behavior for a switching regulator. At very light load and no-load conditions, the buck will automatically skip cycles as needed to maintain output regulation.

#### Soft-Start

Soft-start in the buck regulator is accomplished by gradually increasing the maximum allowed peak inductor current over a 200µs period. This allows the output to rise slowly, controlling the inrush current required to charge up the output capacitor. A soft-start cycle occurs whenever the LTC3672B-2 is enabled, or after a fault condition has occurred (thermal shutdown or UVLO).

## OPERATION

### Switch Slew-Rate Control

The buck regulator contains new patent pending circuitry to limit the slew rate of the switch node (SW pin). This new circuitry is designed to transition the switch node over a period of a couple nanoseconds, significantly reducing radiated EMI and conducted supply noise while maintaining high efficiency.

### LOW $V_{IN}$ SUPPLY UNDERVOLTAGE LOCKOUT

An undervoltage lockout (UVLO) circuit shuts down the LTC3672B-2 when $V_{IN}$ drops below about 1.7V.

### LOW DROPOUT LINEAR REGULATORS (LDOs)

The LTC3672B-2 contains two 150mA fixed-output LDO regulators. LDO1 takes power from the $V_{IN1}$ pin and regulates a 2.8V output at the LDO1 pin. LDO2 takes power straight from $V_{IN}$ and regulates a 1.8V output at the LDO2 pin.

For stability, each LDO output must be bypassed to ground with a minimum 1µF ceramic capacitor.

## APPLICATIONS INFORMATION

### BUCK REGULATOR INDUCTOR SELECTION

Many different sizes and shapes of inductors are available from numerous manufacturers. Choosing the right inductor from such a large selection of devices can be overwhelming, but following a few basic guidelines will make the selection process much simpler.

The buck regulator is designed to work with inductors in the range of 2.2µH to 10µH. A 4.7µH inductor is a good starting point. Larger value inductors reduce ripple current, which improves output ripple voltage. Lower value inductors result in higher ripple current and improved transient response time. To maximize efficiency, choose an inductor with a low DC resistance. Choose an inductor with a DC current rating at least 1.5 times larger than the maximum load current to ensure that the inductor does not saturate during normal operation. If output short-circuit is a possible condition, the inductor should be rated to handle the maximum peak current specified for the step-down converters.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or Permalloy™ materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. Inductors that are very thin or have a very small volume typically have much higher core and DCR losses, and will not give the best efficiency. The choice of which style inductor to use often depends more on the price vs size, performance, and any radiated EMI requirements than on what the buck regulator needs to operate.

Table 1 shows several inductors that work well with the buck regulator. These inductors offer a good compromise in current rating, DCR and physical size. Consult each manufacturer for detailed information on their entire selection of inductors.

# APPLICATIONS INFORMATION

**Table 1. Recommended Inductors for the Buck Regulator**

| INDUCTOR TYPE | L (µH) | MAX $I_{DC}$ (A) | MAX DCR (Ω) | SIZE IN mm (L × W × H) | MANUFACTURER |
|---|---|---|---|---|---|
| DE2818C | 4.7 | 1.25 | 0.072 | 3 × 2.8 × 1.8 | Toko |
| | 3.3 | 1.45 | 0.053 | 3 × 2.8 × 1.8 | www.toko.com |
| D312C | 4.7 | 0.79 | 0.24 | 3.6 × 3.6 × 1.2 | |
| | 3.3 | 0.9 | 0.2 | 3.6 × 3.6 × 1.2 | |
| DE2812C | 4.7 | 1.15 | 0.13* | 3 × 2.8 × 1.2 | |
| | 3.3 | 1.37 | 0.105* | 3 × 2.8 × 1.2 | |
| CDRH3D16 | 4.7 | 0.9 | 0.11 | 4 × 4 × 1.8 | Sumida |
| | 3.3 | 1.1 | 0.085 | 4 × 4 × 1.8 | www.sumida.com |
| CDRH2D11 | 4.7 | 0.5 | 0.17 | 3.2 × 3.2 × 1.2 | |
| | 3.3 | 0.6 | 0.123 | 3.2 × 3.2 × 1.2 | |
| CLS4D09 | 4.7 | 0.75 | 0.19 | 4.9 × 4.9 × 1 | |
| SD3118 | 4.7 | 1.3 | 0.162 | 3.1 × 3.1 × 1.8 | Cooper |
| | 3.3 | 1.59 | 0.113 | 3.1 × 3.1 × 1.8 | www.cooperet.com |
| SD3112 | 4.7 | 0.8 | 0.246 | 3.1 × 3.1 × 1.2 | |
| | 3.3 | 0.97 | 0.165 | 3.1 × 3.1 × 1.2 | |
| SD12 | 4.7 | 1.29 | 0.117* | 5.2 × 5.2 × 1.2 | |
| | 3.3 | 1.42 | 0.104* | 5.2 × 5.2 × 1.2 | |
| SD10 | 4.7 | 1.08 | 0.153* | 5.2 × 5.2 × 1 | |
| | 3.3 | 1.31 | 0.108* | 5.2 × 5.2 × 1 | |
| LPS3015 | 4.7 | 1.1 | 0.2 | 3 × 3 × 1.5 | Coil Craft |
| | 3.3 | 1.3 | 0.13 | 3 × 3 × 1.5 | www.coilcraft.com |

* = Typical DCR

## INPUT/OUTPUT CAPACITOR SELECTION

Low ESR (equivalent series resistance) ceramic capacitors should be used to bypass the following pins to ground: $V_{IN}$, $V_{IN1}$, the buck output, LDO1, and LDO2. Only X5R or X7R ceramic capacitors should be used because they retain their capacitance over wider voltage and temperature ranges than other ceramic types. A 10µF output capacitor is sufficient for the buck regulator output. For good transient response and stability the output capacitor for the buck regulator should retain at least 4µF of capacitance over operating temperature and bias voltage. The $V_{IN}$ pin should be bypassed with a 2.2µF capacitor. The LDO1 and LDO2 output pins should be bypassed with a 1µF capacitor or greater. $V_{IN1}$ should be bypassed with a 1µF capacitor, which may be omitted if $V_{IN1}$ is tied to the $V_{IN}$ pin.

Consult with capacitor manufacturers for detailed information on their selection and specifications of ceramic capacitors. Many manufacturers now offer very thin (<1mm tall) ceramic capacitors ideal for use in height-restricted designs. Table 2 shows a list of several ceramic capacitor manufacturers.

**Table 2. Ceramic Capacitor Manufacturers**

| | |
|---|---|
| AVX | www.avxcorp.com |
| Murata | www.murata.com |
| Taiyo Yuden | www.t-yuden.com |
| Vishay Siliconix | www.vishay.com |
| TDK | www.tdk.com |

## APPLICATIONS INFORMATION

### PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

When laying out the printed circuit board, the following list should be followed to ensure proper operation of the LTC3672B-2:

1) The Exposed Pad of the package should connect directly to a large ground plane to minimize thermal and electrical impedance.

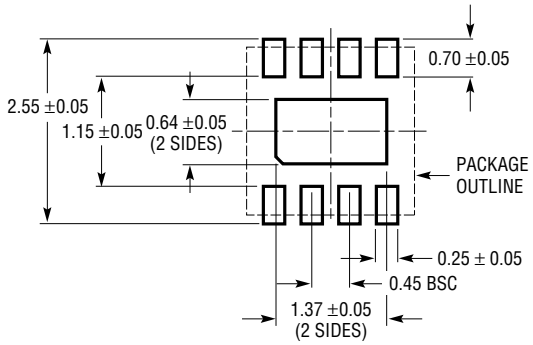
2) The connections from the input supply pins ($V_{IN}$ and $V_{IN1}$) to their respective decoupling capacitors should be kept as short as possible. The GND side of these capacitors should connect directly to the ground plane of the part. The $V_{IN}$ capacitor provides the AC current to the buck regulator's power MOSFETs and their drivers. It is especially important to minimize PCB trace inductance from this capacitor to the $V_{IN}$ and GND pins of the LTC3672B-2.

3) The switching power trace connecting the SW pin to the inductor should be kept as short as possible to reduce radiated EMI and parasitic coupling.

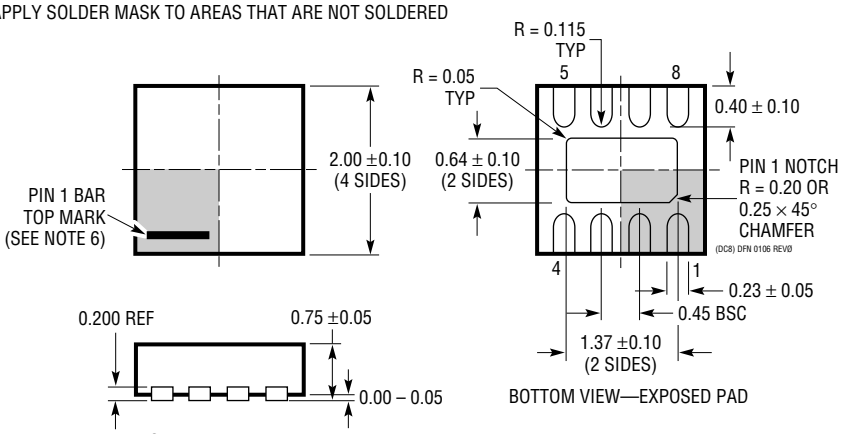
4) The LDO output capacitors should be placed as close to the IC as possible, and connect to the LDO outputs and the GND pin as directly as possible.

# PACKAGE DESCRIPTION

**DC Package**
**8-Lead Plastic DFN (2mm × 2mm)**
(Reference LTC DWG # 05-08-1719 Rev Ø)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

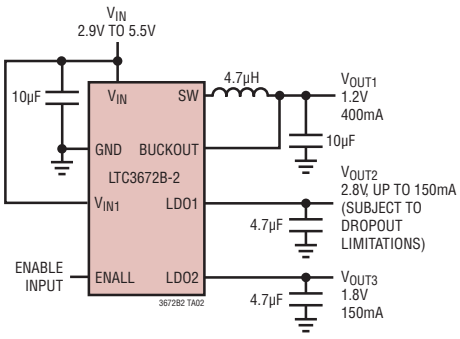



BOTTOM VIEW—EXPOSED PAD

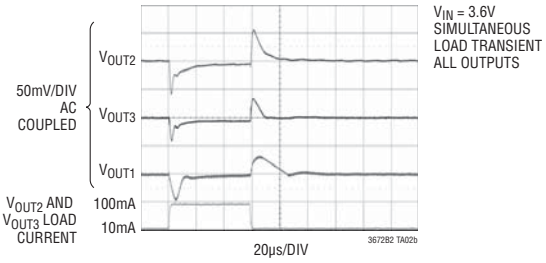
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## TYPICAL APPLICATION

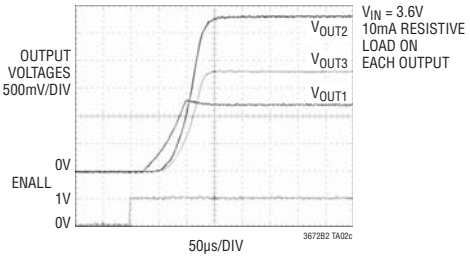
**LTC3672B-2 with More LDO Output Capacitance for Improved Transient Response**




**Load Transient Response**




**Start-Up Transient**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC3405/LTC3405A | 300mA $I_{OUT}$, 1.5MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 20µA, $I_{SD}$ <1µA, ThinSOT™ Package |
| LTC3406A/LTC3406AB | 600mA $I_{OUT}$, 1.5MHz, Synchronous Step-Down DC/DC Converter | 96% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 20µA, $I_{SD}$ <1µA, ThinSOT Package |
| LTC3407A/ LTC3407A-2 | Dual 600mA/800mA $I_{OUT}$, 1.5MHz/2.25MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 40µA, $I_{SD}$ <1µA, MS10E Package |
| LTC3410/LTC3410B | 300mA $I_{OUT}$, 2.25MHz, Synchronous Step-Down DC/DC Converter | 96% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 26µA, $I_{SD}$ <1µA, SC70 Package |
| LTC3411 | 1.25A $I_{OUT}$, 4MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 60µA, $I_{SD}$ <1µA, MS10 Package |
| LTC3419 | Dual 600mA Synchronous 2.75MHz Step-Down DC/DC | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 35µA, $I_{SD}$ < 1µA, 3mm × 3mm DFN, MS10 Package |
| LTC3445 | $I^2C$ Controllable 600mA Synchronous Buck Regulator with Two 50mA LDOs in a 4mm × 4mm QFN | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.85V, $I_Q$ = 360µA, $I_{SD}$ <27µA, 4mm × 4mm QFN Package |
| LTC3446 | Synchronous 1A, 2.25MHz Step-Down DC/DC Regulator with Dual VLDOs | 95% Efficiency, $V_{IN}$: 2.7V to 5.5V, $V_{OUT(MIN)}$ = 0.4V, $I_Q$ = 140µA, $I_{SD}$ <1µA, 3mm × 4mm DFN Package |
| LTC3448 | 600A $I_{OUT}$, 1.5MHz/2.25MHz, Synchronous Step-Down DC/DC Converter with LDO Mode | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 32µA, $I_{SD}$ <1µA, MS10, DFN Packages |
| LTC3541/LTC3541-1/ LTC3541-2/LTC3541-3 | Synchronous 500mA, 2.25MHz Step-Down DC/DC Regulator with a 300mA VLDO in a 3mm × 3mm DFN | 95% Efficiency, $V_{IN}$: 2.7V to 5.5V, $V_{OUT(MIN)}$ = 0.4V, $I_Q$ = 85µA, $I_{SD}$ <1µA, 3mm × 3mm DFN Package |
| LTC3547/ LTC3547B | Dual 300mA $I_{OUT}$, 2.25MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 40µA, $I_{SD}$ <1µA, DFN-8 Package |
| LTC3548/LTC3548-1/ LTC3548-2 | Dual 800mA/400mA $I_{OUT}$, 2.25MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 40µA, $I_{SD}$ <1µA, MS10, DFN Packages |
| LTC3672B-1 | Monolithic Fixed-Output 400mA Buck Regulator with Dual 150mA LDOs in a 2mm × 2mm DFN | 95% Efficiency, $V_{IN}$: 2.9V to 5.5V, $I_Q$ = 260µA, Buckout = 1.8V, LD01 = 1.2V, LDO2 = 2.8V, 2mm × 2mm DFN Package |

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