

EVAL-ADF4007EB1

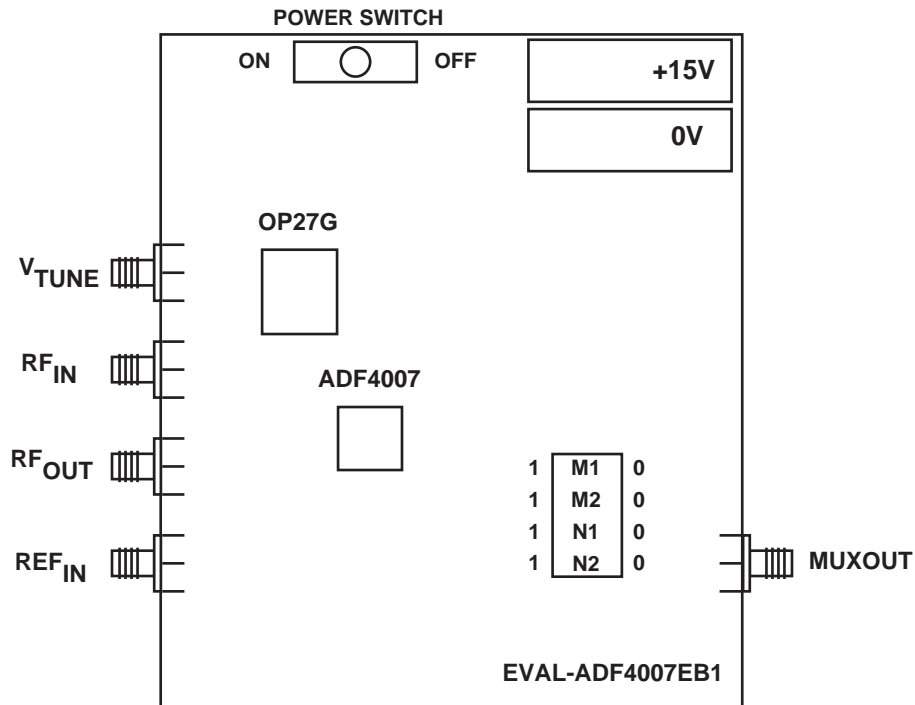
FEATURES

On -Board Regulators for +3V, +5V, +12V Power Supplies
 Includes OP27 for Active Filter Applications.
 Designed for Simple Hook-Up to External VCO Board

GENERAL DESCRIPTION

This board is designed to allow the user to evaluate the performance of the ADF4007 Frequency Synthesizer for PLL's (Phase Locked Loops). The block diagram of the board is shown below. It contains the ADF4007 synthesizer, links for choosing the divide ratio (8, 16, 32 or 64), SMA connector for the reference input, and RF input and output .

BLOCK DIAGRAM



REV.PrB 04/00

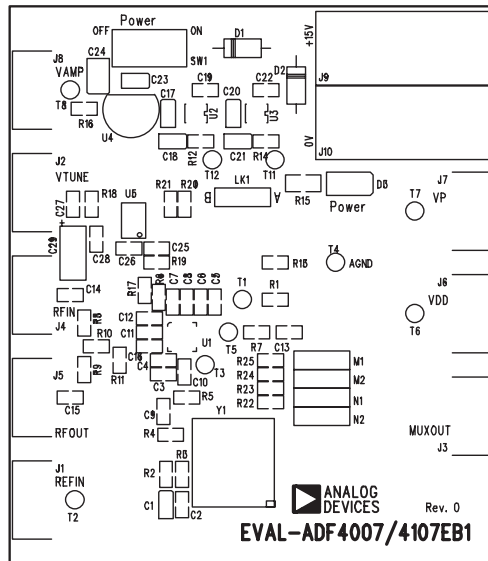
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Hardware Description

The evaluation board is designed to work with external VCO. The layout accommodate loop filter components and also has an op-amp (OP27) for an active filter, if this is needed. The silk screen for the evaluation board is shown below. The board schematic is shown on pages 3 and 4.



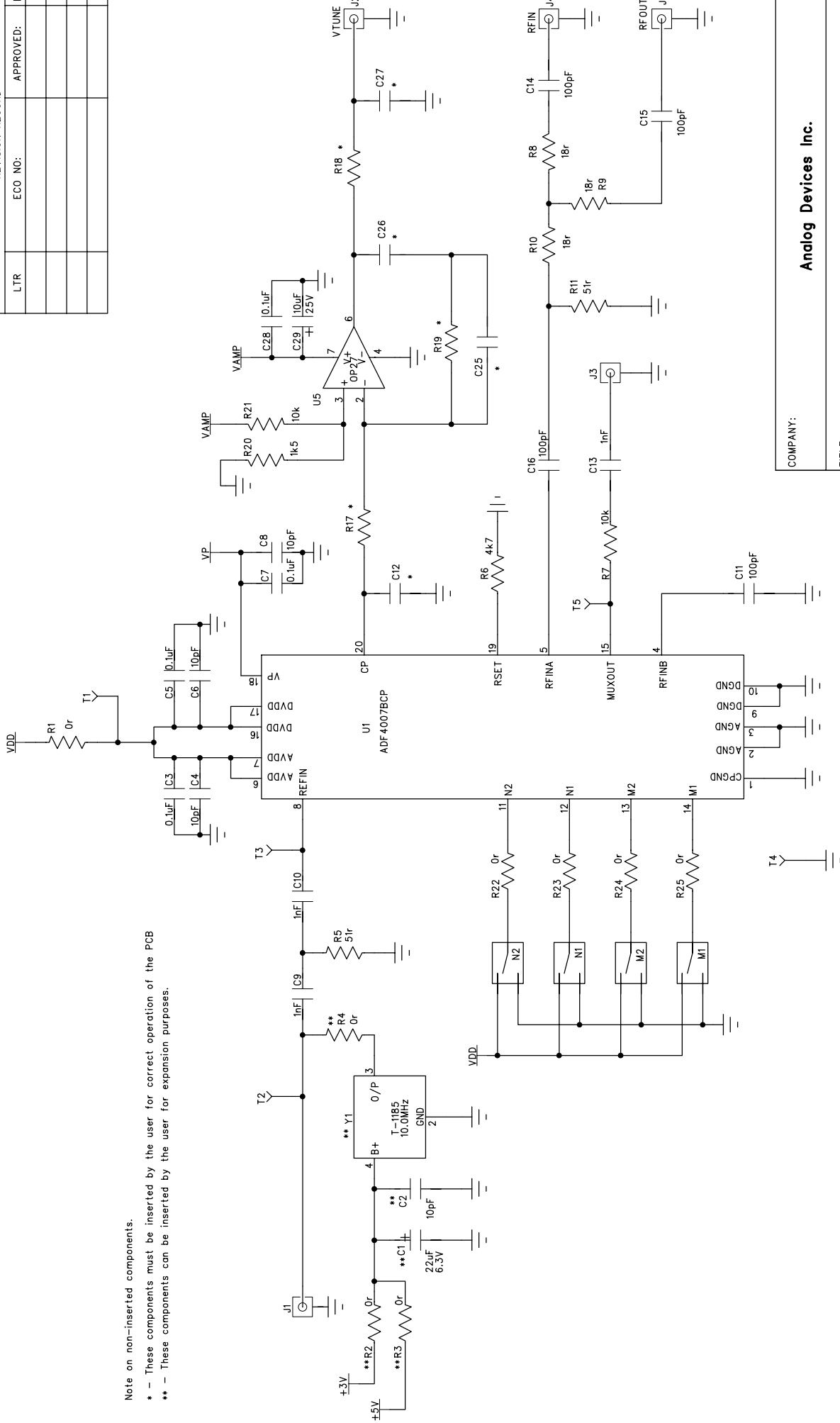
EVAL-ADF4007/107EB (Rev. 0) - COMPONENT SIDE VIEW
Silkscreen

Figure 1. Evaluation Board Silkscreen

The board is powered from a single external +15V supply. The power supply circuitry allows the user to choose either 3V or 5V for the ADF4007 V_p . The ADF4007 V_{DD} is +3.0V and the OP27 V_{CC} is +12V. **It is very important to note that the ADF4007 V_{DD} should never exceed 3.3V or the ADF4007 V_p , whichever is less. Doing so can damage the device.**

VTUNE is available at an output SMA connector. This should be connected to an external VCO board. The output of this board should then be connected back into the EVAL-ADF4007EB1 at RFIN. This is split into 2 equal power levels with one going to RFOUT and the other going to the RFIN of the ADF4007 to close the loop in the PLL. The RFOUT can be fed to a spectrum analyzer to test the output signal. It should have an amplitude 6dB down from the VCO specified output level.

REVISION RECORD	
LTR	ECO NO. APPROVED:



Note on non-inserted components.
 * - These components must be inserted by the user for correct operation of the PCB
 ** - These components can be inserted by the user for expansion purposes.

COMPANY: **Analog Devices Inc.**

TITLE: **EVAL-ADF4007EB1
 Evaluation Board Schematic**

DRAWN: Pat Sheahan	DATED: Nov 02
CHECKED: Mike Curtin	DATED: Nov 02
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

CODE: **EVAL-ADF4007EB1**

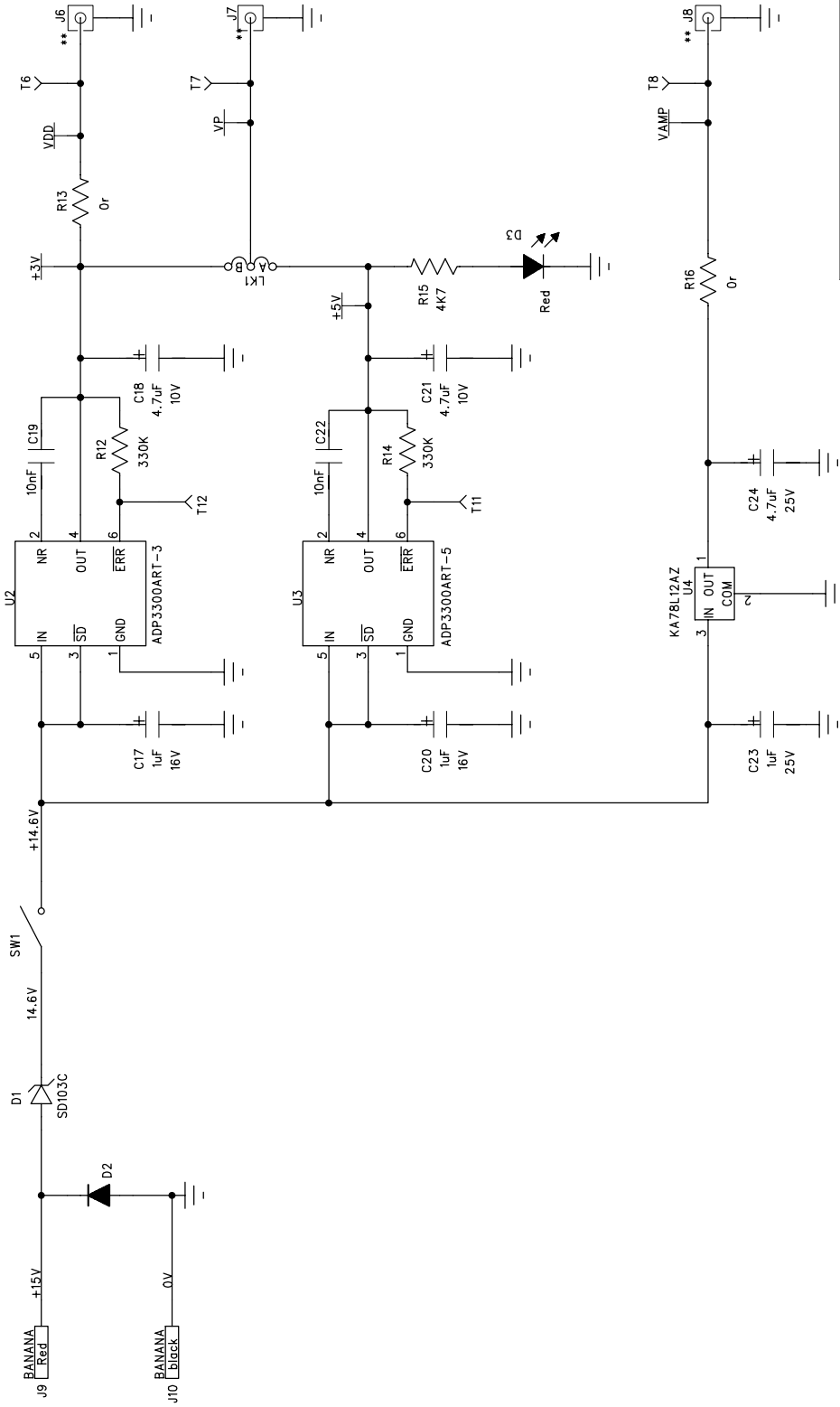
SIZE:

DRAWING NO:

SCALE:

SHEET: 1 OF 2

REVISION RECORD	
LTR	ECO NO:
	APPROVED:



COMPANY:

Analog Devices Inc.

EVAL-ADF4007EB1

Evaluation Board Schematic

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QUALITY CONTROL:	DATED:
RELEASED:	DATED:

DRAWING NO:

EVAL-ADF4007EB1

SIZE:

CODE:

SCALE:

SHEET: 2

OF 2

Table 1. Bill of Materials for the EVAL-ADF4007EB1 (Part 1)

Name	Part Type	Value	Assembly Y/N	PCB Decal	Stock Code	SMD	Layer Name
C1	CAP+	22uF 6.3V	No	CAP\TAJ_A	FEC 197-038	Yes	Top
C2	CAP	10pF	No	0603	FEC 499-110	Yes	Top
C3	CAP	0.1uF	Yes	0603	FEC 499-675	Yes	Top
C4	CAP	10pF	Yes	0603	FEC 499-110	Yes	Top
C5	CAP	0.1uF	Yes	0603	FEC 499-675	Yes	Top
C6	CAP	10pF	Yes	0603	FEC 499-110	Yes	Top
C7	CAP	0.1uF	Yes	0603	FEC 499-675	Yes	Top
C8	CAP	10pF	Yes	0603	FEC 499-110	Yes	Top
C9	CAP	1nF	Yes	0603	FEC 317-202	Yes	Top
C10	CAP	1nF	Yes	0603	FEC 317-202	Yes	Top
C11	CAP	100pF	Yes	0603	FEC 499-122	Yes	Top
C12	CAP		No	0603		Yes	Top
C13	CAP	1nF	Yes	0603	FEC 317-202	Yes	Top
C14	CAP	100pF	Yes	0603	FEC 499-122	Yes	Top
C15	CAP	100pF	Yes	0603	FEC 499-122	Yes	Top
C16	CAP	100pF	Yes	0603	FEC 499-122	Yes	Top
C17	CAP+	1uF 25V	Yes	CAP\TAJ_A	FEC 197-476	Yes	Top
C18	CAP+	4.7uF 10V	Yes	CAP\TAJ_A	FEC 498-658	Yes	Top
C19	CAP	10nF	Yes	0603	FEC 499-146	Yes	Top
C20	CAP+	1uF 25V	Yes	CAP\TAJ_A	FEC 197-476	Yes	Top
C21	CAP+	4.7uF 10V	Yes	CAP\TAJ_A	FEC 498-658	Yes	Top
C22	CAP	10nF	Yes	0603	FEC 499-146	Yes	Top
C23	CAP+	1uF 25V	Yes	CAP\TAJ_A	FEC 197-476	Yes	Top
C24	CAP+	4.7uF 25V	Yes	CAP\TAJ_B	FE 197-506	Yes	Top
C25	CAP		No	0603		Yes	Top
C26	CAP		No	0603		Yes	Top
C27	CAP		No	0603		Yes	Top
C28	CAP	0.1uF	Yes	0603	FEC 499-675	Yes	Top
C29	CAP+	10uF 25V	Yes	CAP\TAJ_C	FEC 197-518	Yes	Top
D1	SD103C	6.2V	Yes	DO35	SD103C	No	Top
D2	DIODE	IN4001	Yes	DO35	FEC 365-117	No	Top
D3	LED		Yes	LED_SMT	FEC 515-620	Yes	Top
J1	SMA		Yes	SMA_CARD_EDGE	Pasternack PE4542	Yes	Top
J2	SMA		Yes	SMA_CARD_EDGE	Pasternack PE4542	Yes	Top
J3	SMA		Yes	SMA_CARD_EDGE	Pasternack PE4542	Yes	Top
J4	SMA		Yes	SMA_CARD_EDGE	Pasternack PE4542	Yes	Top
J5	SMA		Yes	SMA_CARD_EDGE	Pasternack PE4542	Yes	Top
J6	SMA		No	SMA_CARD_EDGE	Pasternack PE4542	Yes	Top
J7	SMA		No	SMA_CARD_EDGE	Pasternack PE4542	Yes	Top
J8	SMA		No	SMA_CARD_EDGE	Pasternack PE4542	Yes	Top
J9	BANANA	Red	Yes	BANANA	FEC 150-039	No	Top
J10	BANANA	Black	Yes	BANANA	FEC 150-040	No	Top
LK1	JUMPER2\SIP3		Yes	LINK-3P	Futura JSC-16-GO	No	Top
M1	JUM_CHANGE_1		Yes	LINK-3P-NOTEXT	Futura JSC-16-GO	No	Top
M2	JUM_CHANGE_1		Yes	LINK-3P-NOTEXT	Futura JSC-16-GO	No	Top
N1	JUM_CHANGE_1		Yes	LINK-3P-NOTEXT	Futura JSC-16-GO	No	Top
N2	JUM_CHANGE_1		Yes	LINK-3P-NOTEXT	Futura JSC-16-GO	No	Top
R1	RES	0r	Yes	0603	FEC 772-227	Yes	Top
R2	RES	0r	No	0603	FEC 772-227	Yes	Top
R3	RES	0r	No	0603	FEC 772-227	Yes	Top
R4	RES	0r	No	0603	FEC 772-227	Yes	Top
R5	RES	51r	Yes	0603	Digikey 311-51.0HCT-ND	Yes	Top
R6	RES	4k7	Yes	0603	FEC 911-318	Yes	Top
R7	RES	10k	Yes	0603	FEC 911-355	Yes	Top
R8	RES	18r	Yes	0603	FEC 911-021	Yes	Top
R9	RES	18R	Yes	0603	FEC 911-021	Yes	Top
R10	RES	18R	Yes	0603	FEC 911-021	Yes	Top
R11	RES	51r	Yes	0603	Digikey 311-51.0HCT-ND	Yes	Top

Table 2. Bill of Materials for the EVAL-ADF4007EB1 (Part 2)

R12	RES	330K	Yes	0603	FEC 911-537	Yes	Top
R13	RES	0r	Yes	0603	FEC 772-227	Yes	Top
R14	RES	330K	Yes	0603	FEC 911-537	Yes	Top
R15	RES	4K7	Yes	0805	FEC 911-938	Yes	Top
R16	RES	0r	Yes	0603	FEC 772-227	Yes	Top
R17	RES		No	0603		Yes	Top
R18	RES		No	0603		Yes	Top
R19	RES		No	0603		Yes	Top
R20	RES	1k	Yes	0603	FEC 911-XXX	Yes	Top
R21	RES	10k	Yes	0603	FEC 911-355	Yes	Top
R22	RES	0r	Yes	0603	FEC 772-227	Yes	Top
R23	RES	0r	Yes	0603	FEC 772-227	Yes	Top
R24	RES	0r	Yes	0603	FEC 772-227	Yes	Top
R25	RES	0r	Yes	0603	FEC 772-227	Yes	Top
SW1	SW_POWER		Yes	SW_SIP-3P	FEC 150-559	No	Top
T1	TESTPOINT		No	TESTPOINT		No	Top
T2	TESTPOINT		No	TESTPOINT		No	Top
T3	TESTPOINT		No	TESTPOINT		No	Top
T4	TESTPOINT		No	TESTPOINT		No	Top
T5	TESTPOINT		No	TESTPOINT		No	Top
T6	TESTPOINT		No	TESTPOINT		No	Top
T7	TESTPOINT		No	TESTPOINT		No	Top
T8	TESTPOINT		No	TESTPOINT		No	Top
T11	TESTPOINT		No	TESTPOINT		No	Top
T12	TESTPOINT		No	TESTPOINT		No	Top
U1	ADF4007		Yes	CSP-20	ADF4007BCP	Yes	Top
U2	ADP3300		Yes	SOT23-6	ADP3300ART-3	Yes	Top
U3	ADP3300		Yes	SOT23-6	ADP3300ART-5	Yes	Top
U4	7812		Yes	TO-92	FEC 563-766	No	Top
U5	OP27	OP27GS	Yes	SO8NB	OP27GS	Yes	Top
Y1	OSC_TCXO	10.0MHZ	No	OSC_TCXO		Yes	Top
Corners	Rubber Stick-On Feet x4			FEC 148-922			
	Bare PCB			Eval-ADF4007/4107EB1 Rev. 0			
	RF Eval Board Cable			Aragorn Services			
	CD & Sleeve			ADI Issue			
	Barcode Label			ADI Issue			
	Eval Board Box			Europaks K-645/1			
	Anti-Static Bag			FEC 522-764			
	Anti-Static Bubble Wrap						



TEST PROCEDURE FOR EVAL-ADF4007EB1

Test Procedure

EVAL-ADF4007EB1

EQUIPMENT LIST

EVAL-ADF4007EB1 Evaluation Board
+15 Volt Power Supply
Signal Generator
Oscilloscope
Frequency Counter
Multimeter
50 ohm terminator
Two BNC to SMA Cables

STEP 1: SET LINK/SWITCH POSITIONS

Ensure Link/Switch Positions are as follows:

LK1: Position A, V_p is 5 Volts
M2: 0 (GND)
M1: 1 (DV_{DD})
N2: 1 (DV_{DD})
N1: 1 (DV_{DD})

Connect 50 ohm terminator to J5

STEP 2: POWER UP THE EVALUATION BOARD

Turn the ON Switch (SW 1) to the ON position. The Power LED should come on .

STEP 3: MEASURE THE FOLLOWING VOLTAGES

J6: +3.0 Volts
J7: +5.0 Volts
J8: +12.0 Volts

STEP 4: CHECK THE R COUNTER

Apply 40 MHz, -5 dBm signal to J1, using one BNC to SMA cable from Signal Generator.

Measure output frequency at J3, using Oscilloscope or Frequency Counter. It should be 10 MHz.

Disconnect the Signal Generator.

STEP 6: CHECK THE N COUNTER

Change M2 to 1 and M1 to 0.

Apply 640 MHz, -4 dBm signal to J1, using one BNC to SMA cable from Signal Generator.

Measure output frequency at J3, using Oscilloscope or Frequency Counter. It should be 10 MHz.

REV.PrA 11/04

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