High Isolation, Silicon SPDT, Nonreflective Switch, 9 kHz to 13.0 GHz

Data Sheet **HMC1118**

FEATURES

- Nonreflective 50 Ω design
- Positive control: 0 V/3.3 V
- Low insertion loss: 0.68 dB at 8.0 GHz
- High isolation: 48 dB at 8.0 GHz
- High power handling
  - 35 dBm through path
  - 27 dBm terminated path
- High linearity
  - 1 dB compression (P1dB): 37 dBm typical
  - Input third-order intercept (IIP3): 62 dBm typical
- ESD rating: 2 kV human body model (HBM)
- 3 mm × 3 mm, 16-lead LFCSP package
- No low frequency spurious
- Settling time (0.05 dB margin of final RF_{OUT}): 7.5 µs

APPLICATIONS

- Test instrumentation
- Microwave radios and very small aperture terminals (VSATs)
- Military radios, radars, and electronic counter measures (ECMs)
- Fiber optics and broadband telecommunications

FUNCTIONAL BLOCK DIAGRAM

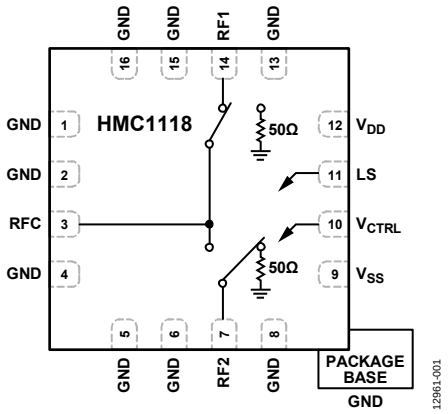

Figure 1.

GENERAL DESCRIPTION

The HMC1118 is a general-purpose, broadband, nonreflective single-pole, double-throw (SPDT) switch in a LFCSP surface mount package. Covering the 9 kHz to 13.0 GHz range, the switch offers high isolation and low insertion loss. The switch features >48 dB isolation, 0.68 dB insertion loss up to 8.0 GHz, and a 7.5 µs settling time of 0.05 dB margin of final RF_{OUT}. The switch operates using positive control voltage logic lines of +3.3 V and 0 V and requires +3.3 V and −2.5 V supplies. The HMC1118 can cover the same operating frequency range with a single positive supply voltage applied and the negative supply voltage (V_{SS}) tied to ground and still maintaining good power handling performance. The HMC1118 is packaged in a 3 mm × 3 mm, surface mount LFCSP package.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

HMC1118* PRODUCT PAGE QUICK LINKS

Last Content Update: 10/28/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMC1118 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1440: Single Positive Supply Operation for the HMC1118

Data Sheet

- HMC1118: High Isolation, Silicon SPDT, Nonreflective Switch, 9 kHz to 13.0 GHz Data Sheet

Product Highlight

- Wideband Switches: Ideal for Broad Spectrum Applications in Test, Military, and Aerospace

TOOLS AND SIMULATIONS

- HMC1118LP3DE S-Parameters

REFERENCE MATERIALS

Press

- Analog Devices Silicon SPDT Switch Delivers Fast Settling Time for Demanding Test and Measurement Applications

DESIGN RESOURCES

- HMC1118 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMC1118 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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10/2017—Rev. 0 to Rev. A

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Updated Outline Dimensions 11
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10/2015—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{CTRL} = 0 V/3.3 V dc, V_{DD} = LS = 3.3 V dc, V_{SS} = −2.5 V dc, T_A = 25°C, 50 Ω system, unless otherwise specified.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INSERTION LOSS					
	9 kHz to 3.0 GHz		0.5	1.0	dB
	9 kHz to 8.0 GHz		0.68	1.1	dB
	9 kHz to 10.0 GHz		0.7	1.3	dB
	9 kHz to 13.0 GHz		1.3	2.0	dB
ISOLATION RFC TO RF1/RF2 (WORST CASE)					
	9 kHz to 3.0 GHz	40	50		dB
	9 kHz to 8.0 GHz	42	48		dB
	9 kHz to 10.0 GHz	28	35		dB
	9 kHz to 13.0 GHz	18	25		dB
RETURN LOSS					
On State	9 kHz to 3.0 GHz		26		dB
	9 kHz to 8.0 GHz		22		dB
	9 kHz to 13.0 GHz		9		dB
Off State	9 kHz to 3.0 GHz		26		dB
	9 kHz to 8.0 GHz		14		dB
	9 kHz to 13.0 GHz		5		dB
RADIO FREQUENCY (RF) SETTLING TIME					
	50% V_{CTRL} to 0.05 dB margin of final RF_{OUT}		7.5		µs
	50% V_{CTRL} to 0.1 dB margin of final RF_{OUT}		6		µs
SWITCHING SPEED					
t_{RISE}/t_{FALL}	10%/90% RF		0.85		µs
t_{ON}/t_{OFF}	50% V_{CTRL} to 10%/90% RF		2.7		µs
INPUT POWER	1 MHz to 13.0 GHz				
1 dB Compression (P1dB)		35	37		dBm
0.1 dB Compression (P0.1dB)			35		dBm
INPUT THIRD-ORDER INTERCEPT (IIP3)	Two-tone input power = 14 dBm at each tone, 1 MHz to 13.0 GHz		62		dBm
RECOMMENDED OPERATING CONDITIONS[1]					
Positive Supply Voltage (V_{DD})		3.0		3.6	V
Negative Supply Voltage (V_{SS})		−2.75		−2.25	V
Control Voltage (V_{CTRL}) Range		0		V_{DD}	V
Logic Select (LS) Voltage Range		0		V_{DD}	V
RF Input Power	V_{DD}/V_{CTRL} = 3.3 V, V_{SS} = −2.5 V, T_A = 85°C, frequency = 2 GHz				
Through Path			35		dBm
Termination Path			27		dBm
Hot Switch Power Level	V_{DD} = 3.3 V, T_A = 85°C, frequency = 2 GHz		27		dBm
Case Temperature Range (T_{CASE})		−40		+85	°C

[1] These are the recommended values for these parameters.

DIGITAL CONTROL VOLTAGES

V_{DD} = 3.3 V ± 10%, V_{SS} = −2.5 V ± 10%, T_{CASE} = −40°C to +85°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition/Comments
INPUT CONTROL VOLTAGE						<1 µA typical
Low	V_{IL}	−0.3		+0.8	V	
High	V_{IH}	2.0		V_{DD} + 0.3	V	

BIAS AND SUPPLY CURRENT

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
SUPPLY CURRENT					
V_{DD} = 3.3 V	I_{DD}		20	200	µA
V_{SS} = −2.5 V	I_{SS}		0.5	10	µA

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Positive Supply Voltage (V_{DD}) Range	−0.3 V to +3.7 V dc
Negative Supply Voltage (V_{SS}) Range	−2.8 V to +0.3 V
Control Voltage (V_{CTRL}) Range	−0.3 V to V_{DD} + 0.3 V
Logic Select (LS) Voltage Range	−0.3 V to V_{DD} + 0.3 V
RF Input Power[1] (V_{DD}/V_{CTRL} = 3.3 V, V_{SS} = −2.5 V, T_A = 85°C, Frequency = 2 GHz)	See Figure 2 to Figure 4
Through Path	37 dBm
Termination Path	28 dBm
Hot Switch Power Level (V_{DD} = 3.3 V, T_A = 85°C, Frequency = 2 GHz)	30 dBm
Storage Temperature Range	−65°C to +150°C
Maximum Reflow Temperature (MSL3 Rating)	260°C
Channel Temperature	135°C
Thermal Resistance (Channel to Package Bottom)	
Through Path	116°C/W
Terminated Path	100°C/W
ESD Sensitivity (HBM), Class 2	2 kV

[1] For recommended operating conditions, see Table 1.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

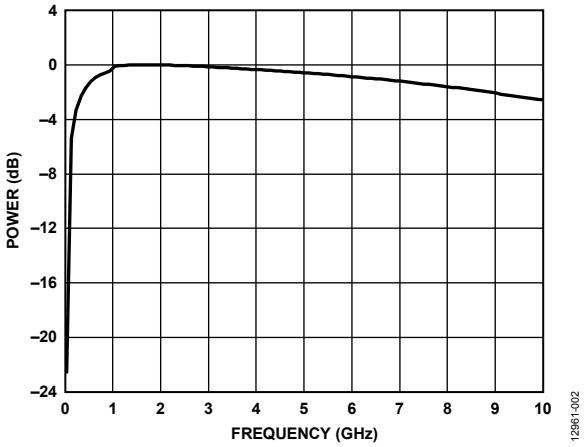

Figure 2. Power Derating Through Path

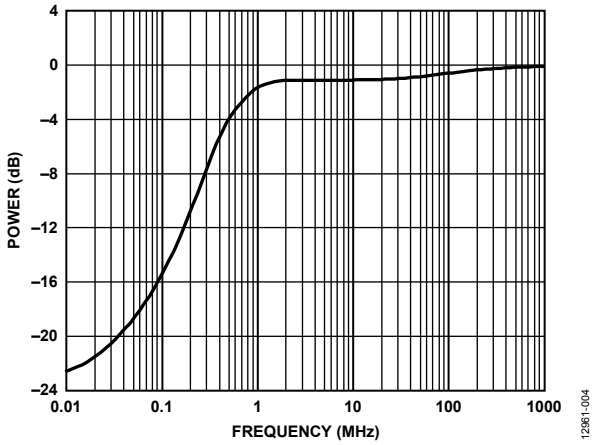

Figure 3. Power Derating Through Path (Low Frequency Detail)

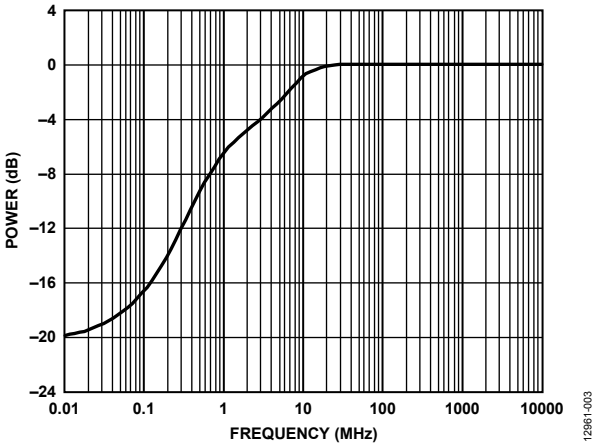

Figure 4. Power Derating for Hot Switching Power

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

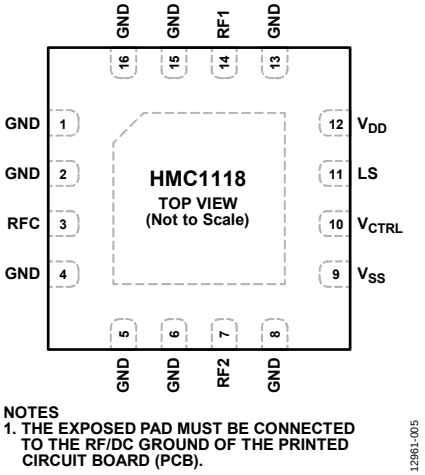

Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4 to 6, 8, 13, 15, 16	GND	Ground. The package bottom has an exposed metal pad that must connect to the printed circuit board (PCB) RF/dc ground. See Figure 6 for the GND interface schematic.
3	RFC	RF Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc.
7	RF2	RF2 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc.
14	RF1	RF1 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc.
9	V_{SS}	Negative Supply Voltage Pin.
10	V_{CTRL}	Control Input Pin. See Table 1, Table 2, and Table 6.
11	LS	Logic Select Input Pin. See Table 1, Table 2, and Table 6.
12	V_{DD}	Positive Supply Voltage Pin.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/dc ground of the printed circuit board (PCB).

Table 6. Truth Table

Control Input		Signal Path State	
LS	**V_{CTRL}**	**RFC to RF1**	**RFC to RF2**
High	Low	On	Off
High	High	Off	On
Low	Low	Off	On
Low	High	On	Off

INTERFACE SCHEMATICS

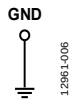

Figure 6. GND Interface Schematic

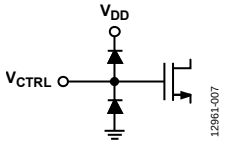

Figure 7. V_{CTRL} Interface Schematic

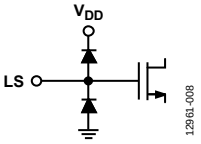

Figure 8. LS Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

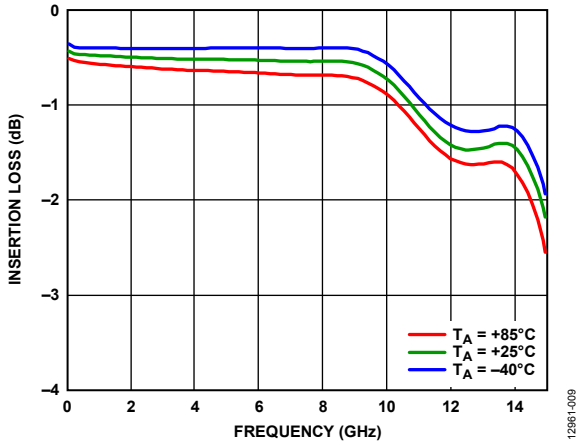

Figure 9. Insertion Loss vs. Frequency

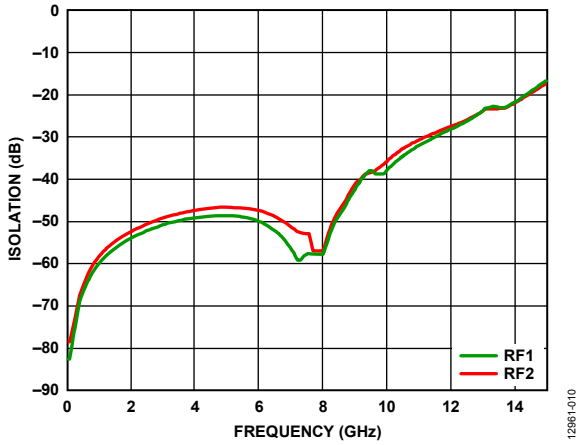

Figure 11. Isolation Between RFC and the RF1 and RF2 Ports vs. Frequency

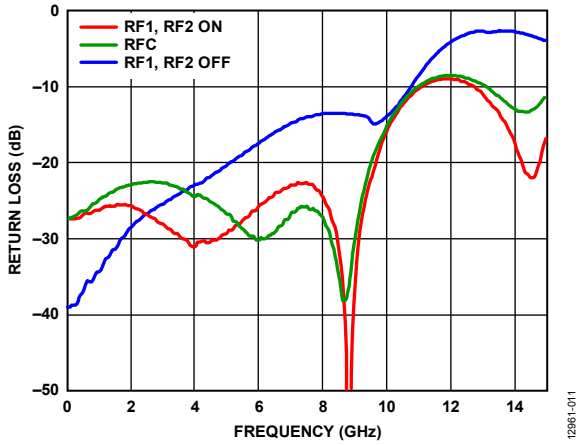

Figure 10. Return Loss vs. Frequency

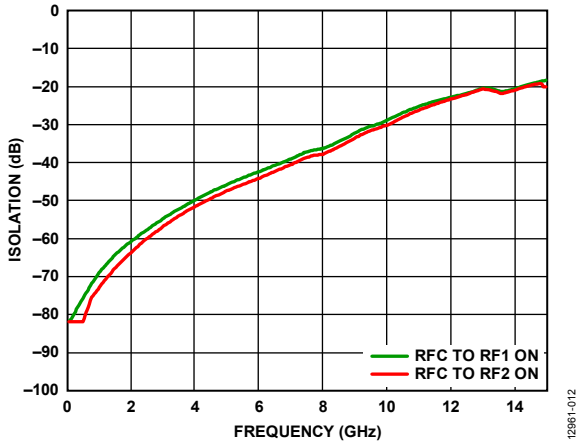

Figure 12. Isolation Between RF1 and RF2 Ports vs. Frequency

INPUT COMPRESSION POINT AND INPUT THIRD-ORDER INTERCEPT

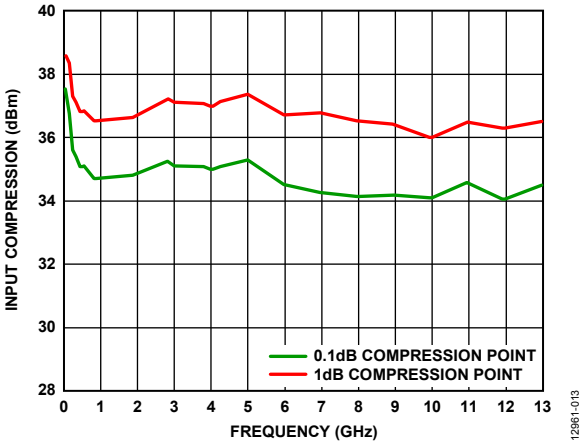

Figure 13. 0.1 dB and 1 dB Compression Point vs. Frequency

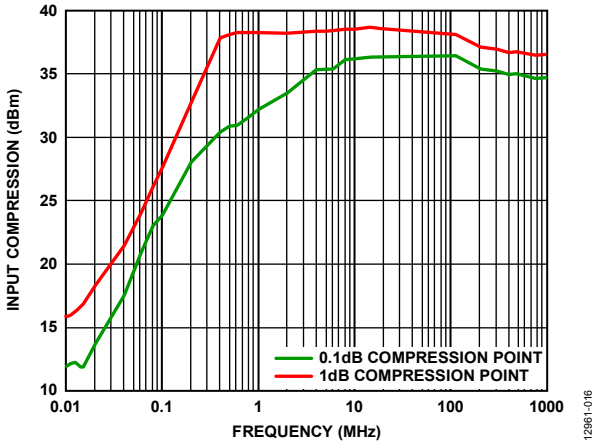

Figure 16. 0.1 dB and 1 dB Input Compression Point vs. Frequency (Low Frequency Detail)

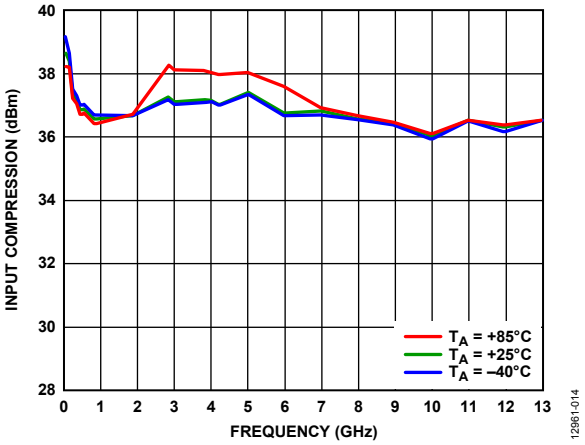

Figure 14. 1 dB Input Compression Point vs. Frequency over Temperature

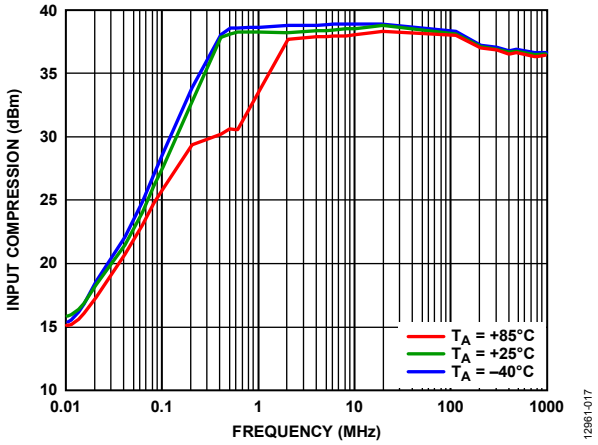

Figure 17. 1 dB Input Compression Point vs. Frequency over Temperature (Low Frequency Detail)

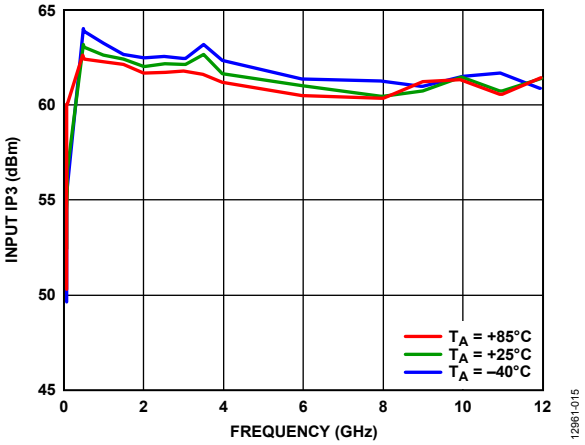

Figure 15. Input Third-Order Intercept (IIP3) Point vs. Frequency over Temperature

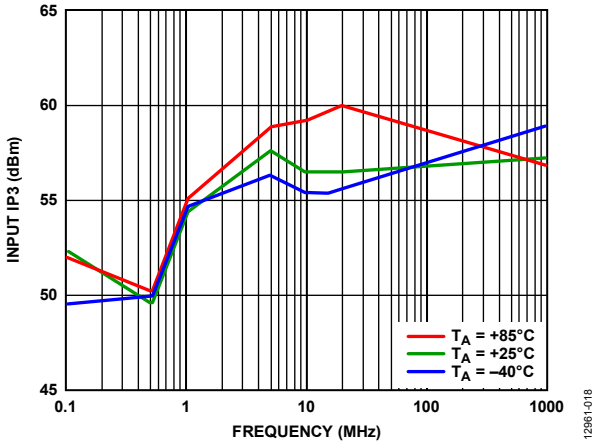

Figure 18. Input Third-Order Intercept (IIP3) Point vs. Frequency over Temperature (Low Frequency Detail)

THEORY OF OPERATION

The HMC1118 requires a positive supply voltage applied to the V_{DD} pin and a negative supply voltage applied to the V_{SS} pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling. The HMC1118 can operate with a single positive supply voltage applied to the V_{DD} pin and the negative voltage input pin (V_{SS}) connected to ground; however, some performance degradations in the input power compression and third-order intercept can occur.

The HMC1118 is controlled via two digital control voltages applied to the V_{CTRL} pin and the LS pin. A small value bypassing capacitor is recommended on these digital signal lines to improve the RF signal isolation.

The HMC1118 is internally matched to 50 Ω at the RF input port (RFC) and the RF output ports (RF1 and RF2); therefore, no external matching components are required. The RF1 and RF2 pins are dc-coupled, and dc blocking capacitors are required on the RF paths if the RF potential is not equal to a common-mode voltage of 0 V. The design is bidirectional; the input and outputs are interchangeable.

The ideal power-up sequence is as follows:

1. Power up GND.
2. Power up V_{DD} and V_{SS}. The relative order is not important.
3. Power up the digital control inputs. The relative order of the logic control inputs is not important. Powering the digital control inputs before the V_{DD} supply can inadvertently forward bias and damage the internal ESD protection structures.
4. Power up the RF input.

The logic select (LS) allows the user to define the control input logic sequence for the RF path selections. With the LS pin set to logic high, the RFC to RF1 path turns on when V_{CTRL} is logic low, and the RFC to RF2 path turns on when V_{CTRL} is logic high. With LS set to logic low, the RFC to RF1 path turns on when V_{CTRL} is logic high, and the RFC to RF2 path turns on when V_{CTRL} is logic low.

Depending on the logic level applied to the LS and V_{CTRL} pins, one RF output port (for example, RF1) is set to on mode, by which an insertion loss path provides the input to the output. The other RF output port (for example, RF2) is then set to off mode, by which the output is isolated from the input. When the RF output port (RF1 or RF2) is in isolation mode, internally terminate it to 50 Ω, and the port absorbs the applied RF signal (see Table 7).

Table 7. Switch Mode Operation

Digital Control Inputs		Signal Mode	
LS	**V_{CTRL}**	**RFC to RF1**	**RFC to RF2**
High	Low	On mode. A low insertion loss path from the RFC port to the RF1 port.	Off mode. The RF2 port is isolation from the RFC port and internally terminated to a 50 Ω load to absorb the applied RF signals.
High	High	Off mode. The RF1 port is isolation from the RFC port and internally terminated to a 50 Ω load to absorb the applied RF signals.	On mode. A low insertion loss path from the RFC port to the RF2 port.
Low	Low	Off mode. The RF1 port is isolation from the RFC port and internally terminated to a 50 Ω load to absorb the applied RF signals.	On mode. A low insertion loss path from the RFC port to the RF2 port.
Low	High	On mode. A low insertion loss path from the RFC port to the RF1 port.	Off mode. The RF2 port is isolation from the RFC port and internally terminated to a 50 Ω load to absorb the applied RF signals.

APPLICATIONS INFORMATION

EVALUATION PCB

Generate the evaluation PCB used in this application with proper RF circuit design techniques. Signal lines at the RF port must have 50 Ω impedance, and the package ground leads and backside ground slug must be connected directly to the ground plane similarly to what is shown in Figure 19. The evaluation board shown in Figure 19 is available from Analog Devices, Inc. upon request.

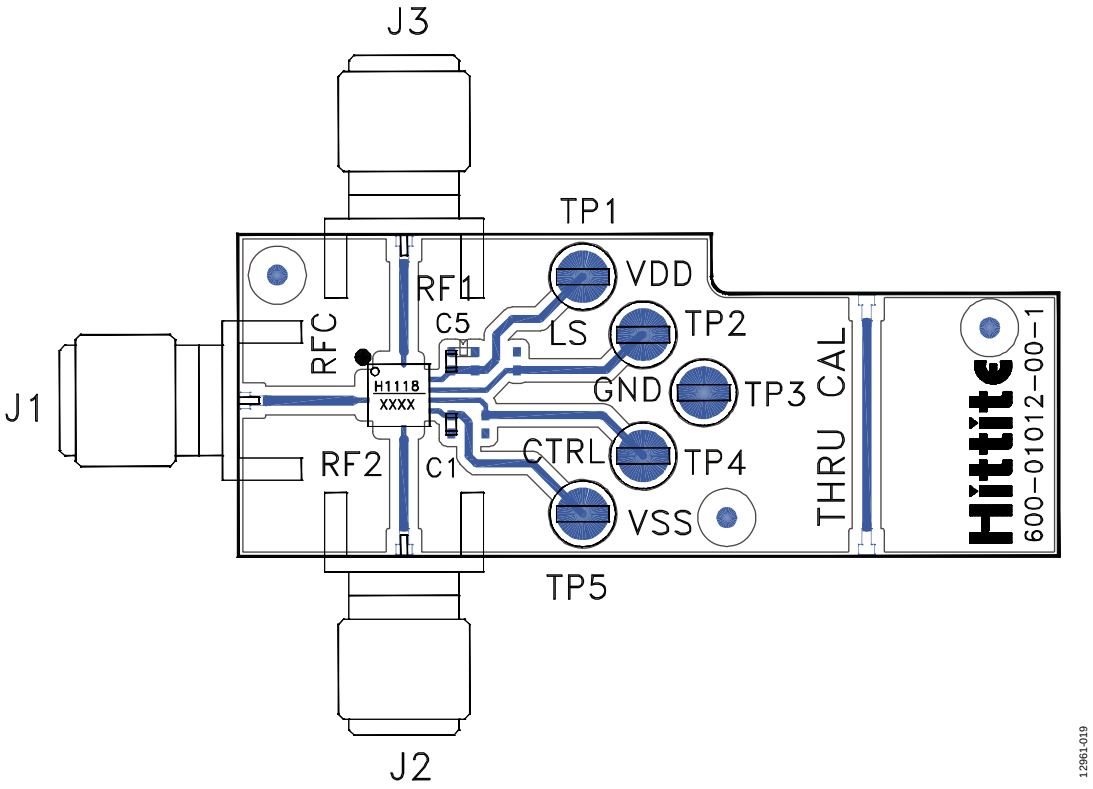

Figure 19. EV1HMC1118LP3D Evaluation PCB

Table 8. Bill of Materials for the EV1HMC1118LP3D Evaluation Board[1]

Item	Description	Manufacturer[2]
J1 to J3	PC mount SMA RF connectors	
TP1 to TP5	Through-hole hold mount test points	
C1, C5	100 pF capacitors, 0402 package	
U1	HMC1118 SPDT switch	Analog Devices, Inc.
PCB	600-01012-00-1 evaluation PCB, Rogers 4350 circuit board material	EV1HMC1118LP3D, Analog Devices, Inc.[1]

[1] Reference this number to order the full evaluation PCB.
[2] The blank cells in the manufacturer column are left blank intentionally for they are user-selectable.

OUTLINE DIMENSIONS

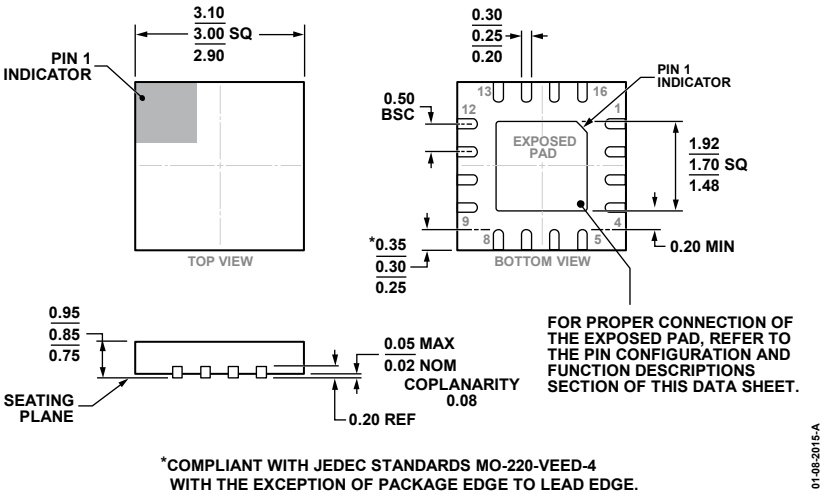

Figure 20. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.85 mm Package Height
(CP-16-38)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option
HMC1118LP3DE	−40°C to +85°C	MSL3	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-38
HMC1118LP3DETR	−40°C to +85°C	MSL3	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-38
EV1HMC1118LP3D			Evaluation Board	

[1] HMC1118LP3DE and HMC1118LP3DETR are RoHS-Compliant Parts.
[2] See the Absolute Maximum Ratings section.