# LT8698S/LT8698S-1
# 5V 3A, 42V Input USB Charger with Cable Drop Compensation and Data Line Protection

## DESCRIPTION

Demonstration circuit 2688A is a USB charger designed to power the 5V USB $V_{BUS}$ rail with up to 3A from an input voltage as high as 42V. The DC2688A circuit features the LT®8698S/LT8698S-1, which is a compact, high efficiency, high speed synchronous monolithic step-down switching regulator which features the second-generation Silent Switcher® technology that minimizes EMI and reduces PCB layout sensitivity. The LT8698S/LT8698S-1 supports a wide variety of portable device charger profiles including USB BC 1.2 CDP, DCP, and SDP as well as common proprietary charger profiles, all of which can be easily evaluated using the DC2688A demo board. The LT8698S/LT8698S-1 also features high speed USB 2.0 compliant data line switches, robust data line protection, and programmable cable drop compensation which maintains accurate 5V $V_{BUS}$ regulation even when USB sockets are separated from the LT8698S/LT8698S-1 by a long cable. These features make the LT8698S/LT8698S-1 well suited for automotive USB host applications.

There are two assembly versions. The DC2688A-A features the LT8698S, while the DC2688A-B features the LT8698S-1. The difference is that the LT8698S includes $V_{IN}$ hot loop capacitors inside the IC package for improved EMI/EMC performance, while the LT8698S-1 does not include these capacitors.

### DEMO BOARD INFORMATION

The main power stage of the DC2688A demo board operates at 2MHz switching frequency by default to minimize solution size. The jumper JP5 on the demo board determines the configuration of the SYNC pin of the LT8698S/LT8698S-1. Setting the jumper JP5 to "FCM W/SSM" location ties SYNC pin to $INTV_{CC}$ which enables forced continuous mode with spread-spectrum modulation for improved EMI performance. Moving JP5 to "PSK" location enables the pulse-skipping mode which improves light load efficiency by reducing the switching frequency at light load and reducing $V_{IN}$ quiescent current between pulses. To synchronize to an external clock, move JP5 to "FCM W/O SSM or SYNC" location and apply external clock on the EXT_SYNC turret.

Figure 1 shows a functional Block Diagram of the DC2688A demo board.

The DC2688A demo board includes a re-timer IC USB2422 whose purpose is to ensure that USB high speed signaling eye pattern can be measured at test plane 2 as defined by USB 2.0 specifications, and that such signaling through the LT8698S/LT8698S-1's USB data line switches conforms to template 1 eye pattern requirements. Please note that a re-timer IC is not necessary in actual applications as the USB host controller will reside on the same PCB board as the LT8698S/LT8698S-1.

The DC2688A demo board includes three headers JP2, JP3, and JP4, which are used for manual control of the LT8698S/LT8698S-1's tristate input pins SEL1, SEL2, and SEL3. Although these select pins are intended to interface with a USB host microcontroller, majority of the functions of the LT8698S/LT8698S-1 may be evaluated by simply using the manual selection of the SEL1, SEL2, and SEL3 headers on the DC2688A board.

The DC2688A demo board is 3.5-inch × 3.5-inch in size and has four copper layers with 2oz copper on the outer layers and 1oz copper on the inner layers. The DC2688A has controlled impedance transmission lines placed for high speed differential USB data signaling, in between the USB-B receptacle, the USB2422 re-timer IC, the LT8698S/LT8698S-1 data line switches, and the USB-A receptacle, with a differential characteristic impedance of 90Ω.

The default rated maximum load current of the DC2688A is 2.4A, with a default $R_{SENSE}$ resistor value of 10mΩ. However, the DC2688A circuit can supply 3A load current with a $R_{SENSE}$ resistor value of 8mΩ.

**Design files for this circuit board are available.**

## DESCRIPTION

Figure 2 shows the efficiency of the DC2688A at 12V and 24V input in pulse-skipping mode of operation (input from $V_{IN}$ turret pin, and $R_{SENSE}$ resistor is 8mΩ)

The DC2688A has an input EMI filter installed. The EMI performance of the demo board DC2688A-A (with EMI filter) is shown in Figure 3 and Figure 4. The red lines in Figure 3 are CISPR 25 class 5 limits for peak detector. The EMI performance of DC2688A-B (with EMI filter) is shown in Figure 5 and Figure 6. To achieve EMI performance as shown in Figure 3 through Figure 6, the input EMI filter is required, and the input voltage should be applied at $V_{EMI}$ terminal.

As shown in the dashed box in Figure 1 functional block diagram, the DC2688A demo board may also be optionally used in conjunction with the Linduino® microcontroller board DC2026C and a touchscreen display shield. The DC2688A demo board includes the AD5593R, which is an 8-channel ADC/GPIO with on-chip reference and $I^2C$ interface. The AD5593R monitors several inputs from the LT8698S/LT8698S-1, communicates with the Linduino board through the $I^2C$ interface, and controls the SEL1, SEL2, and SEL3 tristate input pins.

The LT8698S/LT8698S-1 data sheet gives a complete description of the part, operation and application information. The data sheet must be read in conjunction with this manual for DC2688A.

## DESCRIPTION

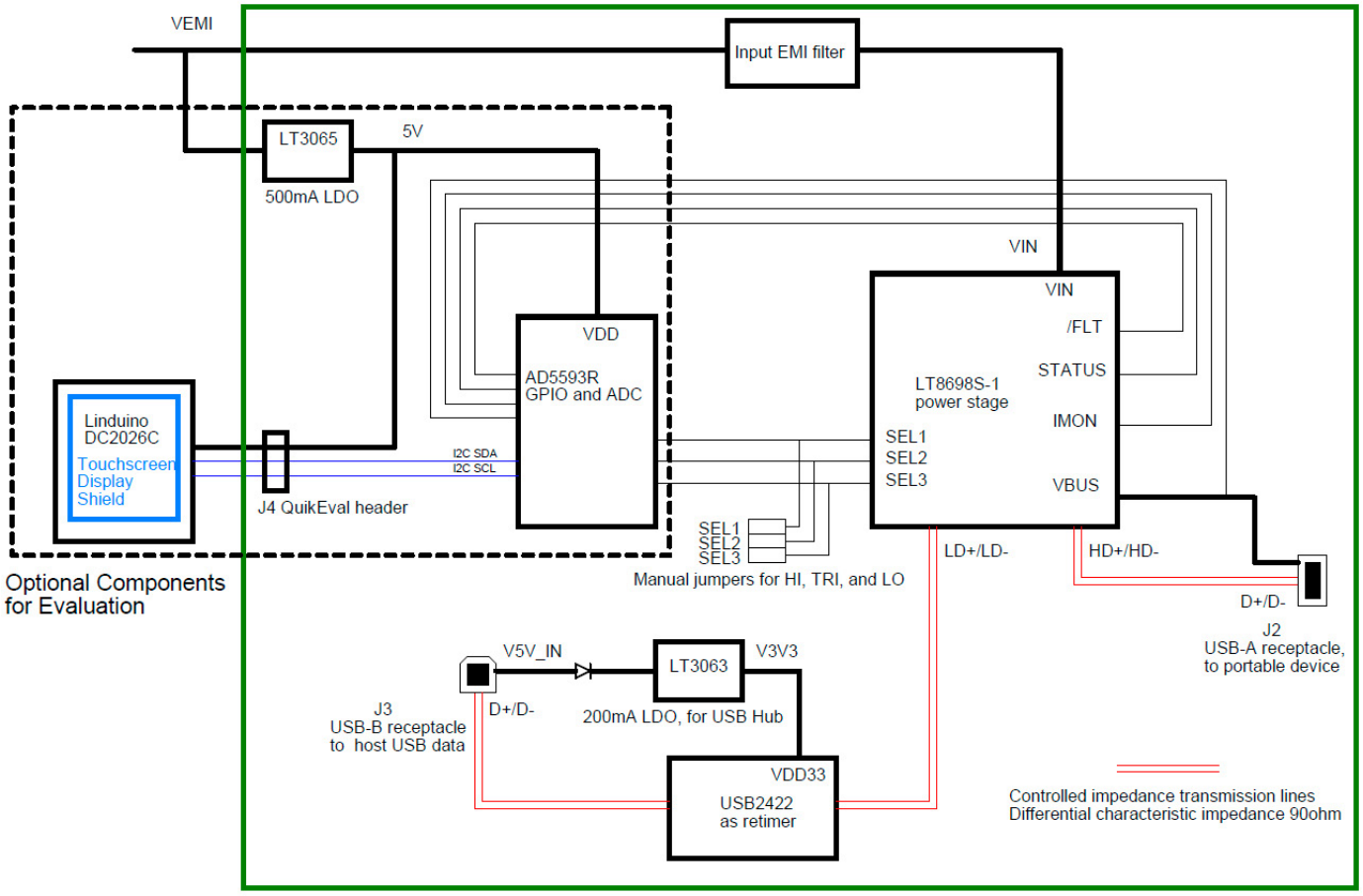



**Figure 1. DC2688A Demo Board Functional Block Diagram**

## PERFORMANCE SUMMARY

**Specifications are at $T_A$ = 25°C**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input Supply Range | | 6.0 | | 42 | V |
| $V_{BUS}$ | USB 5V Bus Voltage | Without Cable Drop Compensation | 4.8 | 5 | 5.2 | V |
| | USB 5V Bus Voltage | With Cable Drop Compensation | | | 6.2 | V |
| $I_{BUS}$ | Maximum Output Current | $R_{SENSE}$ = 10mΩ | 2.4 | | | A |
| | Maximum Output Current | $R_{SENSE}$ = 8mΩ | 3.0 | | | A |
| $f_{SW}$ | Switching Frequency | | 1.95 | 2 | 2.05 | MHz |
| EFE | Efficiency at DC | $V_{IN}$ = 12V, $I_{BUS1}$ = 1.5A | | 92.7 | | % |

## TYPICAL PERFORMANCE CHARACTERISTICS

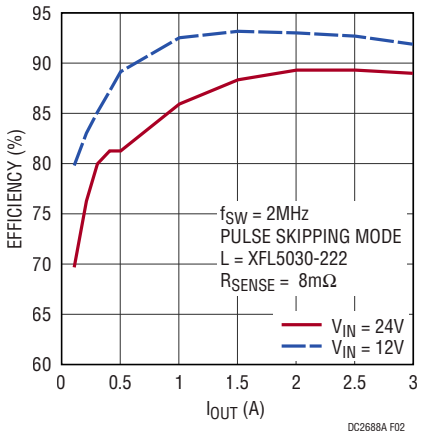
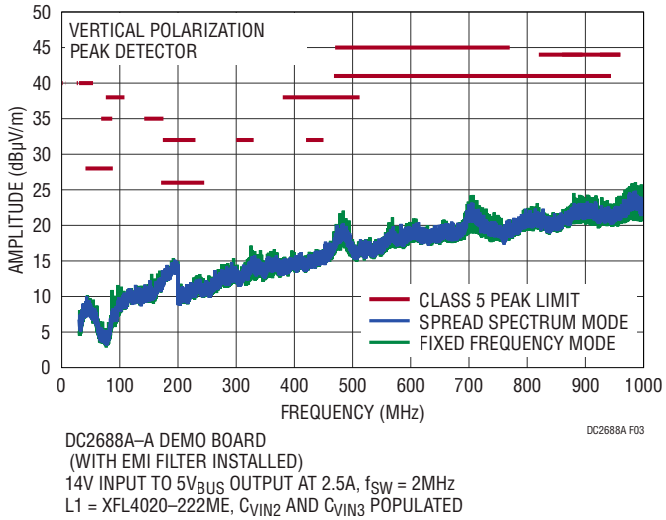


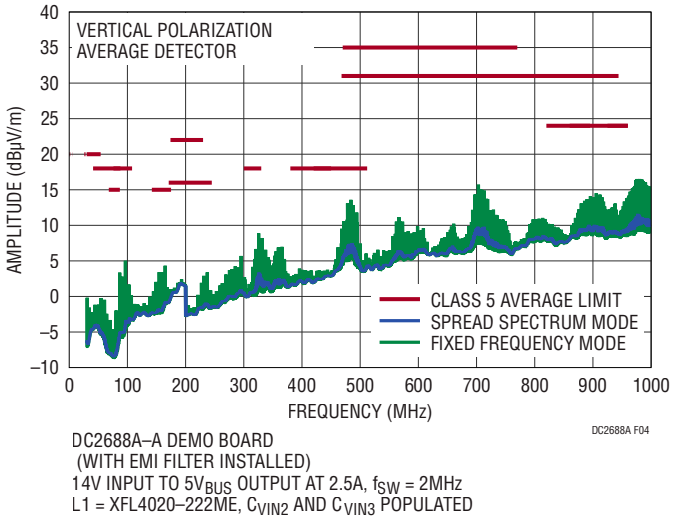

**Figure 2. Efficiency vs Load Current at 2MHz Switching Frequency (Input from $V_{IN}$ Terminal)**

## TYPICAL PERFORMANCE CHARACTERISTICS



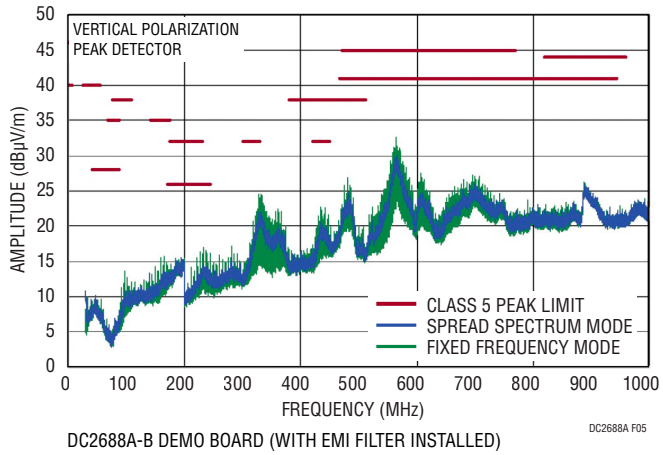

DC2688A–A DEMO BOARD
(WITH EMI FILTER INSTALLED)
14V INPUT TO $5V_{BUS}$ OUTPUT AT 2.5A, $f_{SW}$ = 2MHz
L1 = XFL4020–222ME, $C_{VIN2}$ AND $C_{VIN3}$ POPULATED

**Figure 3. DC2688A-A Demo Circuit EMI Performance in CISPR 25 Radiated Emissions Test, Peak Detector**



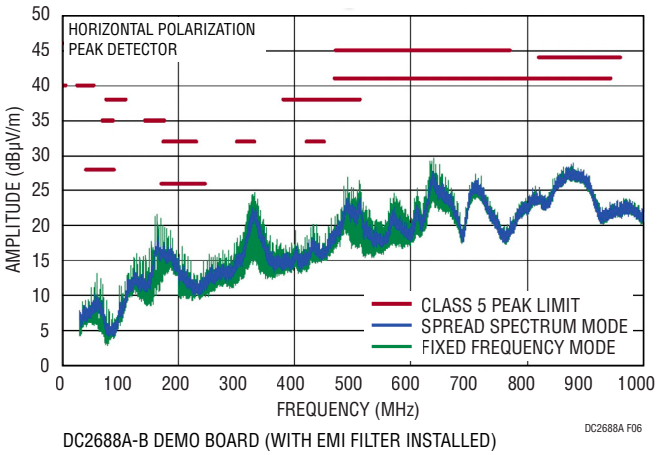

DC2688A–A DEMO BOARD
(WITH EMI FILTER INSTALLED)
14V INPUT TO $5V_{BUS}$ OUTPUT AT 2.5A, $f_{SW}$ = 2MHz
L1 = XFL4020–222ME, $C_{VIN2}$ AND $C_{VIN3}$ POPULATED

**Figure 4. DC2688A-A Demo Circuit EMI Performance in CISPR 25 Radiated Emissions Test, Average Detector**




DC2688A-B DEMO BOARD (WITH EMI FILTER INSTALLED)
14V INPUT TO 5V $V_{BUS}$ AT 2.5A, $f_{SW}$ = 2MHz, L1 = XFL4020-222ME,
$CV_{IN2}$ AND $CV_{IN3}$ POPULATED

**Figure 5. DC2688A-B Demo Circuit EMI Performance in CISPR 25 Radiated Emissions Test, Vertical Polarization**




DC2688A-B DEMO BOARD (WITH EMI FILTER INSTALLED)
14V INPUT TO 5V $V_{BUS}$ AT 2.5A, $f_{SW}$ = 2MHz, L1 = XFL4020-222ME,
$CV_{IN2}$ AND $CV_{IN3}$ POPULATED

**Figure 6. DC2688A-B Demo Circuit EMI Performance in CISPR 25 Radiated Emissions Test, Horizontal Polarization**

## QUICK START PROCEDURE

### EVALUATE DC2688A POWER STAGE

Demonstration circuit 2688A is easy to set up to evaluate the performance of the LT8698S/LT8698S-1. Refer to Figure 7 for proper measurement equipment setup and follow the procedure below.

**NOTE:** When measuring the input or output voltage ripple, care must be taken to avoid long ground lead on the oscilloscope probe. Measure the output voltage ripple by touching the probe tip directly across the $VB_{US}$ and GND terminals. See Figure 7 and Figure 8 for proper measurement technique.

1. Check that JP6 and JP7 are placed on the OFF position to ensure that the on-board LDOs are disabled.
2. Place JP2, JP3, and JP4 all on the "Z" position, which puts the LT8698S/LT8698S-1 in $V_{BUS}$ only mode of operation with $V_{BUS}$ in regulation.
3. With power off, connect the input power supply to $V_{EMI}$ and GND turrets. If the EMI/EMC performance is not important, connect the input power supply to $V_{IN}$ and GND turrets.
4. With power off, connect the loads from $V_{BUS}$ to GND.
5. Check that JP1 EN jumper is placed on the ON position.
6. Turn on the power at the input.

   **NOTE:** Make sure that the input voltage never exceeds 42V.
7. Check for proper output voltages: $V_{BUS}$ voltage should be between 5V to 6.1V and depends on the cable drop compensation settings, and D11 LED indicator lights up in green. For more information on cable drop compensation, please refer to LT8698S/LT8698S-1 data sheet.

   **NOTE:** If there is no output, temporarily disconnect the load to make sure that the load is not set too high.
8. Once the proper output voltages are established, adjust the load within the operating ranges and observe the output voltage regulation, ripple voltage, efficiency and other parameters.
9. An external clock can be added to the EXT_SYNC terminal when SYNC function is used (JP5 on the FCM W/O SSM OR SYNC position). Please make sure that R37 resistor should be chosen to set the LT8698S/LT8698S-1 switching frequency equal to or below the lowest synchronization frequency. JP5 can also set the LT8698S/LT8698S-1 in spread-spectrum mode (JP5 on the FCM W/SSM position) or pulse skipping mode (JP5 on the PSK position).
10. Check STATUS pin voltage on the STATUS turret in relation to the $I_{BUS}$ load current. If $I_{BUS}$ load is lower than 100mA typically, STATUS pin should be low, and the STATUS LED lights up in yellow; if $I_{BUS}$ load is higher than 130mA typically, STATUS pin should be high, and the STATUS LED does not light up.
11. Check $I_{MON}$ point voltage, in relation to $I_{BUS}$ load current. Measure the voltage on the IMON turret: the IMON voltage should be equal to 0.46V/A in proportion to the $I_{BUS}$ load current.

## QUICK START PROCEDURE

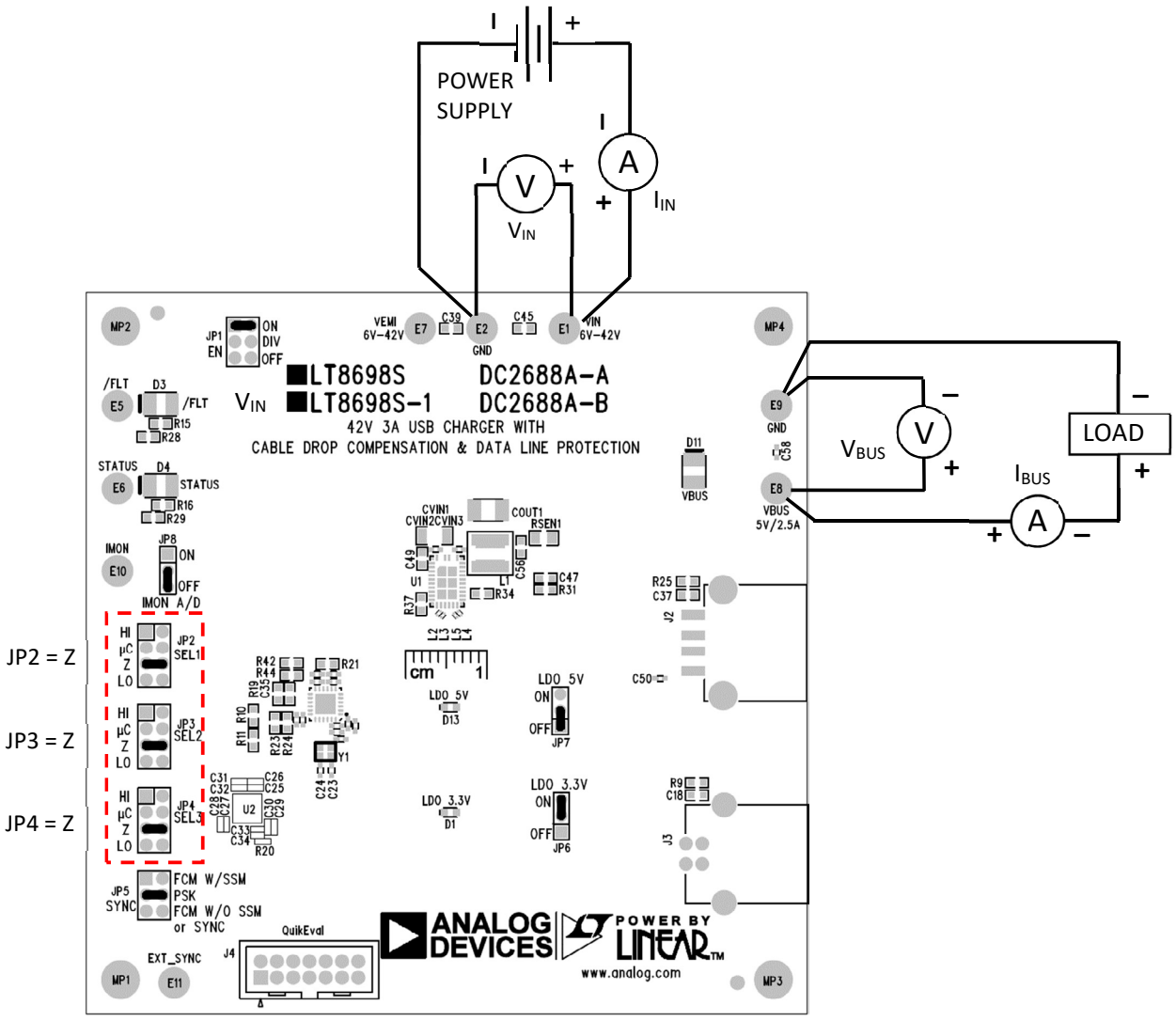



**Figure 7. Proper Measurement Equipment Setup for Evaluating the DC2688A-B Power Stage**

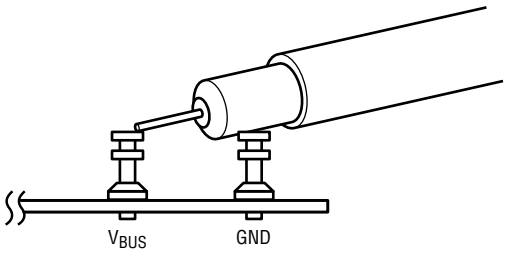



**Figure 8. Measuring Output Ripple**

# QUICK START PROCEDURE

## EVALUATE USB CHARGER PROFILES

The LT8698S/LT8698S-1 supports several common USB charger profiles, and the DC2688A demo board is easy to set up to evaluate these common charger profiles.

Refer to Figure 9 for proper measurement equipment setup and follow the procedure below.

1. Check that JP6 and JP7 are placed on the OFF position, to ensure that the on-board LDOs are disabled.
2. Select JP2, JP3, and JP4 jumpers at appropriate locations based on the desired charger profile and SEL pin lookup table in the LT8698S/LT8698S-1 data sheet. Table 1 shows several popular USB charger profiles available in the LT8698S/LT8698S-1. Refer to LT8698S/LT8698S-1 data sheet for further information about USB charger profiles.
3. With power off, connect the input power supply to $V_{EMI}$ and GND turrets. If the EMI/EMC performance is not important, connect the input power supply to VIN and GND turrets.
4. Check that JP1 EN jumper is placed on the ON position.
5. Turn on the power at the input.

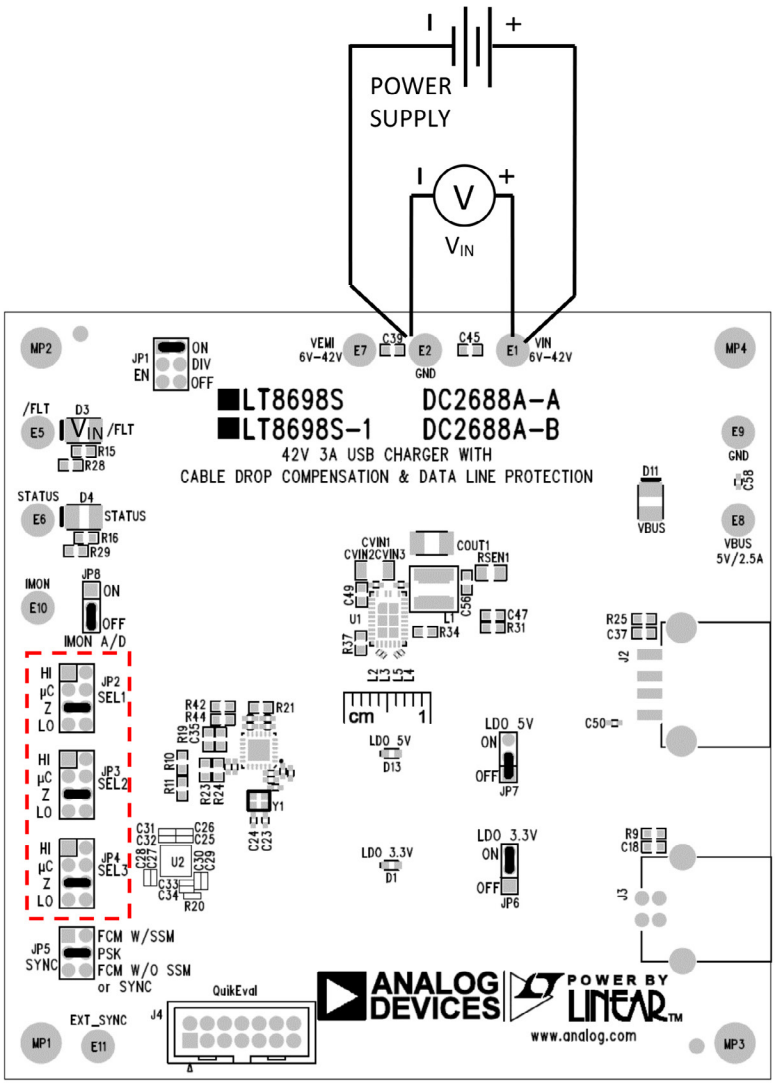
   **NOTE:** Make sure that the input voltage never exceeds 42V.
6. Check for proper output voltages: $V_{BUS}$ = 5V, and D11 LED indicator lights up in green.
7. Attach a portable device to the type A socket of the DC2688A demo board.
8. Observe the battery charging activity on the portable device.
9. Observe charging current by measuring the voltage on IMON turret: the IMON voltage should be equal to 0.46V/A in proportion to the $I_{BUS}$ load current.

**Table 1. Common USB Charger Profiles and Corresponding SEL Pins**

| | SEL1 | SEL2 | SEL3 | CHARGER PROFILE DESCRIPTION |
|---|---|---|---|---|
| State 21 | LOW | TRI | HIGH | USB BC 1.2 DCP Profile |
| State 22 | TRI | TRI | HIGH | 2.0A Vendor Charger Profile |
| State 24 | LOW | HIGH | HIGH | 2.4A Vendor Charger Profile |

## QUICK START PROCEDURE

JP2, JP3 AND JP4 JUMPERS SET TO A CHARGER STATE BASED ON SEL PIN LOOKUP TABLE IN LT8698S DATASHEET




TYPE A CONNECTOR CABLE

USB TO PORTABLE DEVICE

**Figure 9. Proper Measurement Equipment Setup for Evaluating Common USB Charger Profiles**

## QUICK START PROCEDURE

### EVALUATE USB BC 1.2 CDP APPLICATIONS

The LT8698S/LT8698S-1 integrates necessary hardware to support USB BC 1.2 Charging Downstream Port (CDP) charger profile which allows compliant devices to draw high current of up to 1.5A from $V_{BUS}$ while simultaneously communicating with the host at USB high speed of 480Mbps.

Refer to Figure 10 for proper measurement equipment setup and follow the procedure below.

1. Check that JP6 is placed on the ON position to ensure that the 3.3V LDO is enabled.
2. Select JP2 and JP3 to be in the LOW position and select JP4 to be in the LOW or TRI position. Select JP4 SEL3 in the LOW position sets the LT8698S/LT8698S-1 in select state 0 which performs the CDP sequence with the data line switches closed and without termination. Select JP4 SEL3 in the TRI position sets the LT8698S/LT8698S-1 in select state 1 which performs the CDP sequence with the data line switches open and 20k termination resistors tied from HD+ and HD– to GND. Both select 0 and select 1 are valid state in which to start the CDP sequence. For further information about the CDP sequence, please refer to the LT8698S/LT8698S-1 data sheet.
3. With power off, connect the input power supply to $V_{EMI}$ and GND turrets. If the EMI/EMC performance is not important, connect the input power supply to $V_{IN}$ and GND turrets.
4. Check that JP1 EN jumper is placed on the ON position.
5. Turn on the power at the input.

   **NOTE:** Make sure that the input voltage never exceeds 42V.
6. Check for proper output voltages: $V_{BUS}$ = 5V, and D11 LED indicator lights up in green.
7. Plug a USB cable connecting to a PC with type B connector to the type B socket of the DC2688A demo board and connect the USB cable to a computer.
8. Check the STATUS pin voltage and observe STATUS yellow LED is on, meaning STATUS pin is low. At this point, the LT8698S/LT8698S-1 puts a 100µA current source on the D+, asserts STATUS low and waits for a portable device to attach to the USB socket.
9. Attach a CDP compliant portable device to the type A socket of the DC2688A demo board.
10. Observe the CDP negotiation between the portable device and the computer. You may monitor the voltage waveforms on STATUS, $V_{BUS}$, IMON point, D+, and D– during this CDP negotiation. Observe the USB data connection between portable device and the PC as manifested by the portable device showing up in the PC in “devices and driver” or “this PC”, and the PC may be able to access data stored in the portable device.
11. To restart another CDP session, perform the following steps:
    a. Unplug the portable device from the type A socket.
    b. Place the JP1 EN jumper to OFF position and then place it back to ON position. Cycling the EN/UV pin of the LT8698S/LT8698S-1 resets the CDP state machine which is necessary in order to restart another CPD sequence. Alternatively, the CDP state machine can be reset by setting LT868S to a non-CDP state (any select state other than state 0, state 1, and state 2) and coming back to state 0 or state 1. Note: in an actual CDP application, a USB host microcontroller can detect a portable device detach and reset the DP machine by controlling the SEL pin(s).
    c. Repeat from step 8.

## QUICK START PROCEDURE

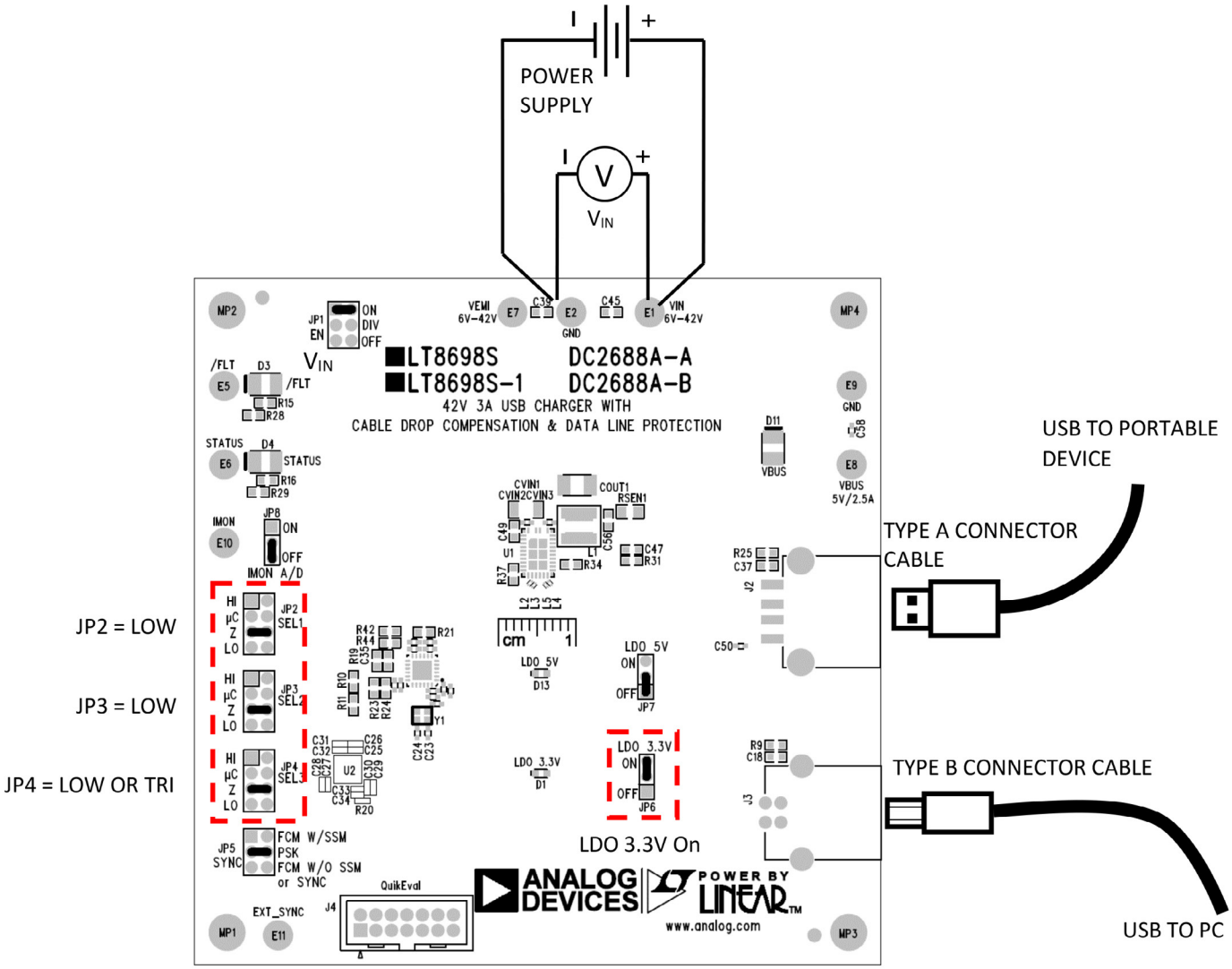



**Figure 10. Proper Measurement Equipment Setup for Evaluating USB CDP Charger Profiles**

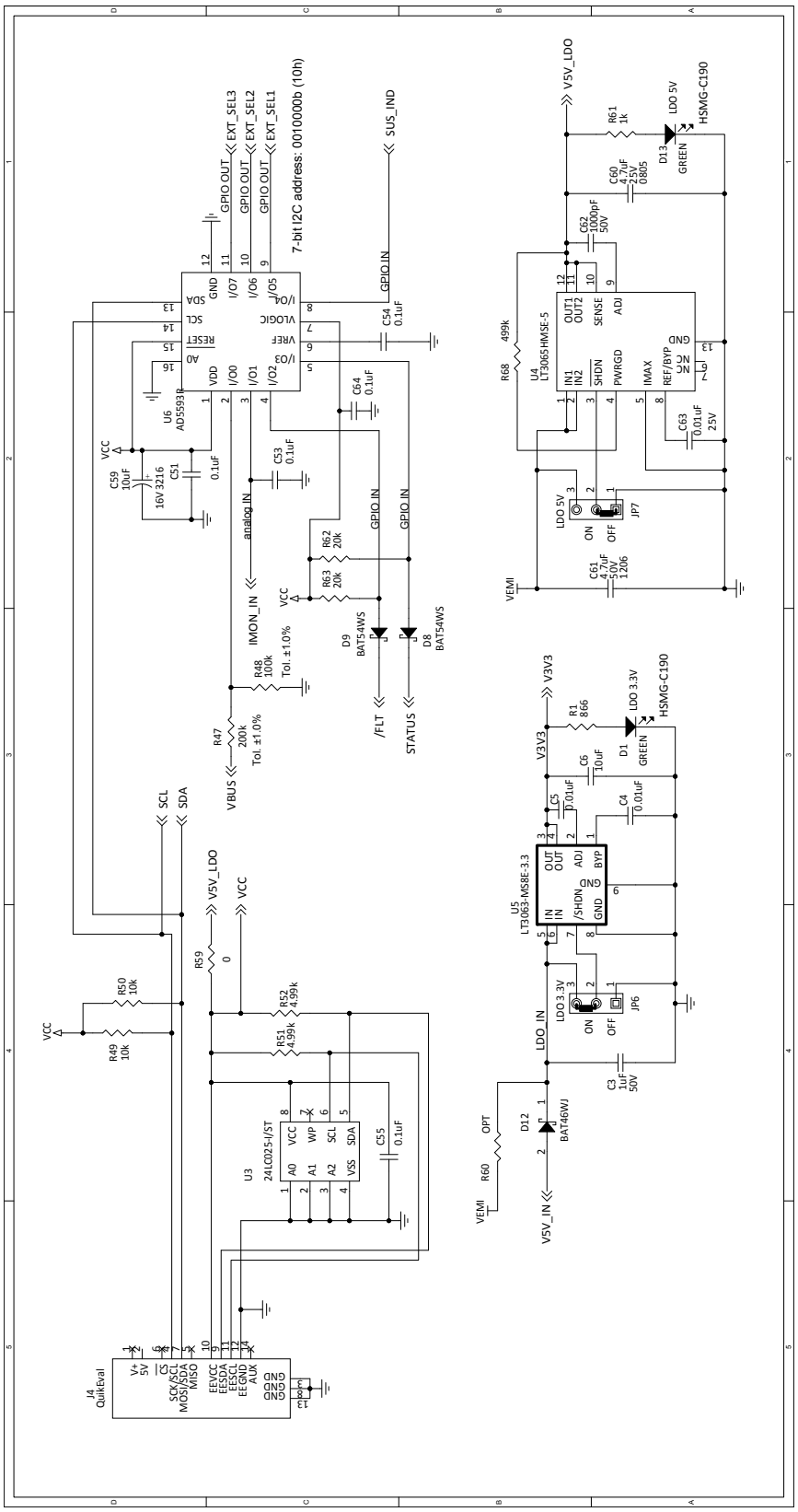
## PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
|---|---|---|---|---|
| **Required Circuit Components** | | | | |
| 1 | 3 | C3, C39, C45 | CAP., 1µF, X5R, 50V, 10%, 0603 | TDK, CGA3E3X5R1H105K080AB |
| 2 | 3 | C4, C5, C63 | CAP., 0.01µF, X5R, 25V, 10%, 0603 | TDK, C1608X7R1E103K080AA |
| 3 | 1 | C6 | CAP., 10µF, X5R, 10V, 10%, 0805 | MURATA, GRM21BR61A106KE19L |
| 4 | 8 | C18, C35, C37, C51, C53, C54, C55, C64 | CAP., 0.1µF, X7R, 25V, 10%, 0603 | TDK, C1608X7R1E104K080AA |
| 5 | 1 | C19 | CAP., 2.2µF, X5R, 25V, 10%, 0603 | MURATA, GRM188R61E225KA12D |
| 6 | 1 | C22 | CAP., 100µF, ALUM. ELECT., 25V, 20%, 6.3mm × 7.7mm SMD, D8 | PANASONIC, EEHZA1E101XP |
| 7 | 2 | C23, C24 | CAP., 18pF, NP0, 25V, 10%, 0402 | AVX, 04023A180KAT2A |
| 8 | 5 | C25, C27, C29, C32, C34 | CAP., 1000pF, X7R, 25V, 10%, 0402 | AVX, 04023C102KAT2A |
| 9 | 2 | C26, C31 | CAP., 1µF, X5R, 16V, 10%, 0402 | TDK, C1005X5R1C105K050BC |
| 10 | 5 | C28, C30, C33, C48, C50 | CAP., 0.1µF, X5R, 25V, 10%, 0402 | AVX, 04023D104KAT2A |
| 11 | 1 | C36 | CAP., 1000pF, C0G, 25V, 10%, 0603 | AVX, 06033A102KAT2A |
| 12 | 1 | C47 | CAP., 4700pF, X7R, 25V, 10%, 0603 | MURATA, GRM188R71E472KA01D |
| 13 | 1 | C49 | CAP., 1µF, X5R, 10V, 10%, 0603 | MURATA, GRM188R61A105KA61D |
| 14 | 1 | C56 | CAP., 1µF, X5R, 25V, 10%, 0603 | MURATA, GRM188R61E105KA12D |
| 15 | 1 | C58 | CAP., 1µF, X5R, 25V, 10%, 0402 | MURATA, GRM155R61E105KA12D |
| 16 | 1 | C59 | CAP., 10µF, TANT., 16V, 10%, 3216, 1Ω, TPSA | AVX, TPSA106K016R1000 |
| 17 | 1 | C60 | CAP., 4.7µF, X7R, 25V, 10%, 0805 | MURATA, GRM21BR71E475KA73L |
| 18 | 2 | C61, CVIN1 | CAP., 4.7µF, X7R, 50V, 10%, 1206 | MURATA, GRM31CR71H475KA12L |
| 19 | 1 | C62 | CAP.,1000pF, C0G, 50V, 5%, 0603 | MURATA, GRM1885C1H102JA01D |
| 20 | 1 | COUT1 | CAP., 22µF, X7R, 25V, 20%, 1210 | MURATA, GRM32ER71E226ME15L |
| 21 | 2 | D1, D13 | LED, GREEN, DIFFUSED, 0603 | BROADCOM, HSMG-C190 |
| 22 | 1 | D3 | LED, RED, NON-DIFFUSED, 1208, PLCC-2, | VISHAY, VLMS30K1L2-GS08 |
| 23 | 1 | D4 | LED, YELLOW, NON-DIFFUSED, 1208, PLCC-2, | VISHAY, VLMY30K2M1-GS08 |
| 24 | 2 | D8, D9 | DIODE, SCHOTTKY, 30V, 200mW, SOD-323 | DIODES INC., BAT54WS-7-F |
| 25 | 1 | D11 | LED, GREEN, NON-DIFFUSED, 3.0mm × 2.2mm SMD, PLCC-2, | VISHAY, VLMC3101-GS08 |
| 26 | 1 | D12 | DIODE, SCHOTTKY, 100V, 250mA, SOD-323F, AEC-Q101 | NEXPERIA, BAT46WJ |
| 27 | 1 | J2 | CONN., USB-A 2.0, RCPT, FEMALE, 4-POS, 1PORT, R/A HORZ. SMT | WURTH ELEKTRONIK, 62900416021 |
| 28 | 1 | J3 | CONN., USB-B, RCPT, FEMALE, 4POS, 1PORT, R/A HORZ, THT | WURTH ELEKTRONIK, 61400416121 |
| 29 | 2 | JP1, JP5 | CONN., HDR., MALE, 2×3, 2mm, VERT, STR, THT | SAMTEC, TMM-103-02-L-D |
| 30 | 3 | JP2, JP3, JP4 | CONN., HDR, MALE, 2×4, 2mm, VERT, STR, THT | WURTH ELEKTRONIK, 62000821121 |
| 31 | 3 | JP6, JP7, JP8 | CONN., HDR, MALE, 1×3, 2mm, VERT, STR, THT | WURTH ELEKTRONIK, 62000311121 |
| 32 | 1 | L1 | IND., 2.2µH, PWR. SHIELDED, 20%, 5.48mm × 5.28mm, AEC-Q200 | COILCRAFT, XFL5030-222MEB |
| 33 | 4 | L2, L3, L4, L5 | IND., 10nH, HIGH-Q, 3%, 0201, AEC-Q200 | TDK, MLG0603P10NHTD25 |
| 34 | 1 | R1 | RES., 866Ω, 1%, 1/10W, 0603, AEC-Q200 | VISHAY, CRCW0603866RFKEA |
| 35 | 2 | R9, R25 | RES., 330Ω, 1%, 1/10W, 0603, AEC-Q200 | VISHAY, CRCW0603330RFKEA |
| 36 | 11 | R10, R11, R19, R21, R24, R28, R29, R32, R42, R44, R48 | RES., 100k, 1%, 1/10W, 0603, AEC-Q200 | VISHAY, CRCW0603100KFKEA |

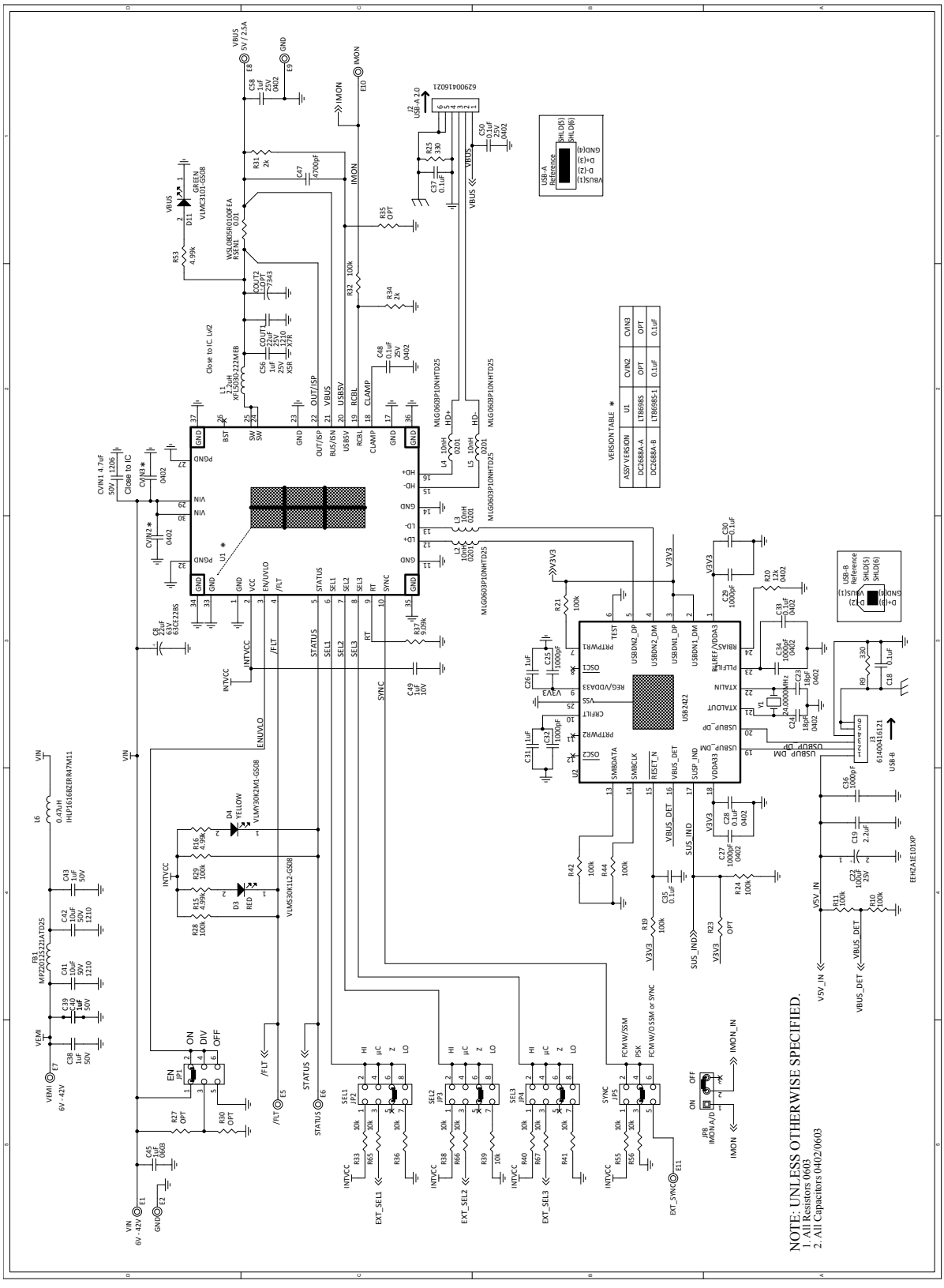
## PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
|---|---|---|---|---|
| 37 | 5 | R15, R16, R51, R52, R53 | RES., 4.99k, 1%, 1/10W, 0603, AEC-Q200 | VISHAY, CRCW06034K99FKEA |
| 38 | 1 | R20 | RES., 12k, 1%, 1/16W, 0402 | VISHAY, CRCW040212K0FKED |
| 39 | 2 | R31, R34 | RES., 2k, 1%, 1/10W, 0603, AEC-Q200 | VISHAY, CRCW06032K00FKEA |
| 40 | 13 | R33, R36, R38, R39, R40, R41, R49, R50, R55, R56, R65, R66, R67 | RES., 10k, 1%, 1/10W, 0603, AEC-Q200 | VISHAY, CRCW060310K0FKEA |
| 41 | 1 | R37 | RES., 9.09k, 1%, 1/10W, 0603, AEC-Q200 | VISHAY, CRCW06039K09FKEA |
| 42 | 1 | R47 | RES., 200k, 1%, 1/10W, 0603 | VISHAY, CRCW06039K09FKEA |
| 43 | 1 | R59 | RES., 0Ω, 1/10W, 0603, AEC-Q200 | VISHAY, CRCW06030000Z0EA |
| 44 | 1 | R61 | RES., 1k, 1%, 1/10W, 0603, AEC-Q200 | VISHAY, CRCW06031K00FKEA |
| 45 | 2 | R62, R63 | RES., 20k, 1%, 1/10W, 0603 | VISHAY, CRCW060320K0FKEA |
| 46 | 1 | R68 | RES., 499k, 1%, 1/10W, 0603, AEC-Q200 | VISHAY, CRCW06031K00FKEA |
| 47 | 1 | RSEN1 | RES., 0.01Ω, 1%, 1/8W, 0805, SENSE, AEC-Q200 | VISHAY, WSL0805R0100FEA |
| 48 | 1 | U2 | IC, 2-PORT USB 2.0 HUB CONTROLLER, SQFN-24 | MICROCHIP, USB2422T-I/MJ |
| 49 | 1 | U3 | IC, MEMORY, EEPROM, 2Kb (256×8), TSSOP-8, 400kHz | MICROCHIP, 24LC025 |
| 50 | 1 | U4 | IC, 500mA LDO LINEAR REGULATOR, MSOP-12 | ANALOG DEVICES, LT3065HMSE-5 |
| 51 | 1 | U5 | IC, 200mA LDO LINEAR REGULATOR, MSOP-8 | ANALOG DEVICES, LT3063EMS8E-3.3#PBF |
| 52 | 1 | U6 | IC, ADC/DAC, 8-CH, 12-BIT, LFCSP-16 | ANALOG DEVICES, AD5593RBCPZ |
| 53 | 1 | Y1 | CRYSTAL, 24.0000MHz, 6pF, 2.0mm × 1.6mm SMD | MURATA, XRCGB24M000F3M00R0 |
| **DC2688A-A Version Specific Components** | | | | |
| 1 | 1 | U1 | IC, USB CHARGER, LQFN-32 | ANALOG DEVICES, LT8698SEV#PBF |
| **DC2688A-B Version Specific Components** | | | | |
| 1 | 1 | U1 | IC, USB CHARGER, LQFN-32 | ANALOG DEVICES, LT8698SEV-1#PBF |
| **Additional Demo Board Circuit Components** | | | | |
| 1 | 1 | C8 | CAP., 22µF, ALUM. ELECT., 63V, 20%, 6.3mm × 7.7mm, CE-BS | SUN ELECTRONIC INDUSTRIES CORP, 63CE22BS |
| 2 | 3 | C38, C40, C43 | CAP., 1µF, X5R, 50V, 10%, 0603 | TDK, CGA3E3X5R1H105K080AB |
| 3 | 2 | C41, C42 | CAP., 10µF, X5R, 50V, 10%, 1210 | MURATA, GRM32ER61H106KA12L |
| 4 | 0 | COUT2 | CAP., OPTION, 7343 | |
| 5 | 2 | CINV2, CINV3 | CAP., 0.1µF, X7R, 50V, 10%, 0402 | MURATA, GRM155R71H104KE14J |
| 6 | 1 | FB1 | IND., 220Ω @ 100MHz, FERRITE BEAD, 25%, 3A, 40mΩ, 0805, AEC-Q200 | TDK, MPZ2012S221ATD25 |
| 7 | 1 | L6 | IND., 0.47µH, PWR., 20%, 7A, 16mΩ, 1616BZ, IHLP-11 SERIES | VISHAY, IHLP1616BZERR47M11 |
| 8 | 0 | R23, R27, R30, R35, R60 | RES., OPTION, 0603 | |
| 9 | 1 | U4 | IC, MEMORY, EEPROM, 2Kb (256x8), TSSOP-8, 400kHz | MICROCHIP, 24LC025-I/ST |
| **Hardware for Demo Board Only** | | | | |
| 1 | 9 | E1, E2, E5, E6, E7, E8, E9, E10, E11 | TEST POINT, TURRET, 0.094" | MILL-MAX, 2501-2-00-80-00-00-07-0 |
| 2 | 1 | J4 | CONN., SHROUDED HDR, MALE, 2×7, 2mm, VERT, STR, THT | MOLEX, 87831-1420 |
| 3 | 4 | MP1, MP2, MP3, MP4 | STANDOFF, NYLON, SNAP-ON, 0.375" | KEYSTONE, 8832 |
| 4 | 7 | XJP1, XJP2, XJP3, XJP4, XJP5, XJP6, XJP7 | CONN., SHUNT, FEMALE, 2-POS, 2mm | SAMTEC, 2SN-BK-G |
| 5 | 1 | XJP8 | CONN., SHUNT, FEMALE, 2-POS, 2mm | WURTH ELEKTRONIK, 60800213421 |

## SCHEMATIC DIAGRAM



# SCHEMATIC DIAGRAM



**ESD Caution**
**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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