

# CK-SSCD Spread Spectrum Differential Clock Specification

## Features

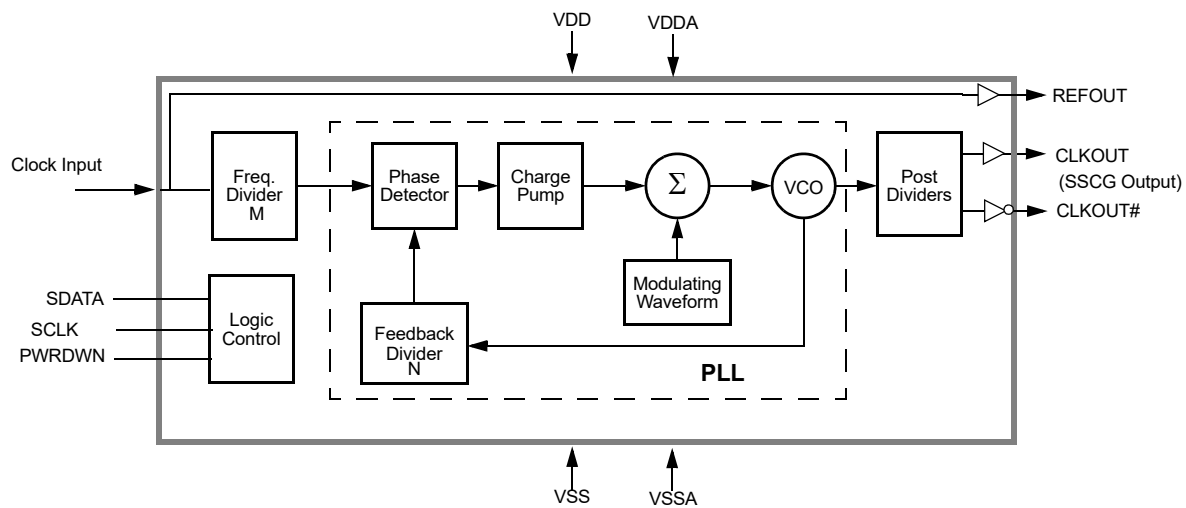
- 3.3 V operation
- 96 MHz and 100 MHz frequency support
- Selectable slew rate control
- 200 ps jitter
- I<sup>2</sup>C programmability

- 250  $\mu$ A power-down current
- Lexmark Spread Spectrum for best electromagnetic interference (EMI) reduction
- 16-pin TSSOP package

## Functional Description

For a complete list of related documentation, click [here](#).

## Logic Block Diagram

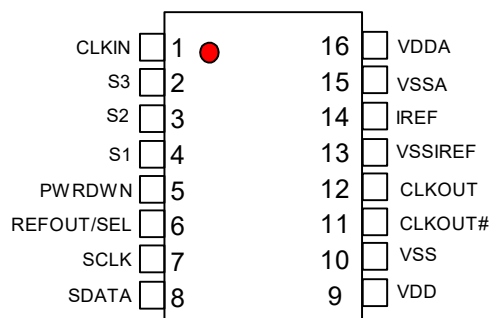


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## Pin Configuration

Figure 1. 16-pin TSSOP pinout



## Pin Definitions

Pin No.	Name	Type	Description
1	CLKIN	Input	<b>3.3 V 14.131818-MHz single-ended clock input</b>
2,3,4	S[3:1]	Input	<b>Spread Spectrum configuration</b>
5	PWRDWN	Input	<b>3.3 V LVTTTL input for power-down active high</b> , no pull-up or pull-down
6	REFOUT/SEL	I/O	<b>Latched input during power-up</b> , 1 (10K external pull-up) = 100 MHz or 0 (10K external pull-down) = 96 MHz. After power-up it becomes 14.31818-MHz REFOUT clock.
7	SCLK	Input	<b>SMBus-compatible SCLK</b>
8	SDATA	I/O	<b>SMBus-compatible SDATA</b>
9	VDD	3.3 V	<b>3.3 V power supply for logic and outputs</b>
10	VSS	Ground	<b>Ground for logic and outputs</b>
11	CLKOUT#	Output	<b>0.7 V 96-MHz or 100-MHz Spread Spectrum differential clock output</b>
12	CLKOUT	Output	<b>0.7 V 96-MHz or 100-MHz Spread Spectrum differential clock output</b>
13	VSSIREF	Ground	<b>Current reference ground</b>
14	IREF	Input	<b>Typically a precision 475Ω external resistor is connected between this pin and VSSIREF to set IOUT (drive current) of CLKOUT differential driver.</b>
15	VSSA	Ground	<b>Ground for PLL</b>
16	VDDA	3.3 V	<b>3.3 V power supply for PLL</b>

## Functional Overview

### Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions such as individual clock output buffers can be individually enabled or disabled.

The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

#### Byte 0: Control Register

Bit	@Power-up	Pin#	Name	Pin Description
7	0	11, 12	SS0	–
6	S1	11, 12	SS1	–
5	S2	11, 12	SS2	–
4	S3	11, 12	SS3	–
3	SEL100/96#	6	SEL100/96#	Select output frequency, 1 = 100 MHz, 0 = 96 MHz
2	0			Reserved must equal 0
1	1	11, 12	Spread Enable	Spread spectrum enable, 0 = Disable, 1 = Enable
0	0		HW/SW Control	Hardware/software control of S[3:0], and output frequency. 0 = hardware control, 1 = software control.

#### Byte 1: [7:2] Control Register

Bit	@Pup	Pin#	Name	Pin Description
7	0			Reserved set equal to '0'
6	0			Reserved set equal to '0'
5	0			Reserved set equal to '0'
4	0			Reserved set equal to '0'
3	0			Reserved set equal to '0'
2	1	11,12	CLKEN	CLKOUT/CLKOUT# enable 0 =Disable, 1 = Enable

#### Byte 1: [1:0] Control Register (Charge Pump Settings)

Bit	@Pup	Default Value	One Step Higher Than Default	Two Steps Higher Than Default
1	0	0	1	1
0	0	0	1	0

#### Bytes 2 through 5: Reserved Registers

Bytes 2 through 5 are Reserved Registers.

#### Byte 6: Vendor/Revision ID Register

Bit	@Pup	Pin#	Name	Pin Description
7	0	–	–	Revision ID Bit 3
6	0	–	–	Revision ID Bit 2
5	0	–	–	Revision ID Bit 1
4	0	–	–	Revision ID Bit 0
3	1	–	–	Vendor ID Bit 3
2	0	–	–	Vendor ID Bit 2
1	0	–	–	Vendor ID Bit 1
0	0	–	–	Vendor ID Bit 0

### Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operation from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individual indexed bytes. The offset of the

indexed byte is encoded in the command code, as described in [Table 1](#).

The block write and block read protocol is outlined in [Table 2](#) while [Table 3](#) outlines the corresponding byte write and byte read protocol. The combined 7 bits slave address and read/write bit form a complete block write (D4h) or block read (D5h) command.

**Table 1. Command Code Definition**

Bit	Description
7	0 = Block read or block write operation 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

**Table 2. Block Read and Block Write Protocol**

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address – 7 bits (D4)	2:8	Slave address – 7 bits (D5)
9	Write = 0	9	Read = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '00000000' stands for block operation	11:18	Command Code – 8 bits '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 0 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	.....	39:46	Data byte from slave – 8 bits
....	Data Byte (N-1) – 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave – 8 bits
....	Data Byte N – 8 bits	56	Acknowledge
....	Acknowledge from slave	....	Data bytes from slave/Acknowledge
....	Stop	....	Data byte N from slave – 8 bits
		....	Not Acknowledge
		....	Stop

**Table 3. Byte Read and Byte Write Protocol**

Byte Write Protocol		Byte Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address – 7 bits (D4)	2:8	Slave address – 7 bits (D5)
9	Write = 1	9	Read = 1
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '100000xx' stands for byte operation, bits[1:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code – 8 bits '100000xx' stands for byte operation, bits[1:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29	Stop	28	Read = 1
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38	Not Acknowledge
		39	Stop

### Spread Enable and Spread Select[3:0]

Spread Enable and Spread Select[3:0] register bits are used to enable and disable spread spectrum on CLKOUT and to change the spread modulation. When the spread selection changes, the CLKOUT output transits to the target spread selection without deviating from clock specifications.

At device power-up spread spectrum is enabled and hardware control mode is enabled. The initial spread-spectrum configuration is determined by the S[3:1] pins, which correspond to the S[3:1] bits in Table 4. The S0 configuration bit is hard-coded to zero when hardware control mode is selected. All four spread spectrum configuration bits, S[3:0], can also be set when the device is in the software control mode.

**Table 4. Spread Spectrum Select (Charge Pump = 00 or Default Condition)**

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
0	0	0	0	Down	0.65
0	0	0	1	Down	0.80
0	0	1	0	Down	0.90
0	0	1	1	Down	1.10
0	1	0	0	Down	1.30
0	1	0	1	Down	1.40
0	1	1	0	Down	1.80
0	1	1	1	Down	2.25
1	0	0	0	Center	±0.25
1	0	0	1	Center	±0.30
1	0	1	0	Center	±0.40
1	0	1	1	Center	±0.45
1	1	0	0	Center	±0.60
1	1	0	1	Center	±0.80
1	1	1	0	Center	±1.00
1	1	1	1	Center	±1.10

**Charge Pump Select Byte1[1:0]**

Programming these bits (Byte1[1:0]) via I<sup>2</sup>C enables the user to have more spread percentage options as described in Table 5. At the start up the default value for byte1[1:0] bits is set to '00', this value can be changed via I<sup>2</sup>C to have higher spread

percentage on CLKOUT and CLKOUT#. Setting the byte[1:0] bits to '11' allows the user to have a slightly higher spread percentage than the default value(00). The '01' option is the highest spread option for maximum EMI reduction.

**Table 5. Spread Spectrum Select (Charge Pump = 11 and 01)**

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount % (Charge pump = 11)	Spread Amount % (Charge pump = 01)
0	0	0	0	Down	0.80	0.90
0	0	0	1	Down	0.90	1.10
0	0	1	0	Down	1.20	1.40
0	0	1	1	Down	1.40	1.60
0	1	0	0	Down	1.60	2.00
0	1	0	1	Down	1.75	2.20
0	1	1	0	Down	2.20	2.75
0	1	1	1	Down	2.60	3.30
1	0	0	0	Center	±0.38	±0.40
1	0	0	1	Center	±0.40	±0.50
1	0	1	0	Center	±0.50	±0.60
1	0	1	1	Center	±0.60	±0.70
1	1	0	0	Center	±0.75	±0.90
1	1	0	1	Center	±1.00	±1.25
1	1	1	0	Center	±1.15	±1.45
1	1	1	1	Center	±1.30	±1.65



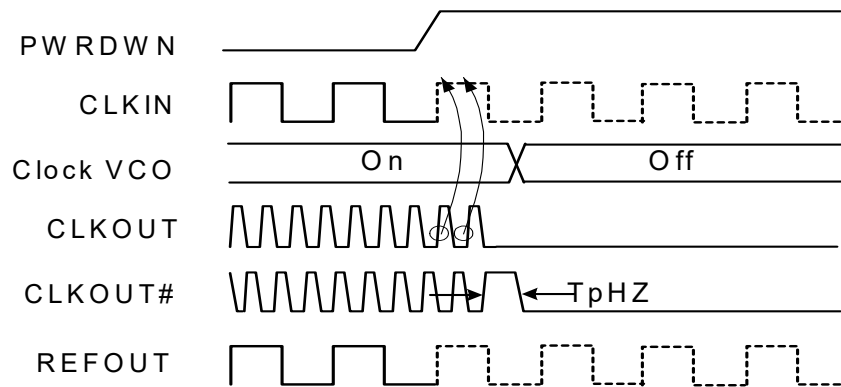
**PWRDWN (Power-down) Clarification**

The PWRDWN (Power-down) pin is used to shut off the clock prior to shutting off power to the device. PWRDWN is an asynchronous active HIGH input. This signal is synchronized internally to the device powering down the clock synthesizer. PWRDWN also is an asynchronous function for powering up the system. When PWRDWN is high, all clocks are tri-stated and the oscillator and PLL are also powered down. All clocks are shut down in a synchronous manner so has not to cause glitches

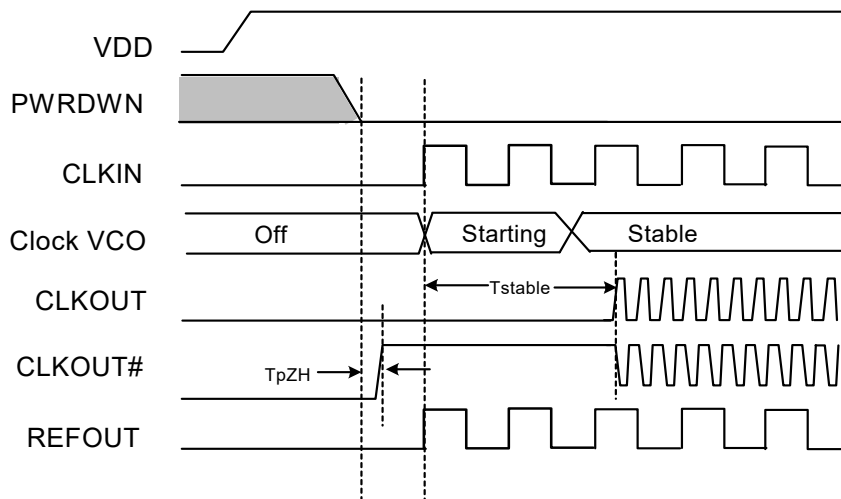
while transitioning to the stopped state. The CLKIN input must be on and within specified operating parameters before PWRDWN is asserted and it must remain in this state while PWRDWN is asserted, see Figure 2.

When PWRDWN is de-asserted (CLKIN starts after powerdown de-assertion to meet the  $I_{DD} \leq 250\mu A$  specification) the clocks should remain stopped until the VCO is stable and within specification ( $t_{STABLE}$ ), see Figure 3.

**Figure 2. Power-down Assertion**



**Figure 3. Power-down Deassertion**



**CLKOUT/CLKOUT# Enable Clarification**

The CLKOUT enable I2C register bit (Byte1, bit2) is used to enable/disable the CLKOUT clock. The PLL and crystal oscillator remains on when the outputs are disabled.

When CLKOUT is disabled, the disabled clock is three-stated. The transition to this mode (three-state) is glitch free. Similarly, when CLKOUT is enabled the clock starts in a predictable manner without any glitches or abnormal behavior.

**Current Reference, IREF**

The details of the current reference circuit are shown in Figure 4. The operational amplifier in the current reference circuit drives

the gate of  $M_{IREF}$  with feedback to establish  $V_{REF} = 1.1\text{ V}$  at both inputs of the amplifier. Thus the reference current is established according to the following formula:

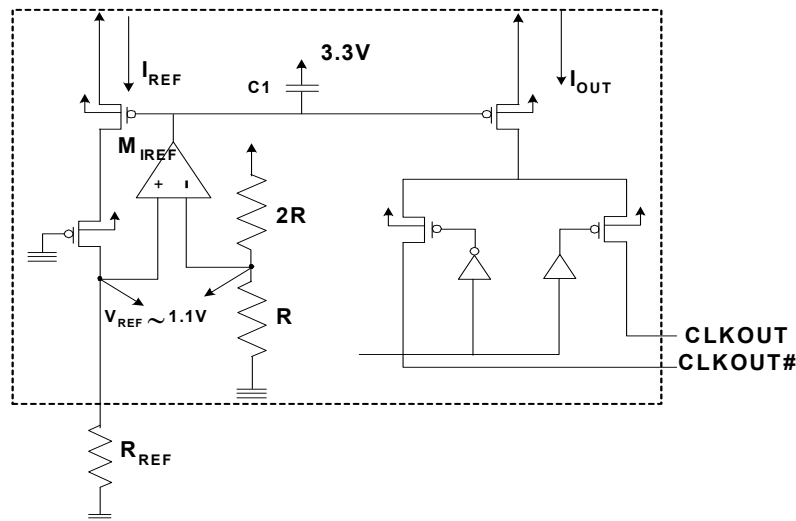
$$I_{REF} = 1.1\text{ V} / R_{REF}$$

where  $R_{REF}$  is the external resistor and 1.1 V is the reference voltage.

The  $I_{REF}$  is scaled by 6x at the output stage and  $I_{OUT}$  is given as:  
 $I_{OUT} = 6 \times I_{REF}$ .

The recommended value for  $R_{REF}$  is 475 Ohms, which corresponds to the  $I_{REF}$  of 2.32 mA.

Figure 4. Current Reference Circuit



## Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V <sub>DD</sub>	Core Supply Voltage		-0.5	4.6	V
V <sub>DDA</sub>	Analog Supply Voltage		-0.5	4.6	V
V <sub>IN</sub>	Input Voltage	Relative to V <sub>SS</sub>	-0.5	V <sub>DD</sub> + 0.5	VDC
T <sub>S</sub>	Temperature, Storage	Non-functional	-65	150	°C
T <sub>A</sub>	Temperature, Operating Ambient	Functional	0	70	°C
T <sub>J</sub>	Temperature, Junction	Functional	-	150	°C
ESD <sub>HBM</sub>	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	-	V

## DC Electrical Specifications

Parameter	Description	Condition	Min	Max	Unit
V <sub>DD</sub>	Power supply for logic and outputs	3.3 ± 5%	3.135	3.465	V
V <sub>DDA</sub>	Power supply for PLL	3.3 ± 5%	3.135	3.465	V
V <sub>IL</sub> I <sub>2C</sub>	Input Low Voltage	SDATA, SCLK	V <sub>SS</sub> - 0.5	0.8	V
V <sub>IH</sub> I <sub>2C</sub>	Input High Voltage	SDATA, SCLK	2.0	V <sub>DD</sub>	V
V <sub>IL</sub>	Input Low Voltage		V <sub>SS</sub> - 0.5	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>DD</sub>	V
I <sub>IL</sub>	Input Leakage Current	except internal pull-ups resistors, 0 < V <sub>IN</sub> < V <sub>DD</sub>	-5	5	μA
I <sub>OZ</sub>	High-impedance Output Current		-10	10	μA
I <sub>DD</sub>	Dynamic Supply Current	without output load	-	50	mA
I <sub>DDS</sub>	Total Power Supply Current in Shutdown mode (No Input Clock)	Shutdown active	-	250	μA
C <sub>IN</sub>	Input Pin Capacitance		2	5	pF
C <sub>OUT</sub>	Output Pin Capacitance		3	6	pF
L <sub>IN</sub>	Input Pin Inductance		-	5	nH
R <sub>PU</sub>	SCLK and SDATA pull-up resistors	when PWRDWN = 1	50	200	kΩ
R <sub>REF</sub>	I <sub>REF</sub> external reference resistor	1% tolerance	200	500	Ω

## Thermal Resistance

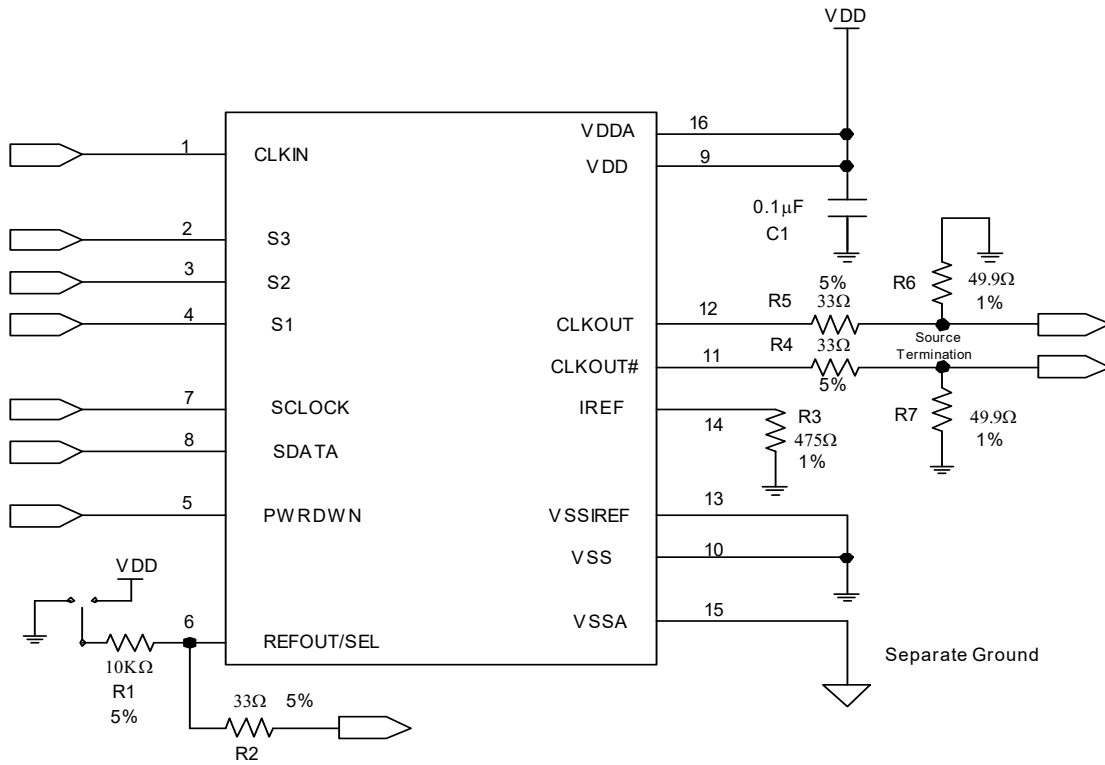
Parameter <sup>[1]</sup>	Description	Test Conditions	16-pin TSSOP	Unit
θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	91	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)		15	°C/W

### Note

1. These parameters are guaranteed by design and are not tested.

**Application Schematic**

**Figure 5. Application Schematic [2, 3]**



**Notes**

2. V<sub>DD</sub> and V<sub>DDA</sub> should be tied together and connected to 3.3 V.
3. V<sub>SSIREF</sub> and V<sub>SS</sub> are tied together and are common ground.

## AC Electrical Specifications

Parameter	Description	Condition	Min	Max	Unit
<b>CLKIN/REFOUT AC Specifications</b>					
T <sub>DC</sub>	Duty Cycle	Measured at 1.5 V crossing point	40	60	%
T <sub>R</sub> / T <sub>F</sub>	Rise and Fall Times	Measured between 0.8 V and 2.0 V (REFOUT with max. 30 pF Lumped capacitive load)	–	1.2	ns
T <sub>CCJ</sub>	Cycle to Cycle Jitter	As an average over 1-μs duration	–	1000	ps
L <sub>ACC</sub>	Long-term Accuracy	Over 150 ms	–	300	ppm
<b>CLKOUT/CLKOUT# AC Specifications</b>					
T <sub>DC</sub>	CLKOUT and CLKOUT# Duty Cycle	Measured at crossing point V <sub>OX</sub>	45	55	%
T <sub>PERIOD</sub>	100 MHz CLKOUT and CLKOUT# Period	Measured at crossing point V <sub>OX</sub>	9.990	10.010	ns
T <sub>PERIOD</sub>	96 MHz CLKOUT and CLKOUT# Period	Measured at crossing point V <sub>OX</sub>	10.406	10.427	ns
T <sub>CCJ</sub>	CLKOUT/CLKOUT# Cycle to Cycle Jitter with Spread Spectrum Enabled	Measured at crossing point V <sub>OX</sub>	–	200	ps
T <sub>R</sub> / T <sub>F</sub>	CLKOUT and CLKOUT# Rise and Fall Times	Measured from V <sub>OL</sub> = 0.175 to V <sub>OH</sub> = 0.525 V	175	700	ps
T <sub>RFM</sub>	Rise/Fall Matching	Determined as a fraction of $2 \times ((T_R - T_F)/(T_R + T_F))$	–	20	%
T <sub>stable</sub> <sup>[4]</sup>	All clock stabilization from Power-up		–	3.0	ms
ΔT <sub>R</sub>	Rise Time Variation		–	125	ps
ΔT <sub>F</sub>	Fall Time Variation		–	125	ps
V <sub>HIGH</sub>	Voltage High		660	850	mv
V <sub>LOW</sub>	Voltage Low		–150	–	mv
V <sub>OX</sub>	Crossing Point Voltage at 0.7 V Swing		250	550	mv
V <sub>OVS</sub>	Maximum Overshoot Voltage		–	V <sub>HIGH</sub> + 0.3	V
V <sub>UDS</sub>	Minimum Undershoot Voltage		–0.3	–	V
V <sub>RB</sub>	Ring Back Voltage	Measure SE	–	0.2	V

**Note**

4. Not 100% tested, guaranteed by design.

## Switching Waveforms

Figure 6. Single-ended Measurement Points for TRise and TFall (CLKOUT and CLKOUT#)

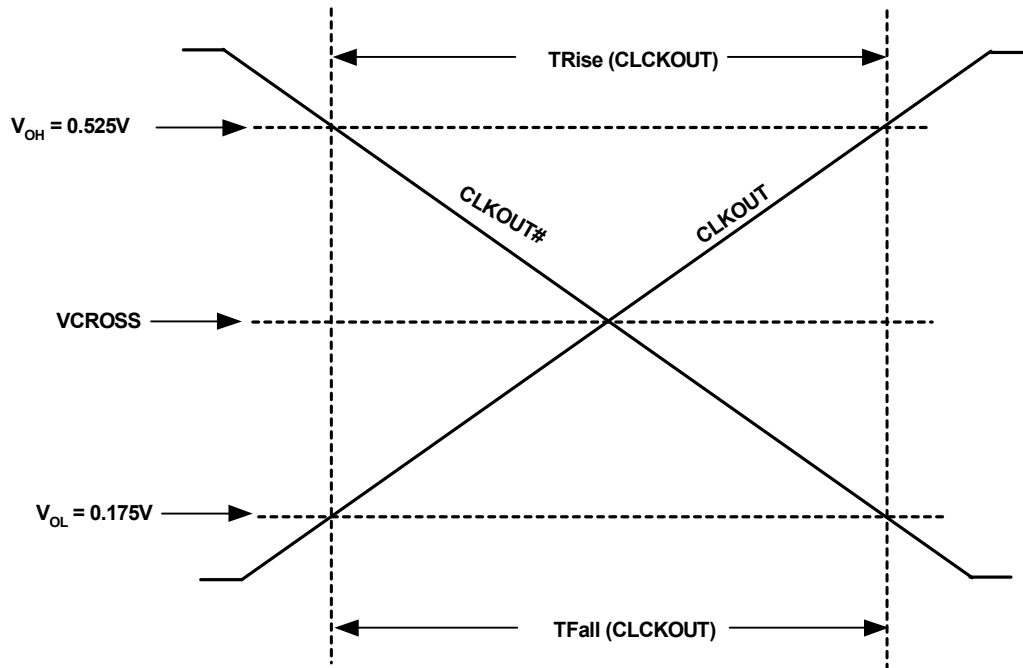
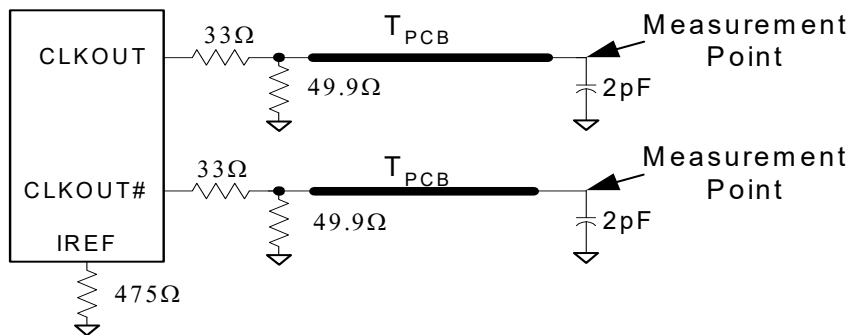


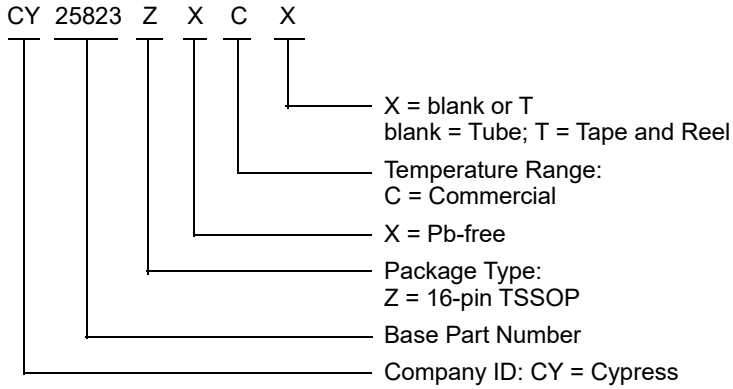
Figure 7. 0.7 V Load Configuration



### Ordering Information

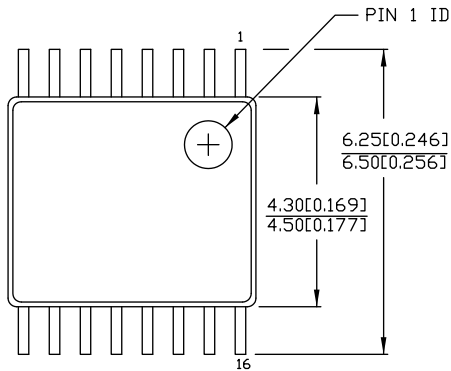
Part Number	Package Type	Product Flow
CY25823ZXC	16-pin TSSOP (Lead-free)	Commercial, 0 °C to 70 °C
CY25823ZXCT	16-pin TSSOP – Tape and Reel (Lead-free)	Commercial, 0 °C to 70 °C

### Ordering Code Definitions



### Package Drawing and Dimensions

Figure 8. 16-pin TSSOP (4.40 mm Body) Z16.173/ZZ16.173 Package Outline, 51-85091

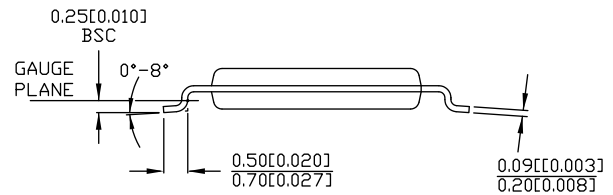
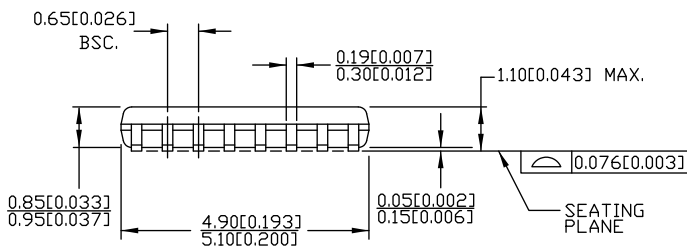


DIMENSIONS IN MM[INCHES] MIN. MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05gms

PART #	
Z16.173	STANDARD PKG.
ZZ16.173	LEAD FREE PKG.



51-85091 \*E



## Acronyms

**Table 6. Acronyms Used in this Document**

Acronym	Description	Acronym	Description
CLKIN	Reference Clock IN	LVC MOS	Low Voltage Complementary Metal Oxide Semiconductor
DL	Drive Level	OE	Output Enable
DNU	Do Not Use	OSC	Oscillator
DUT	Device Under Test	PD	Power-Down
EIA	Electronic Industries Alliance	PLL	Phase Locked Loop
EMI	Electromagnetic Interference	PPM	Parts Per Million
ESD	Electrostatic Discharge	QFN	Quad Flat No Lead
EXCLKIN	External Clock IN	SS	Spread Spectrum
FAE	Field Application Engineer	SSC	Spread Spectrum Clock
FS	Frequency Select	SSON	Spread Spectrum ON
JEDEC	Joint Electron Device Engineering Council		

## Document Conventions

### Units of Measure

**Table 7. Units of Measure**

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	μVrms	microvolts root-mean-square
dB	decibel	μW	microwatt
dBc/Hz	decibel relative to the carrier per Hertz	mA	milliampere
fC	femtoCoulomb	mm	millimeter
fF	femtofarad	ms	millisecond
Hz	hertz	mV	millivolt
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolt
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
μA	microampere	pp	peak-to-peak
μF	microfarad	ppm	parts per million
μH	microhenry	ps	picosecond
μs	microsecond	sps	samples per second
μV	microvolt	σ	sigma: one standard deviation

**Document History Page**

Document Title: CY25823, CK-SSCD Spread Spectrum Differential Clock Specification				
Document Number: 38-07579				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	131662	RGL	12/10/03	New data sheet.
*A	203801	RGL	See ECN	Updated <a href="#">Functional Overview</a> : Updated <a href="#">Data Protocol</a> : Updated <a href="#">Table 2</a> . Updated <a href="#">Table 3</a> .
*B	252269	RGL	See ECN	Corrected to New Lead Free Code
*C	260155	RGL	See ECN	Minor Change: Corrected the package diagram
*D	3196237	BASH	03/15/11	Added <a href="#">Ordering Code Definitions</a> under <a href="#">Ordering Information</a> . Updated <a href="#">Package Drawing and Dimensions</a> : spec 51-85091 – Changed revision from *A to *C. Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated to new template.
*E	4296180	XHT	03/03/2014	Updated <a href="#">Package Drawing and Dimensions</a> : spec 51-85091 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*F	4587350	XHT	12/05/2014	Updated <a href="#">Functional Description</a> : Added “For a complete list of related documentation, click <a href="#">here</a> .” at the end. Updated <a href="#">Package Drawing and Dimensions</a> : spec 51-85091 – Changed revision from *D to *E.
*G	4669367	XHT	02/27/2015	No technical updates. Completing Sunset Review.
*H	5279025	PSR	11/24/2016	Updated <a href="#">Absolute Maximum Conditions</a> : Removed $\theta_{JC}$ , $\theta_{JA}$ parameters and their details. Added <a href="#">Thermal Resistance</a> . Updated to new template.
*I	5993961	AESATMP9	12/14/2017	Updated logo and copyright.
*J	6091326	XHT	04/19/2018	Sunset review.

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