## DESCRIPTIOn

Demonstration circuit 2543B is a high efficiency, high density, open loop charge pump (inductorless) DC/DC converter. This demo board is a voltage divider which achieves a 2:1 step-down ratio from an input voltage from 36 V to 60 V . The output voltage is a fixed ratio of half of the input voltage ( $\mathrm{V}_{\mathrm{IN}} / 2$ ) and can supply a 10 A load current. This demo board has the option to deliver a 20A maximum load with the addition of 15 chip capacitors. See Figure 8 and Figure 10 for the details.
The DC2543B provides a very high efficiency solution of $98.7 \%$ when converting $48 \mathrm{~V}_{\text {IN }}$ to $24 \mathrm{~V}_{\text {OUT }}$ at 10 A as shown in Figure 3. When configured for a 20A output, an efficiency of up to $98.4 \%$ is achievable for a $48 \mathrm{~V}_{\text {IN }}$ to $24 \mathrm{~V}_{\text {OUT }}$ at 20 A as shown in Figure 8.
The demo board features the LTC ${ }^{\circledR} 7820$, a fixed ratio high voltage high power switched capacitor/charge pump controller in a $4 \mathrm{~mm} \times 5 \mathrm{~mm}$ QFN package. Please see LTC7820 data sheet for more detailed information.

The DC2543B needs to be powered on with no load current or a very small load current (less than 50 mA ) with the default setup. Large load current can be applied after $V_{0}$ is established. The board offers a disconnect FET option which is controlled by the LTC7820 FAULT pin to disconnect the load during startup as shown in the schematic. Please refer to "Voltage Divider Prebalance Before Switching" section in the LTC7820 data sheet for more details regarding the startup of the voltage divider. The board also features some protection functions such as overcurrent and thermal shutdown to make it a reliable solution.

## Design files for this circuit board are available.

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## PERFORMANCE SUMMARY Speciictions are at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| PARAMETER | CONDITION | VALUE |
| :--- | :--- | :--- |
| Input Voltage Range |  | 36 V to 60 V |
| Output Voltage, $\mathrm{V}_{\text {OUT }}$ | $\mathrm{V}_{\text {IN }}=36$ to $60 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=0 \mathrm{~A}$ to 10 A | $\mathrm{~V}_{\text {IN }} / 2$ |
| Maximum Output Current, I IOUT | $\mathrm{V}_{\text {IN }}=36$ to $60 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=\mathrm{V}_{\text {IN }} / 2$ | 10 A |
| Typical Efficiency | $\mathrm{V}_{\text {IN }}=48 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=24 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=10 \mathrm{~A}$ | $98.7 \%$ |
| Peak Efficiency | $\mathrm{V}_{\text {IN }}=48 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=24 \mathrm{~V}$ | $99 \%$ |
| Switching Frequency |  | 200 kHz |

NOTE: DC2543B demo board includes a Schottky diode added across the output. This manual describes the demo board entitled "Demo Circuit 2543B." The DC2543B replaces the DC2543A.

## DEMO MANUAL DC2543B

## PUICK START PROCEDURE

Demonstration circuit 2543B is easy to set up to evaluate the performance of the LTC7820. Refer to Figure 1 for the proper measurement equipment setup and follow the procedure below.

1. With power off, connect the input power supply to $V_{\text {IN }}$ ( 36 V to 60 V ) and GND (input return).
2. Connect the output loads between $V_{\text {OUT }}$ and GND (Initial load: no load). Refer to Figure 1.
3. Connect the DVMs to the input and output.
4. Check the default jumper/switch position: SW1 (RUN): OFF; JP2 (BIAS): ON.
5. Turn on the input power supply and adjust voltage to 48 V .

NOTE: Make sure that the input voltage does not exceed 60V.
6. Turn on the switches: SW1: ON.
7. Check for the proper output voltages from $\mathrm{V}_{\mathrm{O}_{-} \mathrm{SNS}}{ }^{+}$to Vo_SNS ${ }^{-}$.
8. Once the proper output voltage is established, adjust the loads within the operating range and measure the efficiency, output ripple voltage and other parameters.
9. After completing all tests, adjust the load to 0 A , power off the input power supply.

Notes:

1. When measuring the output or input voltage ripple, do not use the long ground lead on the oscilloscope probe. See Figure 3 for the proper scope probe technique. Short, stiff leads need to be soldered to the (+) and ( - ) terminals of an output capacitor. The probe's ground ring needs to touch the (-) lead and the probe tip needs to touch the (+) lead.
2. When doing the load step test with the on-board dynamic load circuit, please make sure the load stepup pulse duty cycle does not exceed $2 \%$ and the pulse duration is less than $500 \mu \mathrm{~s}$ so that the temperature of the MOSFETs Q9, Q23 in the dynamic load circuit stay in the safe region. Instead of using the on-board dynamic load circuit, an electric load can also be used for the load step test, which does not have the $2 \%$ maximum duty cycle limit for the load step.
3. It is recommended to set the electronic load in CR (constant resistance) mode for evaluation of the DC2543B board. Some electronic loads draw negative current in CC (constant current) mode when evaluating the output overcurrent protection feature of DC2543B, which can violate the absolute maximum voltage rating -0.3 V for V Low pin.

## PUICK START PROCEDURE



Figure 1. Proper Measurement Equipment Setup
Note: It is recommended to set the electronic load in CR (constant resistance) mode for evaluation of the DC2543B board. Some electronic loads draw negative current in CC (constant current) mode when evaluating the output overcurrent protection feature of DC2543B, which can violate the absolute maximum voltage rating -0.3 V for $\mathrm{V}_{\text {Low }}$ pin.


Figure 2. Measuring Output Voltage Ripple

## DEMO MANUAL DC2543B

## PUICK START PROCEDURE



Figure 3. Efficiency vs Load Current at $\mathrm{V}_{\mathrm{IN}}=48 \mathrm{~V}$, $\mathrm{V}_{\text {OUT }}=24 \mathrm{~V}, \mathrm{I}_{\text {SW }}=200 \mathrm{kHz}$


Figure 5. Output Voltage Ripple at $V_{I N}=48 \mathrm{~V}$, $V_{\text {OUT }}=24 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=10 \mathrm{~A}, \mathrm{f}_{\text {SW }}=200 \mathrm{kHz}$


Figure 4. Load Regulation for 10A Design at $\mathrm{V}_{\text {IN }}=48 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=24 \mathrm{~V}, \mathrm{I}_{\text {SW }}=200 \mathrm{kHz}$


Figure 6. Load Step at $V_{I N}=48 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=24 \mathrm{~V}$


Figure 7. Thermal performance $V_{I N}=48 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=24 \mathrm{~V}, I_{O U T}=10 \mathrm{~A}$,
$\mathrm{T}_{\mathrm{A}}=23^{\circ} \mathrm{C}$, No Airflow

## PUICK START PROCEDURE



Figure 8. Efficiency vs Load Current at $\mathrm{V}_{\mathrm{IN}}=48 \mathrm{~V}$, $\mathrm{V}_{\text {OUT }}=24 \mathrm{~V}, \mathrm{f}_{\text {SW }}=200 \mathrm{kHz}{ }^{*}$


Figure 9. Load Regulation for 20A Design at $\mathrm{V}_{\text {IN }}=48 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=24 \mathrm{~V}$, $\mathrm{f}_{\mathrm{SW}}=200 \mathrm{kHz}$ *


Figure 10. Thermal performance at $\mathrm{V}_{\text {IN }}=48 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=24 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=20 \mathrm{~A}$ $\mathrm{T}_{\mathrm{A}}=23^{\circ} \mathrm{C}$, No Airflow *

* Note: Additional C11, C12, C60, C61, C22-C25, C69-C72, C30, C31, and C36 (10ヶF/50V, MURATA GRM32ER71H106KA12L) are populated; RS1 is changed to $2.5 \mathrm{~m} \Omega$ (WSL20102L500FEB18) for this test.


## DEMO MANUAL DC2543B

## PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
| :---: | :---: | :---: | :---: | :---: |
| Required Circuit Components |  |  |  |  |
| 1 | 1 | C1 | CAP, 33 $\mu \mathrm{F} 20 \%$ 80V ELEC | PANASONIC EEHZA1K330P |
| 2 | 8 | C2, C3, C47, C49, C56, C57, C58, C59 | CAP, 1210 2.2 2 F 10\% 100V X7R | MURATA GRM32DR72A225KA12 |
| 3 | 4 | C4, C5, C15, C126 | CAP, 0603 0.1的 10\% 100V X7R | MURATA GRM188R72A104KA35D |
| 4 | 2 | C6, C7 | CAP, 0805 4.7 F F 10\% 16V X7R | MURATA GRM21BR71C475KA73K |
| 5 | 1 | C8 | CAP, $06030.22 \mu \mathrm{~F} 10 \% 25 \mathrm{~V}$ X7R | MURATA GRM188R71E224KA88D |
| 6 | 2 | C9, C26 | CAP, 0603 0.47 $\mu \mathrm{F} 10 \% 25 \mathrm{~V}$ X7R | MURATA GRM188R71E474KA12D |
| 7 | 2 | C17, C28 | CAP, 0805 2.2 $2 \mathrm{~F} 10 \%$ 50V X7R | TDK C2012X7R1H225K125AC |
| 8 | 11 | C18, C19, C20, C21, C29, C66, C67 | CAP, 1210 10 F 10\% 50V X7R | MURATA GRM32ER71H106KA12L |
| 9 |  | C68, C73, C74, C65 |  |  |
| 10 | 2 | C27, C50 | CAP, $06031 \mu \mathrm{~F} 10 \% 50 \mathrm{~V}$ X5R | MURATA GRM188R61H105K |
| 11 | 2 | C52, C53 | CAP, 1210 22 F 10\% 25V X5R | AVX 12103D226KAT2A |
| 12 | 1 | C54 | CAP, 0603 47nF 10\% 25V X7R | AVX 06033C473KAT2A |
| 13 | 1 | C55 | CAP, 0603 470pF 10\% 50V X7R | MURATA GRM188R71H471KA01D |
| 14 | 3 | D1, D2, D3 | DIODE, SCHOTTKY | CENTRAL SEMI. CMDSH-4E TR |
| 15 | 1 | D6* | DIODE, SCHOTTKY | ON SEMI, NRVTSAF5100E |
| 16 | 2 | D9, D10 | DIODE, ZENER | CENTRAL SEMI. CMHZ5236B TR |
| 17 | 1 | L2 | IND, 68 ${ }^{\text {H }}$ | COILCRAF., LPS6225-683MRB |
| 18 | 1 | Q1 | XSTR, N-CHANNEL MOSFET | INFINEON BSCO27N06LS5 |
| 19 | 3 | Q3, Q6, Q7 | XSTR, N-CHANNEL MOSFET | INFINEON BSC032N04LS |
| 20 | 4 | Q9, Q10, Q11, Q23 | XSTR, N-CH 40V 14A TO-252 | VISHAY SUD50N04-8M8P-4GE3 |
| 21 | 1 | Q22 | TRANSISTOR., SOT-23 | FAIRCHILD., BSS123L |
| 22 | 1 | RS1 | RES., CHIP, 0.005, 1\%, 2010 | VISHAY, WSL20105L000FEA |
| 23 | 1 | RS2 | RES, $20100 \Omega$ JUMPER | VISHAY WSL201000000ZEA9 |
| 24 | 2 | R1, R7 | RES, 0603 1k $21 \%$ | VISHAY CRCW06031K00FKEA |
| 25 | 1 | R2 | RES, $06032.2 \Omega 5 \%$ | YAGEO RC0603JR-072R2L |
| 26 | 4 | R5, R10, R24, R32 | RES, $06030 \Omega$ JUMPER | VISHAY CRCW06030000ZOEA |
| 27 | 4 | R9, R13, R17, R28 | RES, $060310 \mathrm{k} \Omega 1 \%$ | NIC NRC06F1002TRF |
| 28 | 1 | R16 | RES, 0603 60.4k $1 \%$ | VISHAY CRCW060360K4FKEA |
| 29 | 1 | R18 | RES, 0603 100k 1 1\% | VISHAY CRCW0603100KFKEA |
| 30 | 1 | R26 | RES, 0603 154k 1 1\% | YAGEO RC0603FR-07154KL |
| 31 | 1 | R27 | RES, 0603 20k 5 \% | VISHAY CRCW060320KOJNEA |
| 32 | 1 | R29 | RES, 0603 80.6k $1 \%$ | YAGEO RC0603FR-0780K6L |
| 33 | 1 | R30 | RES. 2010 1ת 1\% 1W | IRC LRC-LR2010-01-1R00-F |
| 34 | 1 | R31 | RES, $0603100 \Omega 5 \%$ | VISHAY CRCW0603100ROJNEA |
| 35 | 1 | U1 | IC, LTC7820EUFD, QFN 4mm $\times 5 \mathrm{~mm}$ | ANALOG DEVICES, LTC7820EUFD\#PBF |
| 36 | 1 | U2 | IC, LTC3630AEMSE | ANALOG DEVICES, LTC3630EMSE\#PBF |

## PARTS LIST

## Additional Demo Board Circuit Components

| 1 | 0 | C10-C14, C16, C33, C34, C35, C36, <br> C60-C64, C51, C77 | CAPACITOR, OPT |  |
| :---: | :--- | :--- | :--- | :--- |
| 2 | 0 | C30-C32, C22-C25, C69-C72, C127 |  |  |
| 3 | 0 | Q2, Q4, Q5,Q8 OPT | MOSFET, OPT |  |
| 4 | 0 | R6, R19, R2, R36, R8, R11, R12, <br> R20, R34, R35, R60 | RESISTOR, OPT |  |

Hardware: For Demo Board Only

| 1 | 9 | E1, E2, E6-E8, E10, E12, E14, E15 | TURRET | MILL-MAX 2501-2-00-80-00-00-07-0 |
| :---: | :--- | :--- | :--- | :--- |
| 2 | 1 | JP2 | HEADER, 3 PIN 2mm | WURTH ELEKTRONIK 62000311121 |
| 3 | 4 | J1, J2, J3, J4 | JACK, BANANA | KEYSTONE, 575-4 |
| 4 | 2 | J5, J6 | CONN, BNC, 5 PINS | CONNEX, 112404 |
| 5 | 1 | SW1 | SWITCH, SUBMINIATURE SLIDE | C\&K COMPONENTS, JS202011CQN |
| 6 | 1 | XJP2 | SHUNT 2mm | WURTH ELEKTRONIK 60800213421 |
| 7 | 4 | STANDOFF | STANDOFF, SNAP ON | KEYSTONE 8833 |

*Note: D6 is for negative voltage clamping on V OUT of DC2543B board in output overcurrent test with electronic load. Some electronic loads draw negative current in CC mode when evaluating the output overcurrent protection feature of DC2543B, which can violate the absolute maximum voltage rating -0.3 V for $V_{\text {Low }}$ pin without D6 populated.

## DEMO MANUAL DC2543B

## SCHEMATIC DIAGRAM



## SCHEMATIC DIAGRAM




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