

PacketClock™ Spread Spectrum Clock Generator

Features

- Integrated phase-locked loop (PLL)
- Low jitter, high-accuracy outputs
- 3.3 V operation
- 25 MHz input frequency
- 33.33 MHz or 25 MHz selectable output frequency (-21)

Benefits

- High-performance PLL tailored for spread spectrum application
- Meets critical timing requirements in complex system designs
- Enables application compatibility
- Works with commonly available crystal or driven reference
- Downspread spread spectrum with 30 kHz nominal modulation frequency

Functional Description

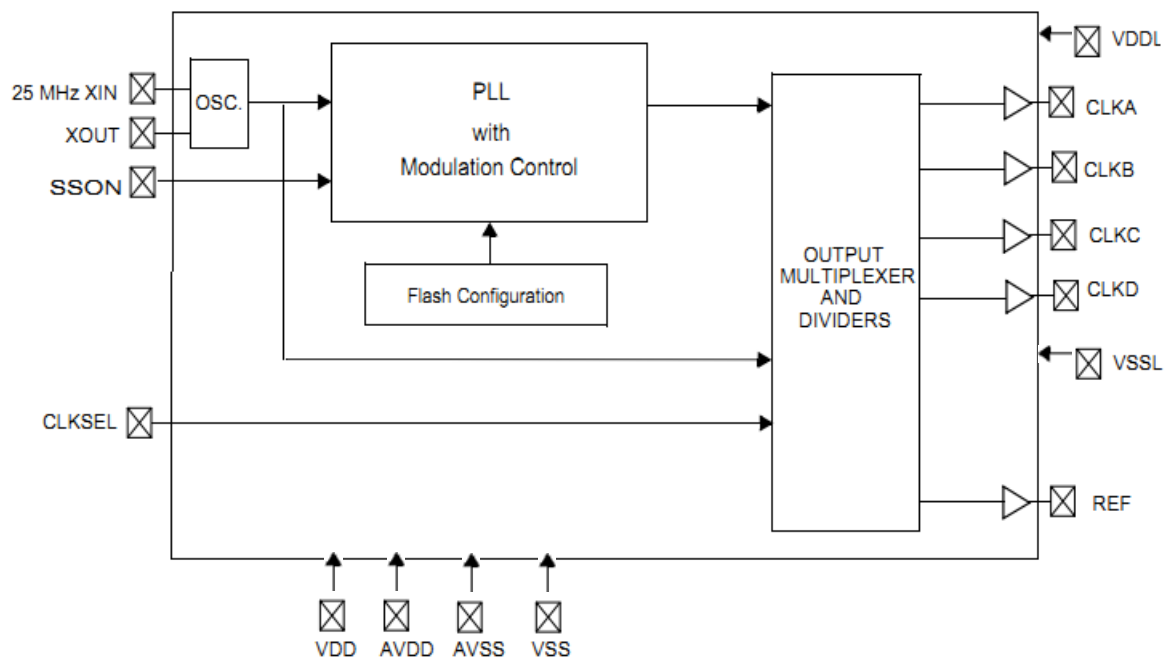
For a complete list of related resources, [click here](#).

Frequency Table

for CLKA-D

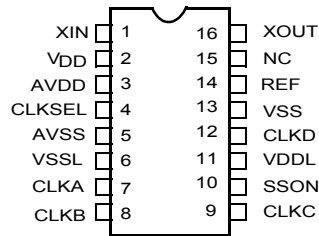
| Part Number | CLKSEL = 0 | CLKSEL = 1 | Spread% | Parallel Crystal Load |
|-------------|------------|------------|---------|-----------------------|
| CY26121-21 | 33.33 MHz | 25.00 | -2.8% | 15 pF |

Logic Block Diagram



Pin Configuration

Figure 1. 16-pin TSSOP pinout



Pin Definitions

| Pin Name | Pin Number | Description |
|---------------------|-------------|---|
| XIN | 1 | Reference input Or crystal input |
| VDD | 2 | 3.3 V voltage supply |
| AVDD | 3 | 3.3 V analog voltage |
| CLKSEL | 4 (-21) | 0 = 33.33 MHz out, 1 = 25 MHz Out. Weak pull-up. |
| AVSS | 5 | Analog ground |
| VSSL | 6 | CLK ground |
| CLK(A:D) | 7, 8, 9, 12 | Clock outputs at V _D DL level |
| SSON | 10 | Spread spectrum enable pin 0 = SS off; 1 = SS on. Weak pull-up. |
| VDDL | 11 | 3.3 V clock voltage supply |
| VSS | 13 | Ground |
| REF | 14 | Reference output at V _D D level |
| NC | 15 | No connect |
| XOUT ^[1] | 16 | Crystal output |

Notes

1. Float XOUT if XIN is externally driven.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Supply voltage (V_{DD} , AV_{DD} , V_{DDL}) -0.5 to +7.0 V
 DC input voltage -0.5 V to $V_{DD} + 0.5$ V

Storage temperature
 (Non-condensing) -55 °C to +125 °C
 Junction temperature -40 °C to +125 °C
 Data retention at $T_j = 125$ °C > 10 years
 Package power dissipation 350 mW
 Static discharge voltage
 (per MIL-STD-883, Method 3015) ≥ 2000 V

Recommended Operating Conditions

| Parameter | Description | Min | Typ | Max | Unit |
|----------------------|---|-------|------|-------|------|
| V_{DD} , AV_{DD} | Supply voltage | 3.135 | 3.30 | 3.465 | V |
| V_{DDL} | Supply voltage for CLK (A-D) | 3.135 | 3.30 | 3.465 | V |
| T_A | Ambient temperature (industrial temp grade) | -40 | - | 85 | °C |
| C_{LOAD} | Max. output load capacitance | - | - | 15 | pF |
| F_{ref} | Reference frequency | - | 25 | - | MHz |

Crystal Specification

| Parameter ^[2] | Description | Min | Typ | Max | Unit |
|--------------------------|--------------------------------|-----|-----|-----|----------|
| CR_{load} | Crystal load capacitance (-21) | - | 15 | - | pF |
| ESR | Equivalent series resistance | - | - | 50 | Ω |

DC Electrical Specifications

| Parameter | Description | Condition | Min | Typ | Max | Unit |
|-------------------------|--------------------------------|---|---------------------|-----|---------------------|------------|
| I_{OH} | Output high current | $V_{OH} = V_{DD} - 0.5$ V, $V_{DD}/V_{DDL} = 3.3$ V | 12 | 24 | - | mA |
| I_{OL} | Output low current | $V_{OL} = 0.5$ V, $V_{DD}/V_{DDL} = 3.3$ V | 12 | 24 | - | mA |
| I_{IH} | Input high current | $V_{IH} = V_{DD}$ | - | 5 | 10 | μ A |
| I_{IL} | Input low current | $V_{IL} = 0$ V | - | - | 50 | μ A |
| V_{IH} | Input high voltage | CMOS levels | $0.7 \times V_{DD}$ | - | - | V |
| V_{IL} | Input low voltage | CMOS levels | - | - | $0.3 \times V_{DD}$ | V |
| C_{IN} ^[3] | Input capacitance | Input pins excluding XIN | - | - | 7 | pF |
| R_{UP} ^[3] | Pull-up resistor on input pins | $V_{DD} = 3.14$ to 3.47 V, measured at $V_{IN} = 0$ V | 80 | 100 | 150 | k Ω |
| I_{DD} | Supply current | $AV_{DD}/V_{DD}/V_{DDL}$ Current. | - | 42 | 60 | mA |

Thermal Resistance

| Parameter ^[3] | Description | Test Conditions | 16-pin TSSOP | Unit |
|--------------------------|--|---|--------------|------|
| θ_{JA} | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51. | 90 | °C/W |
| θ_{JC} | Thermal resistance (junction to case) | | 14 | °C/W |

Notes

- A fundamental parallel resonant crystal must be used.
- Guaranteed by Characterization, not 100% tested.
- These parameters are guaranteed by design and are not tested.

AC Electrical Specifications

| Parameter ^[4] | Description | Condition | Min | Typ | Max | Unit |
|--------------------------|---------------------------------|--|-----|-----|-----|------|
| DC | Output duty cycle | Duty Cycle is defined in Figure 2, 50% of V_{DD} | 45 | 50 | 55 | % |
| ER | Rising edge rate | Output clock edge rate, measured from 20% to 80% of V_{DD} , $C_{LOAD} = 15$ pF. See Figure 3. | 0.8 | 1.4 | – | V/ns |
| EF | Falling edge rate | Output clock edge rate, measured from 80% to 20% of V_{DD} , $C_{LOAD} = 15$ pF. See Figure 3. | 0.8 | 1.4 | – | V/ns |
| tj | RMS clock cycle-to-cycle Jitter | RMS cycle-to-cycle jitter with spread on. Measured at $V_{DD}/2$. | – | 15 | 40 | ps |

Voltage and Timing Definitions

Figure 2. Duty Cycle Definition

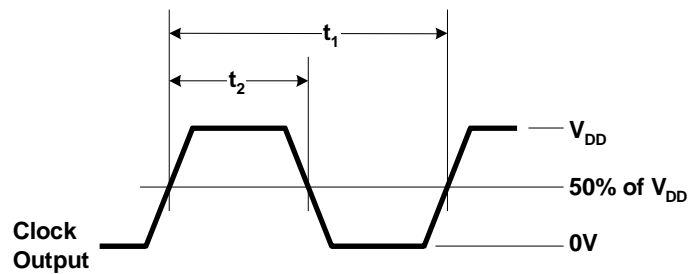
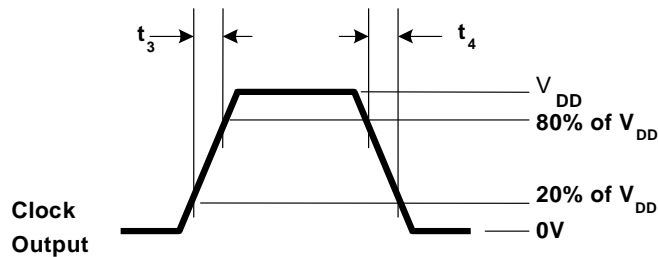


Figure 3. $ER = (0.6 \times V_{DD}) / t_3$, $EF = (0.6 \times V_{DD}) / t_4$



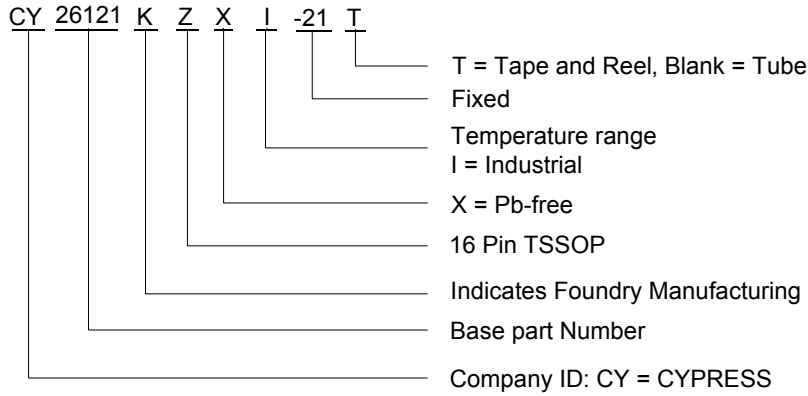
Notes

- Guaranteed by Characterization, not 100% tested.

Ordering Information

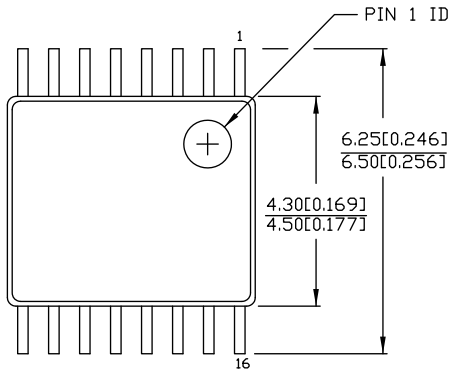
| Ordering Code | Package Type | Operating Range |
|-----------------|------------------------------|-----------------------------|
| CY26121KZXI-21 | 16-pin TSSOP | Industrial, -40 °C to 85 °C |
| CY26121KZXI-21T | 16-pin TSSOP – Tape and Reel | Industrial, -40 °C to 85 °C |

Ordering Code Definitions



Package Drawing and Dimensions

Figure 4. 16-pin TSSOP (4.40 mm Body) Z16.173/ZZ16.173 Package Outline, 51-85091

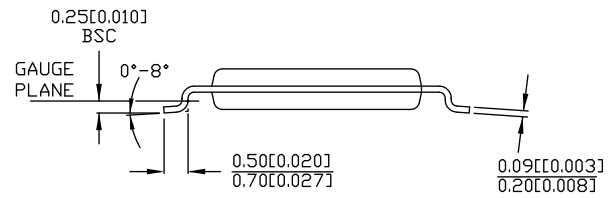
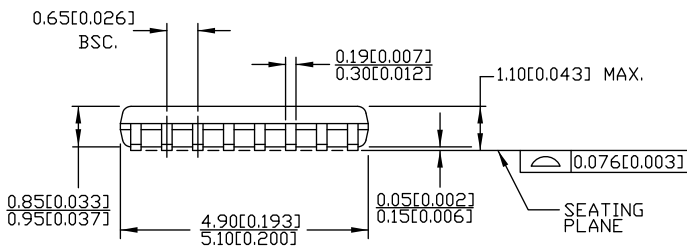


DIMENSIONS IN MM [INCHES] MIN. MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05gms

| PART # | |
|----------|----------------|
| Z16.173 | STANDARD PKG. |
| ZZ16.173 | LEAD FREE PKG. |



51-85091 *E

Acronyms

Table 1. Acronyms Used in this Document

| Acronym | Description |
|---------|-----------------------------------|
| ESR | Equivalent Series Resistance |
| PLL | Phase-Locked Loop |
| TSSOP | Thin-Shrunk Small Outline Package |

Document Conventions

Units of Measure

Table 2. Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| kΩ | kiloohm |
| MHz | megahertz |
| μA | microampere |
| mA | milliampere |
| mW | milliwatt |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| ps | picosecond |
| V | volt |

Document History Page

| Document Title: CY26121, PacketClock™ Spread Spectrum Clock Generator Document Number: 38-07350 | | | | |
|--|---------|------------|-----------------|---|
| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change |
| ** | 121669 | 02/11/03 | CKN | New data sheet. |
| *A | 2440886 | See ECN | KVM / AESA | Updated Ordering Information : Added part numbers CY26121ZXC-21, CY26121ZXC-21T, CY26121ZXI-21, and CY26121ZXI-21T. Added part numbers CY26121KZC-21, CY26121KZC-21T, CY26121KZI-21, and CY26121KZI-21T. Added part numbers CY26121KZXC-21, CY26121KZXC-21T, CY26121KZXI-21, and CY26121KZXI-21T. Removed part numbers CY26121ZI-11, CY26121ZI-11T, CY26121ZI-31 and CY26121ZI-31T. Added Note "Not recommended for new designs." and referred in some MPNs. Updated to new template. |
| *B | 2899683 | 03/26/10 | KVM | Removed reference to -2, -3, -11, -31 parts in all instances across the document. Updated Ordering Information : Removed inactive parts. Removed Note "Not recommended for new designs." and its references. Updated Package Drawing and Dimensions . |
| *C | 3383431 | 09/26/2011 | PURU | Updated Logic Block Diagram. Added Ordering Code Definitions under Ordering Information . Updated Package Drawing and Dimensions . Added Acronyms and Units of Measure . |
| *D | 4556342 | 10/30/2014 | TAVA | Updated Package Drawing and Dimensions : spec 51-85091 – Changed revision from *C to *E. Updated to new template. Completing Sunset Review. |
| *E | 5279177 | 05/20/2016 | PSR | Added Thermal Resistance . Updated to new template. |

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