Low Jitter Clock Generator with Eight LVPECL Outputs

Data Sheet

AD9525

FEATURES

- Integrated ultralow noise synthesizer
- 8 differential 3.6 GHz LVPECL outputs and 1 LVPECL SYNC output or 2 CMOS SYNC outputs
- 2 differential reference inputs and 1 single-ended reference input

APPLICATIONS

- LTE and multicarrier GSM base stations
- Clocking high speed ADCs, DACs
- ATE and high performance instrumentation
- 40/100 Gb/sec OTN line side clocking
- Cable/DOCSIS CMTS clocking
- Test and measurement

FUNCTIONAL BLOCK DIAGRAM

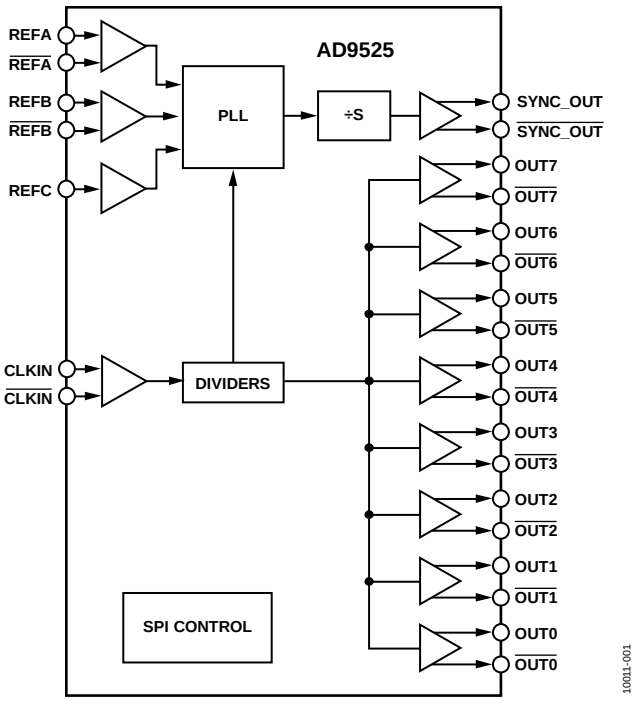

Figure 1.

GENERAL DESCRIPTION

The AD9525 is designed to support converter clock requirements for long-term evolution (LTE) and multicarrier GSM base station designs.

The AD9525 provides a low power, multioutput, clock distribution function with low jitter performance, along with an on-chip PLL that can be used with an external VCO or VCXO. The VCO input and eight LVPECL outputs can operate up to a frequency of 3.6 GHz. All outputs share a common divider that can provide a division of 1 to 6.

The AD9525 offers a dedicated output that can be used to provide a programmable signal for resetting or synchronizing a data converter. The output signal is activated by a SPI write.

The AD9525 is available in a 48-lead LFCSP and can be operated from a single 3.3 V supply. The external VCXO or VCO can have an operating voltage of up to 5.5 V.

The AD9525 operates over the extended industrial temperature range of −40°C to +85°C.

Rev. A

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REVISION HISTORY

4/13—Rev. 0 to Rev. A

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10/12—Revision 0: Initial Version

SPECIFICATIONS

Typical is given for VDD3 = 3.3 V ± 5%; VDD3 ≤ VDD_CP ≤ 5.25 V; T_A = 25°C; OUT_RSET resistor = 4.12 kΩ; CP_RSET resistor (CPRSET) = 5.1 kΩ, unless otherwise noted. Minimum and maximum values are given over full VDD3 and T_A (−40°C to +85°C) variation as listed in Table 1. REFA at 122.88 MHz, CLKIN frequency = 2949.12 MHz.

CONDITIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
VDD3		3.3		V	3.3 V ± 5%
VDD_CP	VDD3		5.25	V	Nominally 3.3 V to 5.0 V ± 5%
OUT_RSET PIN RESISTOR		4.12		kΩ	Sets internal biasing currents; connect to ground
CP_RSET PIN RESISTOR (CPRSET RESISTOR)		5.1		kΩ	Sets internal CP current range, nominally 4.8 mA (CP_LSB = 600 µA); actual current calculated by CP_LSB = 3.06/CPRSET, connect to ground; CPRSET range = 2.7 kΩ to10 kΩ
TEMPERATURE RANGE, T_A	−40	+25	+85	°C	

SUPPLY CURRENT

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT FOR VDD3 and VDD_CP PINS					f_{CLK} = 2949.12 MHz; REFA and REFB enabled at 122.88 MHz; R dividers = 2; M divider = 2; PFD = 61.44 MHz; eight LVPECL outputs at 1474.56 MHz; LVPECL 780 mV mode
VDD3 (Pin 3, Pin 36, Pin 41, Pin 46), Total Supply Voltage for Outputs		310	369	mA	Outputs terminated with 50 Ω to VDD3 − 2 V
VDD3 (Pin 9), Supply Voltage for M Divider, CLK Inputs and Distribution		98	107	mA	
VDD_CP (Pin 13), Supply Voltage for Charge Pump		6.6	7.6	mA	
VDD3 (Pin 20), Supply Voltage for PLL		53	63.4	mA	
VDD3 (Pin 32), Supply Voltage for SYNC_OUT		45	54	mA	

POWER DISSIPATION

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION, CHIP					Does not include power dissipated in external resistors; all LVPECL outputs terminated with 50 Ω to VDD3 − 2 V; LVPECL 780 mV mode
Power-On Default		782	871	mW	No programming; default register values
Typical Operation 1		1.15	1.23	W	f_{CLK} = 2949.12 MHz; REFA and REFB enabled at 122.88 MHz; R dividers = 2; M divider = 2; PFD = 61.44 MHz; eight LVPECL outputs at 1474.56 MHz
Typical Operation 2		1.17	1.25	W	f_{CLK} = 2949.12 MHz; PLL on; REFA enabled at 122.88 MHz; M divider = 1; PFD = 122.88MHz; eight LVPECL outputs at 2949.12 MHz
$\overline{PD}$ Power-Down		51	56.4	mW	$\overline{PD}$ pin pulled low
$\overline{PD}$ Power-Down, Maximum Sleep		13.2	19.1	mW	$\overline{PD}$ pin pulled low; power-down distribution reference, Reg. 0x230[1] = 1b; note that powering down distribution reference disables safe power-down mode (see Power-Down Modes section)
VDD_CP Supply		22	25	mW	PLL operating; typical closed-loop configuration

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DELTAS, INDIVIDUAL FUNCTIONS					Power delta when a function is enabled/disabled
M Divider On/Off		5	8.7	mW	M divider bypassed
P Divider On/Off		3	5.7	mW	P divider bypassed
B Divider On/Off		16	23.1	mW	B divider bypassed
REFB On		15	25	mW	Delta from powering down REFB differential input
PLL On/Off		254	300.5	mW	PLL off to PLL on, normal operation; no reference enabled
One Channel, One Driver		107	132	mW	No LVPECL output on to one LVPECL output on at 2949.12 MHz; same output pair
One Channel, Two Drivers		184	233	mW	No LVPECL output on to two LVPECL outputs on at 2949.12 MHz; same output pair

REFA AND REFB INPUT CHARACTERISTICS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL MODE (REFA, $\overline{\text{REFA}}$; REFB, $\overline{\text{REFB}}$)					Differential mode (can accommodate single-ended input by ac grounding unused input)
Input Frequency	0		500	MHz	Frequencies below ~1 MHz should be dc-coupled; be careful to match self-bias voltage
Input Sensitivity	200			mV p-p	Frequency at 122.88 MHz
Self-Bias Voltage, REFA and REFB	1.52	1.65	1.78	V	Self-bias voltage of REFA and REFB inputs[1]
Self-Bias Voltage, $\overline{\text{REFA}}$ and $\overline{\text{REFB}}$	1.38	1.50	1.61	V	Self-bias voltage of $\overline{\text{REFA}}$ and $\overline{\text{REFB}}$ inputs[1]
Input Resistance, REFA and REFB	4.5	4.7	4.9	kΩ	Self-biased[1]
Input Resistance, $\overline{\text{REFA}}$ and $\overline{\text{REFB}}$	4.9	5.2	5.4	kΩ	Self-biased[1]
DUTY CYCLE					Duty cycle bounds are set by pulse width high and pulse width low
Pulse Width Low	500			ps	
Pulse Width High	500			ps	

[1] The differential pairs of REFA and $\overline{\text{REFA}}$, REFB and $\overline{\text{REFB}}$ self-bias points are offset slightly to avoid chatter on an open input condition.

REFC INPUT CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFC INPUT					
Input Frequency Range			300	MHz	DC-coupled input (not self-biased)
Input High Voltage	2.0			V	
Input Low Voltage			0.8	V	
Input Current		1		µA	
Duty Cycle					Duty cycle bounds are set by pulse width high and pulse width low
Pulse Width Low	1			ns	
Pulse Width High	1			ns	

CLOCK INPUTS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Input Frequency	0		3.6	GHz	Frequencies below ~1 MHz should be dc-coupled; be careful to match self-bias voltage
Input Sensitivity	150			mV p-p	Measured at 3.1 GHz
Input Level			2	V p-p	Larger voltage swings can turn on the protection diodes and can degrade jitter performance
Input Common-Mode Voltage, V_{CM}	1.55	1.64	1.74	V	Self-biased; enables ac coupling
Input Common-Mode Range, V_{CMR}	1.3		1.8	V	With 200 mV p-p signal applied; dc-coupled
Input Resistance	6.7	7	7.4	kΩ	Self-biased
Input Capacitance		2		pF	

PLL CHARACTERISTICS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE/FREQUENCY DETECTOR (PFD)					
PFD Input Frequency			125	MHz	Antibacklash pulse width = 1.3 ns, 2.9 ns
			45	MHz	Antibacklash pulse width = 6.0 ns
CHARGE PUMP (CP)					VDD_CP (Pin 13); V_{CP} is the voltage of the charge pump pin (CP, Pin 14)
I_{CP} Sink/Source					Programmable
High Value	4.5	4.9	5.4	mA	With CPRSET = 5.1 kΩ; higher I_{CP} is possible by changing CPRSET; V_{CP} = VDD_CP/2 V
Low Value	0.57	0.61	0.67	mA	With CPRSET = 5.1 kΩ; lower I_{CP} is possible by changing CPRSET, V_{CP} = VDD_CP/2 V
Absolute Accuracy		2.5		%	V_{CP} = VDD_CP/2 V
CPRSET Range	2.7		10	kΩ	
I_{CP} High Impedance Mode Leakage		3.5		µA	VDD_CP = 5 V
Sink-and-Source Current Matching		2		%	0.5 V < V_{CP} < VDD_CP − 0.5 V
I_{CP} vs. V_{CP}		1.5		%	0.5 V < V_{CP} < VDD_CP − 0.5 V
I_{CP} vs. Temperature		2		%	V_{CP} = VDD_CP/2 V
P DIVIDER (PART OF N DIVIDER)					
Input Frequency P = 1			1500	MHz	
Input Frequency P = 2			3000	MHz	
Input Frequency P = 3			3600	MHz	
Input Frequency P = 4			3600	MHz	
Input Frequency P = 5			3600	MHz	
Input Frequency P = 6			3600	MHz	
B DIVIDER (PART OF N DIVIDER)					
Input Frequency			1500	MHz	B counter input frequency (N Divider input frequency divided by P)
M DIVIDER					
Input Frequency			3600	MHz	
NOISE CHARACTERISTICS					
In-Band Phase Noise of the Charge Pump/ Phase Frequency Detector (In-Band Means Within the LBW of the PLL)					PLL in-band phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log(N) (where N is the value of the N divider)
At 61.44 MHz PFD Frequency		−144		dBc/Hz	
At 122.88 MHz PFD Frequency		−141		dBc/Hz	
PLL Figure of Merit (FOM)		−222		dBc/Hz	Reference slew rate > 0.25 V/ns; FOM +10 log (f_{PFD}) is an approximation of the PFD/CP in-band phase noise (in the flat region) inside the PLL loop bandwidth; when running closed loop, the phase noise, as observed at the VCO output, is increased by 20 log(N)

PLL DIGITAL LOCK DETECT

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PLL DIGITAL LOCK DETECT WINDOW[1]					Signal available at the STATUS and REF_MON pins when selected by appropriate register settings; lock detect window settings can be varied by changing the CPRSET resistor
Lock Threshold (Coincidence of Edges)					Selected by Reg. 0x010[1:0] and Reg. 0x019[1], which is the threshold for transitioning from unlock to lock
Low Range (ABP 1.3 ns, 2.9 ns)		4		ns	Reg. 0x010[1:0] = 00b, 01b,11b; Reg. 0x019[1] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		7		ns	Reg. 0x010[1:0] = 00b, 01b, 11b; Reg. 0x019[1] = 0b
High Range (ABP 6.0 ns)		3.5		ns	Reg. 0x010[1:0] = 10b; Reg. 0x019[1] = 0b
Unlock Threshold (Hysteresis)[1]					Selected by Reg. 0x017[1:0] and Reg. 0x019[1], which is the threshold for transitioning from unlock to lock
Low Range (ABP 1.3 ns, 2.9 ns)		8.3		ns	Reg. 0x010[1:0] = 00b, 01b, 11b; Reg. 0x019[1] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		16.9		ns	Reg. 0x010[1:0] = 00b, 01b, 11b; Reg. 0x019[1] = 0b
High Range (ABP 6.0 ns)		11		ns	Reg. 0x010[1:0] = 10b; Reg. 0x019[1] = 0b

[1] For reliable operation of the digital lock detect, the period of the PFD frequency must be greater than the unlock-after-lock time.

CLOCK OUTPUTS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL CLOCK OUTPUTS					
Output Frequency, Maximum	3.6			GHz	
Rise Time/Fall Time (20% to 80%)		105	162	ps	
Duty Cycle					Input duty cycle = 50/50
M = 1	47	50	53	%	FOUT = 2800 MHz
	45	50	55	%	FOUT < 3000 MHz
M = 2, 4, 6	47	49	51	%	FOUT = 1400 MHz
	45	49	55	%	FOUT < 1500 MHz
M = 3, 5	32	32	33	%	FOUT = 933.33 MHz
Output Differential Voltage, Magnitude	750	830	984	mV	Voltage across pins, output driver static; Termination = 50 Ω to VDD3 − 2 V
Common-Mode Output Voltage	VDD3 − 1.42	VDD3 − 1.37	VDD3 − 1.32	V	Output driver static; VDD3 (Pin 3, Pin 36, Pin 41, Pin 46); Termination = 50 Ω to VDD3 − 2 V

TIMING CHARACTERISTICS

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PROPAGATION DELAY, t_{PECL}, CLKIN TO LVPECL OUTPUT					Termination as shown in Figure 35
For All M Divider Values	461	522	600	ps	High frequency clock distribution configuration
Variation with Temperature		388		fs/°C	
OUTPUT SKEW, LVPECL OUTPUTS[1]					
All LVPECL Outputs		13.5	25.2	ps	Across temperature and VDD per device
Temperature Coefficient		14		fs/°C	
All LVPECL Outputs Across Multiple Parts			144	ps	
OUTPUT SKEW, LVPECL-TO-SYNC_OUT[1]					
SYNC_OUT LVPECL Mode					
All LVPECL Outputs		189	298	ps	Across temperature and VDD per device
Temperature Coefficient		543		fs/°C	
All LVPECL Outputs Across Multiple Parts			417	ps	
SYNC_OUT CMOS Mode					
All LVPECL Outputs		1.64	2.34	ns	Across temperature and VDD per device
All LVPECL Outputs Across Multiple Parts			2.46	ns	
PROPAGATION DELAY, REF TO LVPECL OUTPUT	267	581	924	ps	REF refers to either REFA/$\overline{\text{REFA}}$ or REFB/$\overline{\text{REFB}}$ pairs

[1] The output skew is the difference between any two paths while operating at the same voltage and temperature.

Timing Diagrams

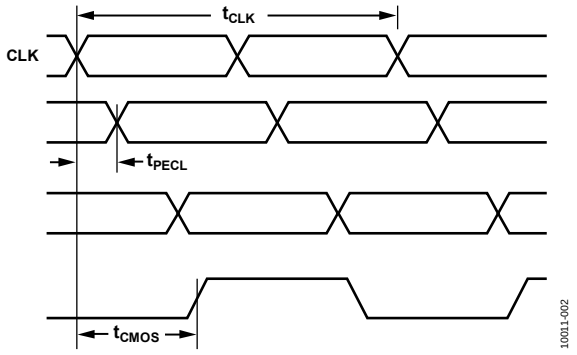


Figure 2. CLK/$\overline{\text{CLK}}$ to Clock Output Timing, M Divider = 1

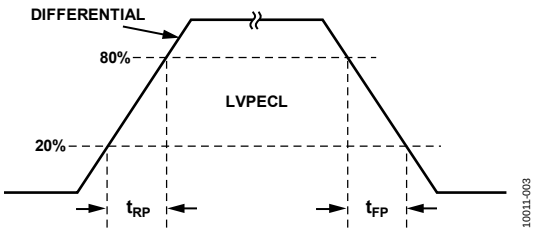


Figure 3. LVPECL Timing, Differential

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING EXTERNAL 122.88 MHZ VCXO)

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup using an external 122.88 MHz VCXO (Crystek CVHD-950); reference = 122.88 MHz; R divider = 1; LBW = 40 Hz
FOUT = 122.88 MHz		107		fs rms	Integration BW = 1 kHz to 40 MHz
		69		fs rms	Integration BW = 12 kHz to 20 MHz
FOUT = 61.44 MHz		108		fs rms	Integration BW = 1 kHz to 20 MHz
		107		fs rms	Integration BW = 12 kHz to 20 MHz

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING EXTERNAL 1475 MHZ VCO)

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup using an external 1475 MHz VCO (Bowei Model MVCO-1475); reference = 122.88 MHz; R divider = 1; PLL LBW = 18 kHz
FOUT = 1474.56 MHz		99		fs rms	Integration BW = 1 kHz to 100 MHz
		77		fs rms	Integration BW = 10 kHz to 100 MHz
		74		fs rms	Integration BW = 10 kHz to 40 MHz
		68		fs rms	Integration BW = 12 kHz to 20 MHz
Reference Sideband Spurs		−93		dBc	±122.88 MHz
FOUT = 245.76 MHz		104		fs rms	Integration BW = 1 kHz to 100 MHz
		87		fs rms	Integration BW = 10 kHz to 100 MHz
		75		fs rms	Integration BW = 12 kHz to 20 MHz
Reference Sideband Spurs		−98		dBc	±122.88 MHz

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup using an external 1475 MHz VCO (Z-Communications CRO1474-LF); reference = 122.88 MHz; R divider = 1; PLL LBW = 8 kHz
FOUT = 1474.56 MHz		72		fs rms	Integration BW = 1 kHz to 100 MHz
		40		fs rms	Integration BW = 10 kHz to 100 MHz
		33		fs rms	Integration BW = 10 kHz to 40 MHz
		28		fs rms	Integration BW = 12 kHz to 20 MHz
Reference Sideband Spurs		−94		dBc	±122.88 MHz
FOUT = 245.76 MHz		83		fs rms	Integration BW = 1 kHz to 100 MHz
		61		fs rms	Integration BW = 10 kHz to 40 MHz
		46		fs rms	Integration BW = 12 kHz to 20 MHz
Reference Sideband Spurs		−93		dBc	±122.88 MHz

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING EXTERNAL 2.05 GHZ VCO)

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup using an external 2.05 MHz VCO (Bowei Model MVCO-2050A); reference = 122.054215 MHz; R divider = 12; PLL LBW = 5 kHz
FOUT = 2048.867 MHz		19		fs rms	Integration BW = 200 kHz to 5 MHz
		21		fs rms	Integration BW = 200 kHz to 10 MHz
		87		fs rms	Integration BW = 12 kHz to 20 MHz
Reference Sideband Spurs		−105		dBc	±10.671MHz

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING EXTERNAL 3 GHZ VCO)

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup using an external 2950 MHz VCO (Z-Communications Model CRO-2950); reference = 122.88 MHz; R divider = 1
FOUT = 2949.12 MHz; PLL LBW = 7 kHz		63		fs rms	Integration BW = 1 kHz to 100 MHz
		38		fs rms	Integration BW = 10 kHz to 100 MHz
		34		fs rms	Integration BW = 10 kHz to 40 MHz
		28		fs rms	Integration BW = 12 kHz to 20 MHz
Reference Sideband Spurs		−99		dBc	±122.88 MHz
FOUT = 1474.56 MHz; PLL LBW = 7 kHz		62		fs rms	Integration BW = 1 kHz to 100 MHz
		36		fs rms	Integration BW = 10 kHz to 100 MHz
		31		fs rms	Integration BW = 10 kHz to 40 MHz
		25		fs rms	Integration BW = 12 kHz to 20 MHz
Reference Sideband Spurs		−100		dBc	±122.88 MHz
FOUT = 491.52 MHz; PLL LBW = 7 kHz		78		fs rms	Integration BW = 1 kHz to 100 MHz
		60		fs rms	Integration BW = 10 kHz to 100 MHz
		44		fs rms	Integration BW = 10 kHz to 40 MHz
		33		fs rms	Integration BW = 12 kHz to 20 MHz
Reference Sideband Spurs		−96		dBc	±122.88 MHz

CLOCK OUTPUT ADDITIVE PHASE NOISE (DISTRIBUTION ONLY; CLOCK INPUT TO DISTRIBUTION OUTPUT, INCLUDING VCO DIVIDER)

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK-TO-LVPECL ADDITIVE PHASE NOISE					Distribution section only; does not include PLL and VCO
CLK = 2949.12 MHz, FOUT = 2949.12 MHz					
Divider = 1					
At 10 Hz Offset		−112		dBc/Hz	
At 100 Hz Offset		−122		dBc/Hz	
At 1 kHz Offset		−133		dBc/Hz	
At 10 kHz Offset		−141		dBc/Hz	
At 100 kHz Offset		−146		dBc/Hz	
At 800 kHz Offset		−148		dBc/Hz	
At 1 MHz Offset		−148		dBc/Hz	
At 10 MHz Offset		−149		dBc/Hz	
At 100 MHz Offset		−151		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK = 1474.56 MHz, FOUT = 1474.56 MHz					
Divider = 1					
At 10 Hz Offset		−114		dBc/Hz	
At 100 Hz Offset		−125		dBc/Hz	
At 1 kHz Offset		−134		dBc/Hz	
At 10 kHz Offset		−144		dBc/Hz	
At 100 kHz Offset		−149		dBc/Hz	
At 800 kHz Offset		−151		dBc/Hz	
At 1 MHz Offset		−151		dBc/Hz	
At 10 MHz Offset		−154		dBc/Hz	
CLK = 122.88 MHz, FOUT = 122.88 MHz					
Divider = 1					
At 10 Hz Offset		−134		dBc/Hz	
At 100 Hz Offset		−145		dBc/Hz	
At 1 kHz Offset		−153		dBc/Hz	
At 10 kHz Offset		−159		dBc/Hz	
At 100 kHz Offset		−161		dBc/Hz	
At 800 kHz Offset		−161		dBc/Hz	
At 1 MHz Offset		−161		dBc/Hz	
At 10 MHz Offset		−161		dBc/Hz	

$\overline{PD}$, $\overline{RESET}$, AND REF_SEL PINS

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CHARACTERISTICS					
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
Logic 1 Current		1		µA	
Logic 0 Current $\overline{PD}$, $\overline{RESET}$		−112		µA	The minus sign indicates that current is flowing out of the AD9525, which is due to the internal pull-up resistor
Logic 0 Current REF_SEL		1		µA	
Capacitance		2		pF	
RESET TIMING					
Pulse Width Low	50			ns	
$\overline{RESET}$ Inactive to Start of Register Programming	100			ns	

STATUS AND REF_MON PINS

Table 18.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS					1 mA output load
Output Voltage High, V_{OH}	2.7			V	
Output Voltage Low, V_{OL}			0.4	V	
MAXIMUM TOGGLE RATE		200		MHz	Applies when mux is set to any divider or counter output or PFD up/down pulse; usually debug mode only; beware that spurs can couple to output when any of these pins is toggling

SERIAL CONTROL PORT

Table 19.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$ (INPUT)					$\overline{CS}$ has an internal 30 kΩ pull-up resistor
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current			2.5	μA	
Input Logic 0 Current		−112		μA	The minus sign indicates that current is flowing out of the AD9525, which is due to the internal pull-up resistor
Input Capacitance		2		pF	
SCLK (INPUT)					SCLK has an internal 30 kΩ pull-down resistor
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		112		μA	
Input Logic 0 Current			1	μA	
Input Capacitance		2		pF	
SDIO (WHEN INPUT)					
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		10		nA	
Input Logic 0 Current		20		nA	
Input Capacitance		2		pF	
SDIO, SDO (OUTPUTS)					1 mA load current
Output Logic 1 Voltage	2.7			V	
Output Logic 0 Voltage			0.4	V	
TIMING					
Clock Rate (SCLK, $1/t_{SCLK}$)			31	MHz	
Pulse Width High, t_{HIGH}	16			ns	
Pulse Width Low, t_{LOW}	16			ns	
SDIO to SCLK Setup, t_{DS}	2			ns	
SCLK to SDIO Hold, t_{DH}	1.1			ns	
SCLK to Valid SDIO and SDO, t_{DV}			12	ns	
$\overline{CS}$ to SCLK Setup and Hold, t_S, t_H	2			ns	
$\overline{CS}$ Minimum Pulse Width High, t_{PWH}	3.6			ns	

ABSOLUTE MAXIMUM RATINGS

Table 20.

Parameter	Rating
VDD3 to GND	−0.3 V to +3.6 V
VDD_CP, CP to GND	−0.3 V to +5.8 V
REFA, $\overline{\text{REFA}}$, REFB, $\overline{\text{REFB}}$, REFC to GND	−0.3 V to VDD3 + 0.3 V
OUT_RSET to GND	−0.3 V to VDD3 + 0.3 V
CP_RSET to GND	−0.3 V to VDD3 + 0.3 V
CLKIN, $\overline{\text{CLKIN}}$ to GND	−0.3 V to VDD3 + 0.3 V
CLKIN to $\overline{\text{CLKIN}}$	−1.2 V to +1.2 V
SCLK, SDIO, SDO, $\overline{\text{CS}}$ to GND	−0.3 V to VDD3 + 0.3 V
OUT0, $\overline{\text{OUT0}}$, OUT1, $\overline{\text{OUT1}}$, OUT2, $\overline{\text{OUT2}}$, OUT3, $\overline{\text{OUT3}}$, OUT4, $\overline{\text{OUT4}}$, OUT5, $\overline{\text{OUT5}}$, OUT6, $\overline{\text{OUT6}}$, OUT7, $\overline{\text{OUT7}}$, SYNC_OUT, $\overline{\text{SYNC\_OUT}}$ to GND	−0.3 V to VDD3 + 0.3 V
$\overline{\text{RESET}}$, $\overline{\text{PD}}$, STATUS, REF_MON to GND	−0.3 V to VDD3 + 0.3 V
Junction Temperature[1]	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 sec)	300°C

[1] See Table 21 for θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 21. Thermal Resistance (Simulated)

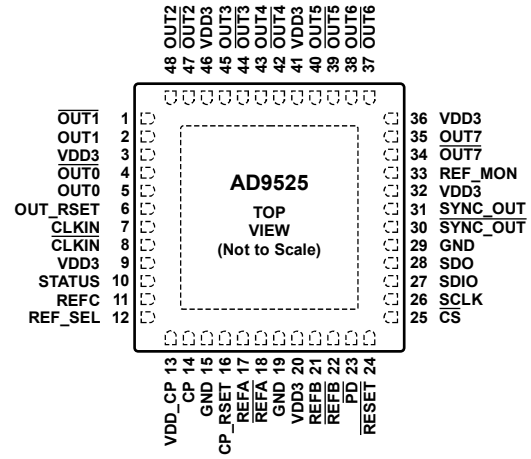
Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Ψ_{JT}[1, 2]	Unit
48-Lead LFCSP	0	27.3	2.1	14.7	0.2	°C/W
	1.0	23.9			0.3	°C/W
	2.5	21.4			0.4	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD IS A GROUND CONNECTION ON THE CHIP THAT MUST BE SOLDERED TO THE ANALOG GROUND OF THE PCB TO ENSURE PROPER FUNCTIONALITY AND HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH BENEFITS.

10011-004

Figure 4. Pin Configuration

Table 22. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	$\overline{\text{OUT1}}$	O	LVPECL Complementary Output 1.
2	OUT1	O	LVPECL Output 1.
3	VDD3	P	3.3 V Power Supply for Channel OUT0 and Channel OUT1.
4	$\overline{\text{OUT0}}$	O	LVPECL Complementary Output 0.
5	OUT0	O	LVPECL Output 0.
6	OUT_RSET	O	Clock Distribution Current Set Resistor. Connect a 4.12 kΩ resistor from this pin to GND.
7	CLKIN	I	Along with $\overline{\text{CLKIN}}$, this pin is the differential input for the clock distribution section.
8	$\overline{\text{CLKIN}}$	I	Along with CLKIN, this pin is the differential input for the clock distribution section. If a single-ended input is connected to the CLKIN pin, connect a 0.1 µF bypass capacitor from $\overline{\text{CLKIN}}$ to ground.
9	VDD3	P	3.3 V Power Supply for CLK Inputs, M Divider, and Output Distribution.
10	STATUS	O	Lock Detect and Other Status Signals.
11	REFC	I	Reference Clock Input C. This pin is a CMOS input for the PLL reference.
12	REF_SEL	I	Reference Input Select. Logic high = REFB. No internal pull-up or pull-down resistor on this pin.
13	VDD_CP	P	Power Supply for Charge Pump (CP). VDD3 < VDD_CP < 5.0 V. VDD_CP must still be connected to 3.3 V if the PLL is not used.
14	CP	O	Charge Pump (Output). This pin connects to an external loop filter. This pin can be left unconnected if the PLL is not used.
15	GND	GND	Ground for Charge Pump VDD_CP Supply. Connect to ground.
16	CP_RSET	O	Charge Pump Current Set Resistor. Connect a 5.1 kΩ resistor from this pin to GND. This resistor can be omitted if the PLL is not used.
17	REFA	I	Reference Clock Input A. Along with $\overline{\text{REFA}}$, this pin is the differential input for the PLL reference.
18	$\overline{\text{REFA}}$	I	Reference Clock Input A. Along with REFA, this pin is the differential input for the PLL reference.
19	GND	GND	Ground for PLL Power Supply. Connect to ground.
20	VDD3	P	3.3 V Power Supply for PLL.
21	REFB	I	Reference Clock Input B. Along with $\overline{\text{REFB}}$, this pin is the differential input for the PLL reference.
22	$\overline{\text{REFB}}$	I	Reference Clock Input B. Along with REFB, this pin is the differential input for the PLL reference.
23	$\overline{\text{PD}}$	I	Chip Power-Down, Active Low. This pin has an internal 30 kΩ pull-up resistor.
24	$\overline{\text{RESET}}$	I	Chip Reset, Active Low. This pin has an internal 30 kΩ pull-up resistor.
25	$\overline{\text{CS}}$	I	Serial Control Port Chip Select; Active Low. This pin has an internal 30 kΩ pull-up resistor.
26	SCLK	I	Serial Control Port Clock Signal. This pin has an internal 30 kΩ pull-down resistor.
27	SDIO	I	Serial Control Port Bidirectional Serial Data In/Out.

Pin No.	Mnemonic	Type	Description
28	SDO	I	Serial Control Port Unidirectional Serial Data Out.
29	GND	GND	Connect to ground.
30	$\overline{\text{SYNC\_OUT}}$	O	LVPECL Complementary Output for Programmable Sync Signal.
31	SYNC_OUT	O	LVPECL Output for Programmable Sync Signal.
32	VDD3	P	Power Supply for SYNC_OUT Driver.
33	REF_MON	O	Reference Monitor (Output). This pin has multiple selectable outputs.
34	$\overline{\text{OUT7}}$	O	LVPECL Complementary Output 7.
35	OUT7	O	LVPECL Output 7.
36	VDD3	P	3.3 V Power Supply for Channel OUT6 and Channel OUT7.
37	$\overline{\text{OUT6}}$	O	LVPECL Complementary Output 6.
38	OUT6	O	LVPECL Output 6.
39	$\overline{\text{OUT5}}$	O	LVPECL Complementary Output 5.
40	OUT5	O	LVPECL Output 5.
41	VDD3	P	3.3 V Power Supply for Channel OUT4 and Channel OUT5.
42	$\overline{\text{OUT4}}$	O	LVPECL Complementary Output 4.
43	OUT4	O	LVPECL Output 4.
44	$\overline{\text{OUT3}}$	O	LVPECL Complementary Output 3.
45	OUT3	O	LVPECL Output 3.
46	VDD3	P	3.3 V Power Supply for Channel OUT2 and Channel OUT3.
47	$\overline{\text{OUT2}}$	O	LVPECL Complementary Output 2.
48	OUT2	O	LVPECL Output 2.
EP	EP, GND	GND	Exposed Paddle. The exposed pad is a ground connection on the chip that must be soldered to the analog ground of the PCB to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.

TYPICAL PERFORMANCE CHARACTERISTICS

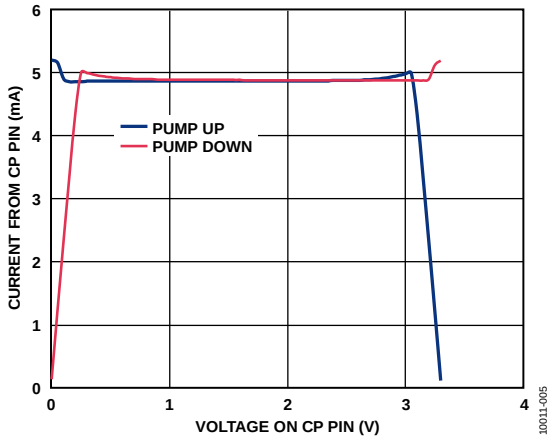


Figure 5. Charge Pump Characteristics at VDD_CP = 3.3 V

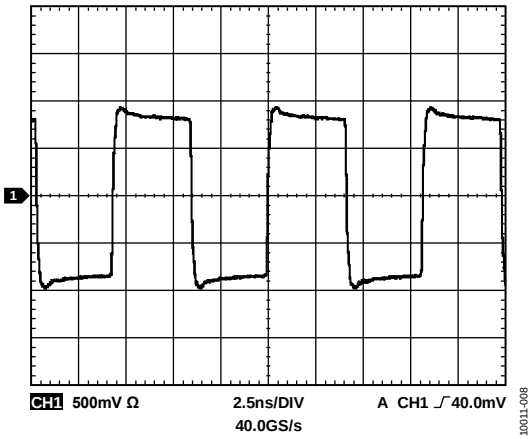


Figure 8. LVPECL Output (Differential) at 122.88 MHz

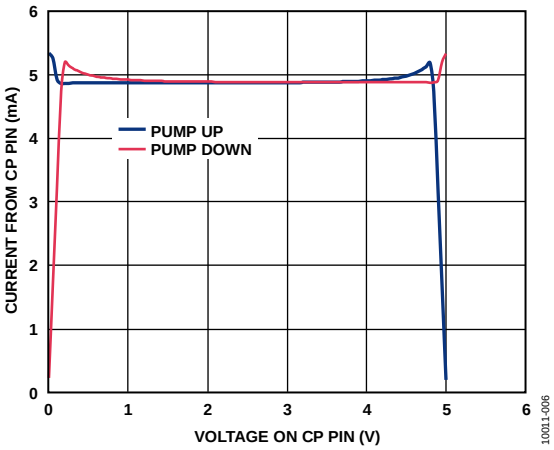


Figure 6. Charge Pump Characteristics at VDD_CP = 5.0 V

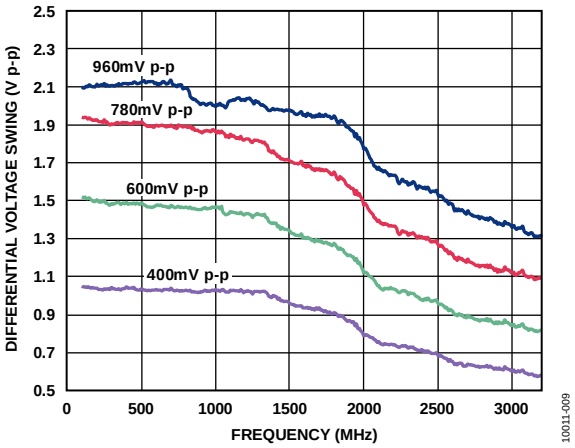


Figure 9. LVPECL Differential Voltage Swing vs. Frequency

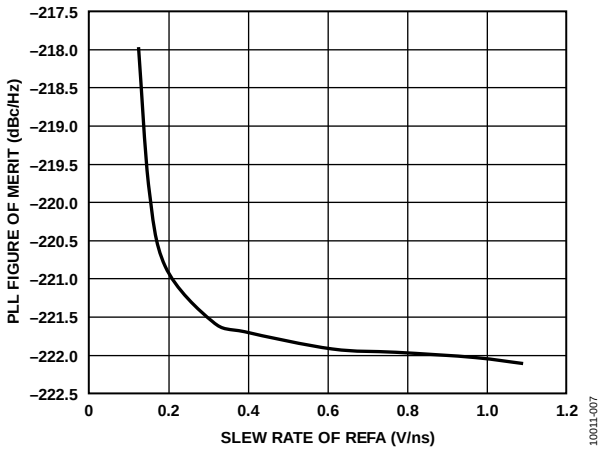


Figure 7. PLL Figure of Merit (FOM) vs. Slew Rate at REFA

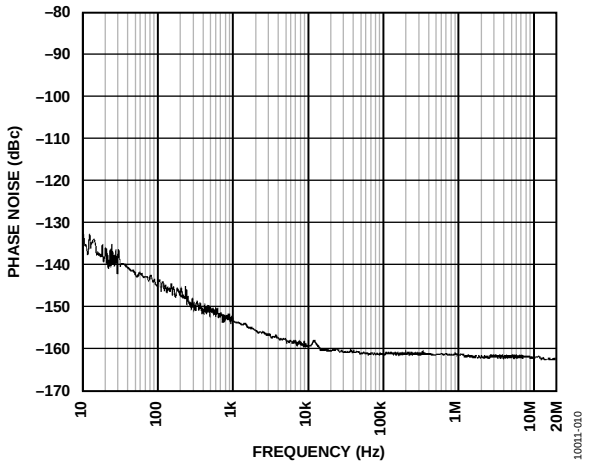


Figure 10. Additive (Residual) Phase Noise, CLK-to-LVPECL at 122.88 MHz, Divide-by-1

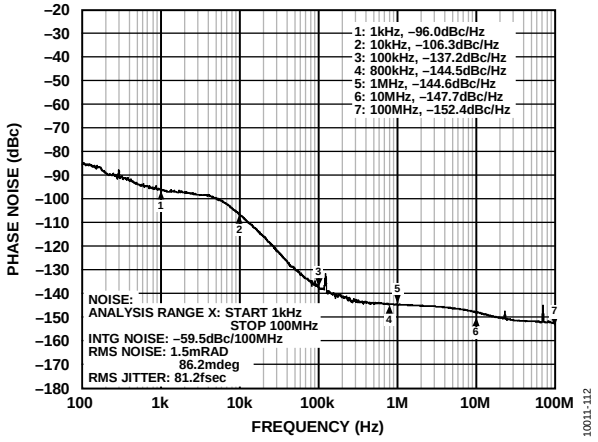


Figure 13. Phase Noise (Absolute), External VCO (Z-Communications Model CRO-2950) at 2949.12 MHz; PFD = 122.88 MHz; LBW = 8 kHz; LVPECL Output = 2949.12 MHz

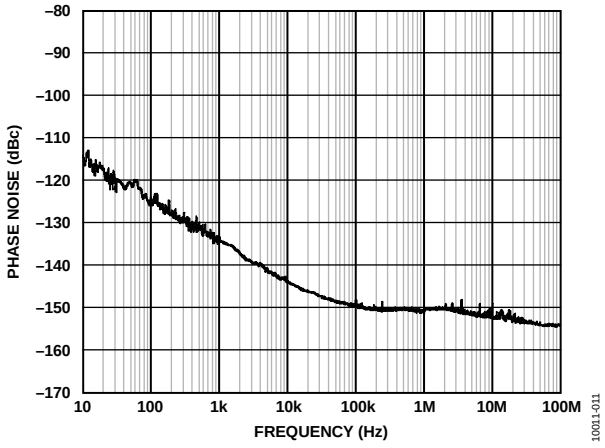


Figure 11. Additive (Residual) Phase Noise, CLK-to-LVPECL at 1500 MHz, Divide-by-1

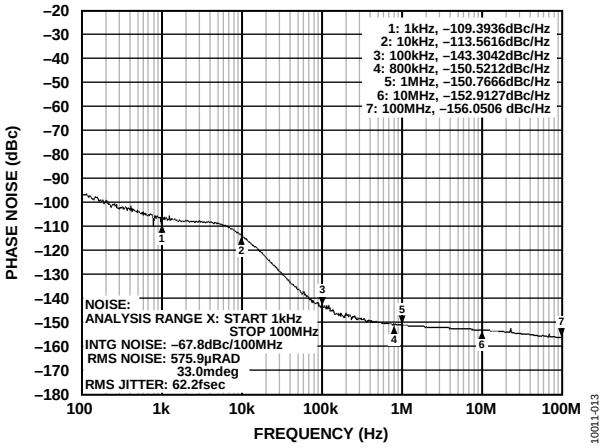


Figure 14. Phase Noise (Absolute), External VCO (Z-Communications Model CRO-2950) at 2949.12 MHz; PFD = 122.88 MHz; LBW = 8k Hz; LVPECL Output = 1474.56 MHz

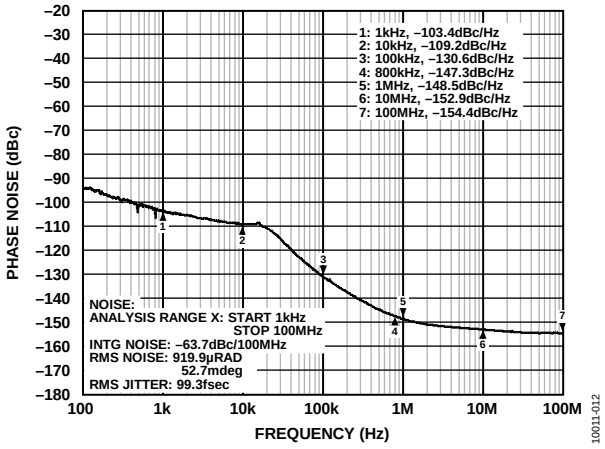


Figure 12. Phase Noise (Absolute), External VCO (Bowei Model MVCO-1475) at 1474.56 MHz; PFD = 122.88 MHz; LBW = 18 kHz; LVPECL Output = 1474.56 MHz

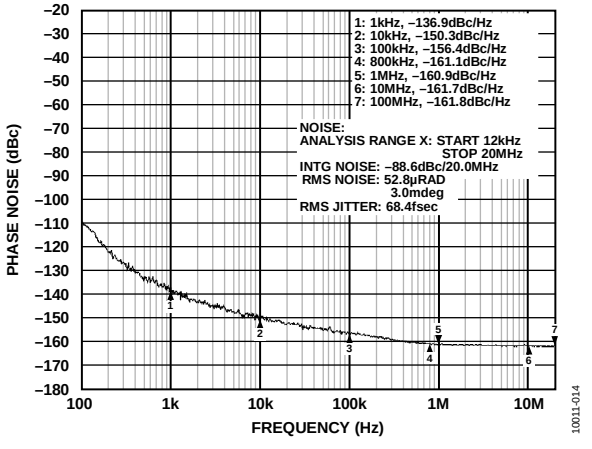


Figure 15. Phase Noise (Absolute), External VCXO (122.88 MHz VCXO) (Crystek CVHD-950); Reference = 122.88 MHz; R Divider = 1); LBW = 40 Hz; LVPECL Output = 122.88 MHz

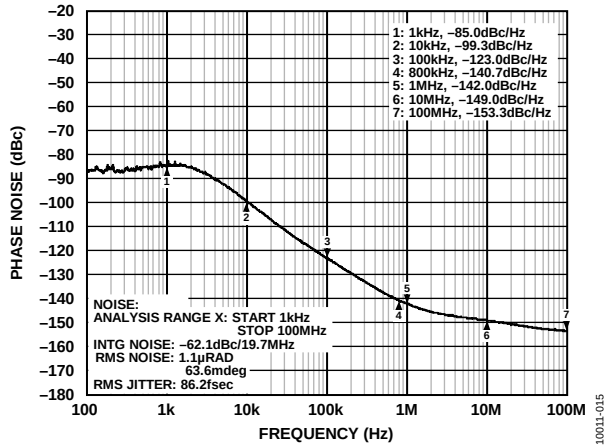


Figure 16. Phase Noise (Absolute), External VCO 2.05 GHz VCO (Bowei Model MVCO-2050A); at 2050 MHz; Reference = 122.054215 MHz; R Divider = 12

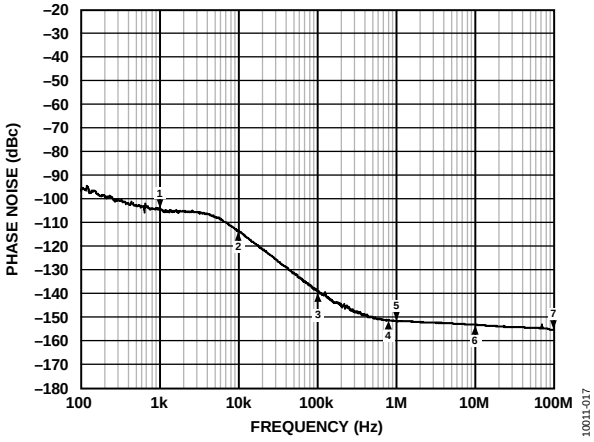


Figure 17. Phase Noise (Absolute), External VCO (Z-Communications CRO1474-LF) at 1474.56 MHz; PFD = 122.88 MHz; LBW = 15 kHz; LVPECL Output = 1474.56 MHz

TERMINOLOGY

Phase Jitter and Phase Noise

An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as being Gaussian (normal) in distribution.

This phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in decibels) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval; it can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on the performance of ADCs, DACs, and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings varies. In a square wave, the time jitter is a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the signal-to-noise ratio (SNR) and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise

Additive phase noise is the amount of phase noise that can be attributed to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted, making it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise. When there are multiple contributors to phase noise, the total is the square root of the sum of squares of the individual contributors.

Additive Time Jitter

Additive time jitter is the amount of time jitter that can be attributed to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

DETAILED BLOCK DIAGRAM

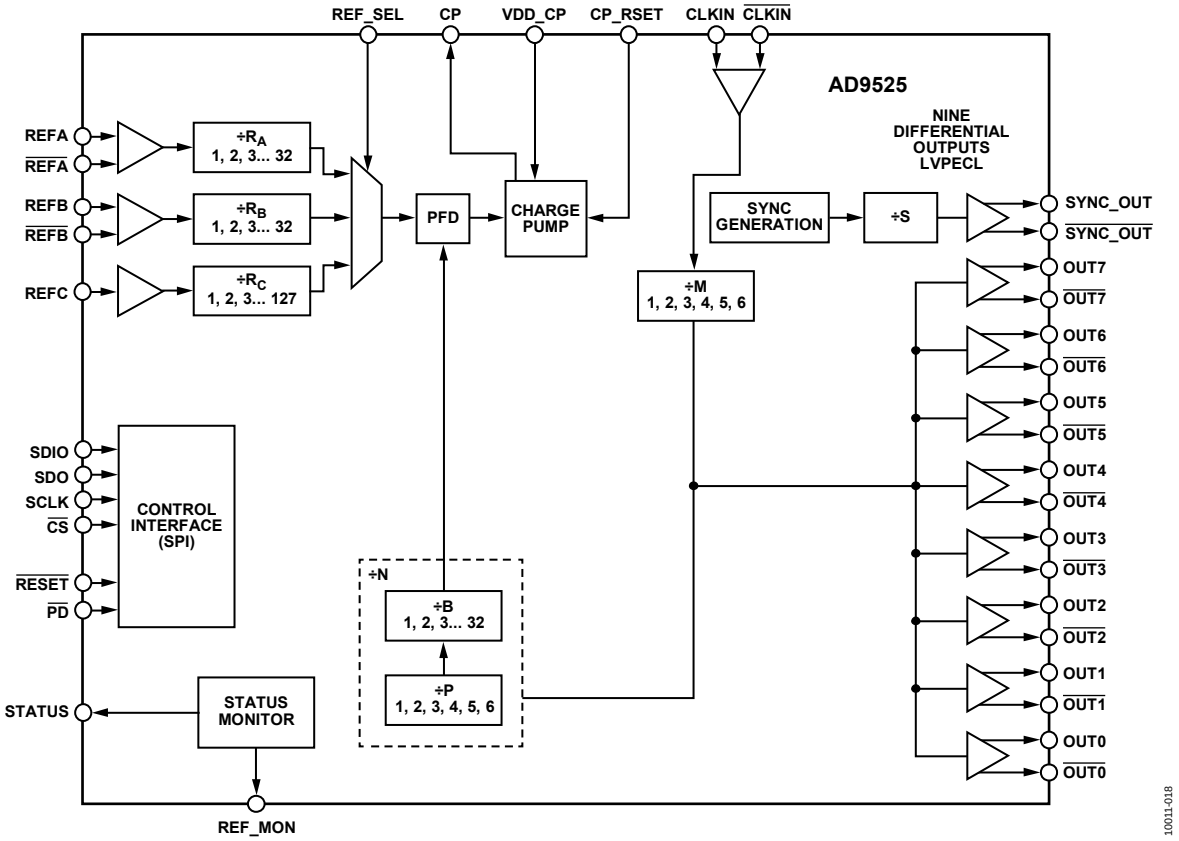


Figure 18. Detailed Block Diagram

THEORY OF OPERATION

The AD9525 PLL is useful for generating clock frequencies from a supplied reference frequency. In addition, the PLL can be used to clean up jitter and phase noise on a noisy reference. The exact choice of PLL parameters and loop dynamics is application specific. The flexibility and depth of the AD9525 PLL allow the part to be tailored to function in many different applications and signal environments.

The AD9525 includes on-chip PLL blocks that can be used with an external VCO or VCXO to create a complete phase-locked loop. The PLL requires an external loop filter, which usually consists of a small number of capacitors and resistors. The configuration and components of the loop filter help to establish the loop bandwidth and stability of the PLL. The external loop filter that must be connected between CP and the tuning pin of the VCO/VCXO. This loop filter determines the loop bandwidth and stability of the PLL. Make sure to select the proper PFD polarity for the VCO/VCXO being used.

The AD9525 can also be configured as a clock distribution by shutting down the PLL and using CLKIN and $\overline{\text{CLKIN}}$ as the input. The M divider can be used to divide the input frequency down to the desired output frequency to each of the eight LVPECL outputs.

CONFIGURATION OF THE PLL

Configuration of the PLL is accomplished by programming the various settings for the R divider, N divider, PFD polarity, and charge pump current. The combination of these settings and the loop filter determines the PLL loop bandwidth and PLL stability. These are managed through programmable register settings and by the design of the external loop filter.

Successful PLL operation and satisfactory PLL loop performance are highly dependent on proper configuration of the PLL settings, and the design of the external loop filter is crucial to the proper operation of the PLL.

ADIsimCLK™ is a free program that can help with the design and exploration of the capabilities and features of the AD9525, including the design of the PLL loop filter. The AD9516 model found in ADIsimCLK Version 1.2 can also be used for modeling the AD9525 loop filter. It is available at www.analog.com/clocks.

Phase Frequency Detector (PFD)

The PFD takes inputs from the R divider and the N divider and produces an output proportional to the phase and frequency difference between them. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. The antibacklash pulse width is set by Register 0x010[1:0].

An important limit to keep in mind is the maximum frequency allowed into the PFD. The maximum input frequency into the PFD is a function of the antibacklash pulse setting, as specified in the phase/frequency detector (PFD) parameter in Table 7.

Charge Pump (CP)

The charge pump is controlled by the PFD. The PFD monitors the phase and frequency relationship between its two inputs and tells the CP to pump up or pump down to charge or discharge the integrating node (part of the loop filter). The integrated and filtered CP current is transformed into a voltage that drives the tuning node of the external VCO to move the VCO frequency up or down. The CP can be set for high impedance (allows holdover operation), for normal operation (attempts to lock the PLL loop), for pump-up, or for pump-down (test modes). The CP current is programmable in eight steps. The exact value of the CP current LSB is set by the CPRSET resistor, which is nominally 5.1 kΩ. The actual LSB current can be calculated by CP_LSB = 3.06/CPRSET.

PLL External Loop Filter

An example of an external loop filter for the PLL is shown in Figure 19. A loop filter must be calculated for each desired PLL configuration. The values of the components depend on the VCO frequency, the K_{VCO}, the PFD frequency, the charge pump current, the desired loop bandwidth, and the desired phase margin. The loop filter affects the phase noise, the loop settling time, and the loop stability. A basic knowledge of PLL theory is necessary for understanding loop filter design. ADIsimCLK can help with the calculation of a loop filter according to the application requirements.

PLL Reference Inputs

The AD9525 features two fully differential PLL reference input circuits. The differential inputs are self-biased, allowing for easy ac coupling of input signals. All PLL reference inputs are off by default. The self-bias level of the two sides is offset slightly to prevent chattering of the input buffer when the reference is ac coupled and is slow or missing. The input offset increases the voltage swing required of the driver to overcome the offset. The input frequency range and common-mode voltages for the reference inputs are specified in Table 4.

The reference input receiver is powered down when the PLL is powered down. It is possible to dc couple to these inputs. If the differential reference input is driven by a single-ended signal, the unused side ($\overline{\text{REFA}}$ or $\overline{\text{REFB}}$) should be decoupled via a suitable capacitor to a quiet ground.

The AD9525 provides a third single-ended CMOS reference input referred to as REFC.

Reference Switchover

The AD9525 supports two separate differential reference inputs. Manual switchover is performed between these inputs either through Register 0x01A or by using the REF_SEL pin. This feature supports networking and other applications that require redundant references.

Manual switchover requires that a clock be present on the reference input that is being switched to or that the switchover deglitching feature be disabled (Register 0x01A[4]).

Reference Dividers R

The reference inputs are routed to their respective divider, R. R can be set to any value from 1 to 32 (Both R = 0 and R = 1 give divide-by-1.).

The division is set by the values of R_{LOW} and R_{HIGH}. The divider can be bypassed (equivalent to divide-by-1, divider circuit is powered down) by setting the bypass bit.

For each R divider, the frequency division (R_X) is set by the values of R_{LOW} and R_{HIGH} (four bits each, representing Decimal 0 to Decimal 15), where

$$Number\ of\ Low\ Cycles = R_{LOW} + 1$$

$$Number\ of\ High\ Cycles = R_{HIGH} + 1$$

The high and low cycles are cycles of the clock signal currently routed to the input of the R.

When a divider is bypassed, $R_X = 1$.

Otherwise, $R_X = (R_{HIGH} + 1) + (R_{LOW} + 1) = R_{HIGH} + R_{LOW} + 2$. This allows each reference divider to divide by any integer from 1 to 32.

The output of the R divider goes to a mux to select one of the references to the PFD inputs. The frequency applied to the PFD must not exceed the maximum allowable frequency, which depends on the antibacklash pulse setting (see Table 7).

The R divider has its own reset. The R divider can also be reset using the shared reset bit of the R and B counters. This reset bit is not self-clearing.

The R divider in the REFC path has a division ratio programmable from 1 to 127.

VCO/VCXO, M and N Feedback Dividers

The feedback division is the product of the M divider and the N divider. The N divider is a combination of a prescaler (P) and a B divider.

$$f_{VCO} = (f_{REF}/R) \times N \times M$$

where:
M =1, 2, 3, 4, 5, or 6.
$N = (P \times B)$.
P =1, 2, 3, 4, 5, or 6.
B = 1, 2, 3, … or 32.

M Divider

The M divider is a fixed divide (FD) of 1, 2, 3, 4, 5, or 6.

The maximum input frequency to the M counter is reflected in the maximum CLKIN input frequency specified in Table 6.

The M divider provides frequency division between the CLKIN input and the N feedback divider and clock distribution output channels.

The M divider can also be set to static, which is useful for applications where the only desired output frequency is the CLK input frequency.

P Divider

The P divider is a fixed divide (FD) of 1, 2, 3, 4, 5 or 6.

The maximum input frequency to the P counter is reflected in the maximum CLKIN input frequency specified in Table 6.

B Divider

The B divider is a fixed divide (FD) of 1, 2, 3, …or 32.

The maximum input frequency to the B counter is ~1500 MHz, as specified in Table 7. This is the prescaler input frequency (external VCO or CLKIN) divided by the P and M counters. For example, M = 1 and P = 1 mode is not allowed if the external VCO frequency is greater than 1500 MHz because the frequency going to the B divider is too high.

The division is set by the values of B_{LOW} and B_{HIGH}. The divider can be bypassed (equivalent to divide-by-1, divider circuit is powered down) by setting the bypass bit.

The frequency division, B_X, is set by the values of B_{LOW} and B_{HIGH} (four bits each, representing Decimal 0 to Decimal 15), where

$$Number\ of\ Low\ Cycles = B_{LOW} + 1$$

$$Number\ of\ High\ Cycles = B_{HIGH} + 1$$

The high and low cycles are cycles of the clock signal currently routed to the input of the B divider.

When a divider is bypassed, $B_X = 1$.

Otherwise, $B_X = (B_{HIGH} + 1) + (B_{LOW} + 1) = B_{HIGH} + B_{LOW} + 2$.

Although manual reset is not normally required, the B counter has its own reset bit. Note that this reset bit is not self-clearing.

Digital Lock Detect (DLD)

By selecting the proper output through the mux on each pin, the DLD function is available at the STATUS and REF_MON pins. The digital lock detect circuit indicates a lock when the time difference of the rising edges at the PFD inputs is less than a specified value (the lock threshold). The loss of a lock is indicated when the time difference exceeds a specified value (the unlock threshold). Note that the unlock threshold is wider than the lock threshold, which allows some phase error in excess of the lock window to occur without chattering on the lock indicator.

The lock detect window timing depends on the value of the CPRSET resistor, as well as three settings: the digital lock detect window bit (Register 0x019[1]), the antibacklash pulse width bits (Register 0x010[1:0], see Table 8), and the lock detect counter bits (Register 0x019[3:2]). The lock and unlock detection values in Table 8 are for the nominal value of CPRSET = 5.11 kΩ. Doubling the CPRSET value to 10 kΩ doubles the values in Table 8.

A lock is not indicated until there is a programmable number of consecutive PFD cycles with a time difference that is less than the lock detect threshold. The lock detect circuit continues to indicate a lock until a time difference greater than the unlock threshold occurs on a single subsequent cycle. For the lock detect to work properly, the period of the PFD frequency must be greater than the unlock threshold. The number of consecutive PFD cycles required for a lock is programmable (Register 0x018[6:5]).

Note that, in certain low (<500 Hz) loop bandwidth, high phase margin cases, it is possible that the DLD can chatter during acquisition. This is normal and occurs because the PFD inputs are moving slowly in and out of the lock/unlock window during PLL loop settling. Adjustment of the lock detect counter setting (Register 0x019[3:2]) can suppress this behavior.

External VCXO/VCO Clock Input (CLKIN/$\overline{\text{CLKIN}}$)

This differential input is used to drive the AD9525 clock distribution section. The pins are internally self-biased, and the input signal should be ac-coupled via capacitors.

The CLKIN/$\overline{\text{CLKIN}}$ input can be used either as a distribution only input (with the PLL off) or as a feedback input for an external VCO/VCXO using the internal PLL. Sample configurations are illustrated in Figure 19 through Figure 21. Refer to the manufacturer's recommendation for VCO terminations; a T or PI attenuator is often recommended, as illustrated in Figure 19.

For operation using a CMOS input, an external resistive divider is required to limit the swing on CLKIN (see Table 6 for the maximum input rating).

Status Monitor

The AD9525 contains three frequency status monitors that are used to indicate if the PLL reference (or references, in the case of single-ended mode) and the VCO have fallen below a threshold.

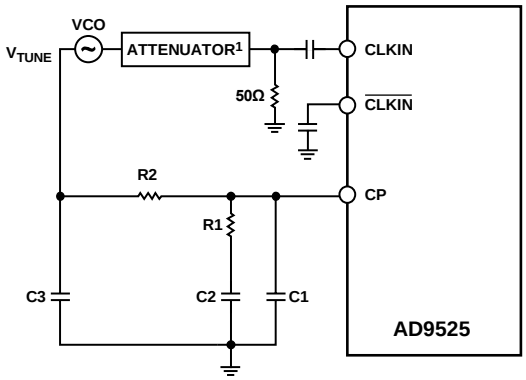


Figure 19. CLKIN Configured as Single-Ended VCO

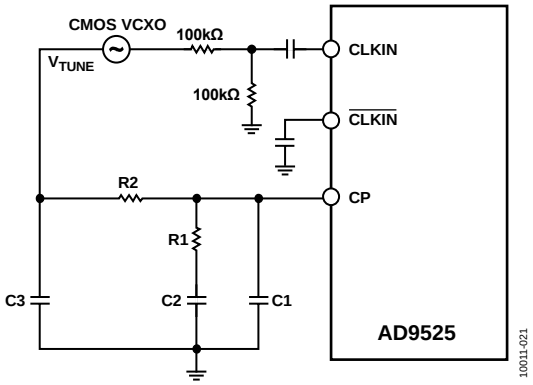


Figure 20. CLKIN Configured as Single-Ended CMOS VCXO

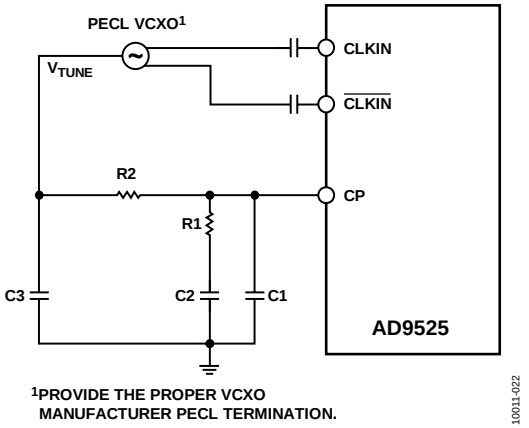


Figure 21. CLKIN Configured as Differential LVPECL VCXO

CLOCK DISTRIBUTION

The AD9525 can be used only as a clock fan out buffer by disabling the PLL circuit blocks except for the clock distribution section. The clock distribution consists of eight LVPECL clock output drivers that share a common M divider. See the M Divider section for more information on the common M divider.

Duty Cycle and Duty-Cycle Correction

The duty cycle of the clock signal at the output of a driver is a result of either or both of the following conditions:

- The CLKIN, $\overline{\text{CLKIN}}$ input duty cycle. If the CLKIN, $\overline{\text{CLKIN}}$ input is routed directly to the output, the duty cycle of the output is the same as the CLKIN, $\overline{\text{CLKIN}}$ input.
- The M divider value. An odd M divider value results in a non-50% duty cycle.

Table 23.Typical Output Duty Cycle with M Divider ≠ 1

M Divider	Output Duty Cycle (%)
Even	50
Odd = 3	33.3
Odd = 5	40

LVPECL Output Drivers

The LVPECL differential voltage (V_{OD}) is selectable (from ~400 mV to 960 mV (see Bit 2 and Bit 1 in Register 0x0F0 to Register 0x0F7).

The LVPECL output polarity can be set as noninverting or inverting, which allows for the adjustment of the relative polarity of outputs within an application without requiring a board layout change. Each LVPECL output can be powered down or powered up, as needed. Because of the architecture of the LVPECL output stages, there is the possibility of electrical overstress and breakdown under certain power-down conditions.

For this reason, the LVPECL outputs have two power-down modes: total power-down and safe power-down. The primary power-down mode is the safe power-down mode. This mode continues to protect the output devices while powered down. There are three ways to activate safe power-down mode: individually set the power-down bit for each driver, power down an individual output channel, or activate sleep mode.

In total power-down mode 0x0230[1] = 1 (power down distribution reference). This mode must not be used if there is an external voltage bias network (such as Thevenin equivalent termination) on the output pins that will cause a dc voltage to appear at the powered down outputs. However, total power-down mode is allowed when the LVPECL drivers are terminated using only pull-down resistors.

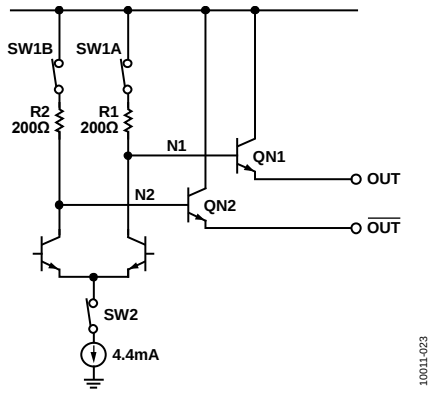


Figure 22. LVPECL Output Simplified Equivalent Circuit

SYNC_OUT

SYNC_OUT provides one LVPECL output or two CMOS output signal that can used to reset or synchronize a converter. SYNC_OUT functionality block diagram is shown in Figure 23. The SYNC_OUT signal is derived from the PLL phase detector reference input clock or feedback (N-divider) clock. A programmable 16-bit S divider further divides the selected reference clock. There are three different modes of operation for SYNC_OUT: single shot, periodic, or pseudorandom. SYNC_OUT is retimed to the high speed clock.

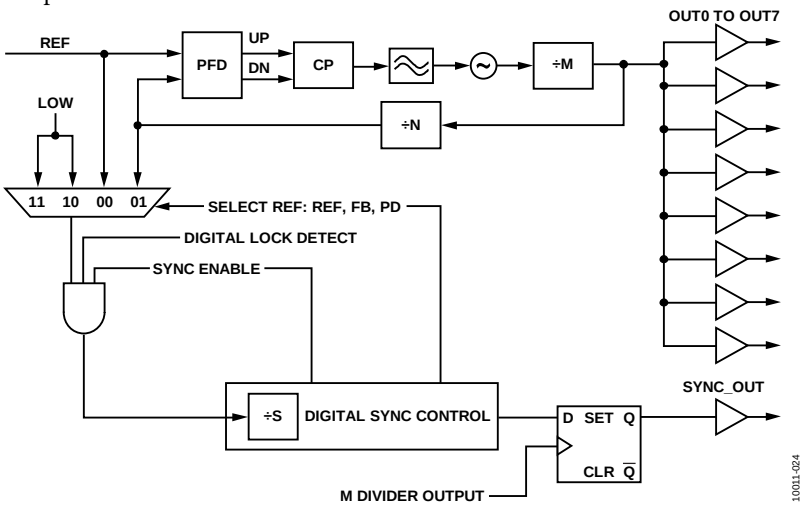


Figure 23. SYNC_OUT Functional Diagram

Single Shot Mode

In single shot mode one sync pulse occurs after writing SYNC ENABLE 0x192[4] = 1. An IO_UPDATE is required to complete a register write. The width of the sync pulse is determined by the value of the S divider. A divider value of 0x0000 allows a pulse whose width is equal to one half period of the phase detector rate. A divider value of 0x0001 allows a pulse whose width is equal to two half periods of the phase detector rate. In single shot mode, the sync enable bit is self-clearing and the sync circuits are ready to receive another sync enable.

Periodic Mode

In periodic mode, the pulse is continuous until SYNC ENABLE is cleared by a register writing SYNC ENABLE 0x192[4] = 0. An IO_UPDATE is required to complete a register write. The width of the sync pulse is equal to one half period of the phase detector rate. The pulse repetition rate is determined by the value of the S divider. A divider value of 0x0000 allows a pulse rate equal to the phase detector rate. A divider value of 0x0001 allows a pulse rate equal to two half periods of the phase detector rate. The SYNC_OUT signal is resampled with the OUT clock to ensure time alignment and minimum output skew. There is a possibility in periodic mode that the SYNC_OUT could slip one half cycle of the OUT clock period.

Pseudorandom Mode

Pseudorandom mode is similar to periodic mode but the pulse is a PN17 sequence that is continuous until SYNC ENABLE is cleared by a register writing SYNC ENABLE 0x192[4] = 0. An IO_UPDATE is required to complete a register write. The width of the sync pulse is equal to one half period the phase detector rate. The pulse repetition rate is determined by the value of the S divider. A divider value of 0x0000 allows a pulse rate equal to the phase detector rate. A divider value of 0x0001 allows pulse rate equal to two half the phase detector rate.

SYNC_OUT Programming

The procedure to configure the SYNC_OUT depends on the logic requirement of the converters that require synchronization. Analog Devices, Inc., converters are synchronized on the rise edge of the SYNC pulse.

SYNC_OUT CMOS Driver

The user can also configure the LVPECL SYNC_OUT as a pair of CMOS outputs. When the output is configured as CMOS, CMOS Output A and CMOS Output B are automatically turned on. Either CMOS Output A or Output B can be turned on or off independently. The user can also select the relative polarity of the CMOS outputs for any combination of inverting and noninverting (see Register 0x0F9). The user can power down each CMOS output as needed to save power. The CMOS driver is in tristate when it is powered down.

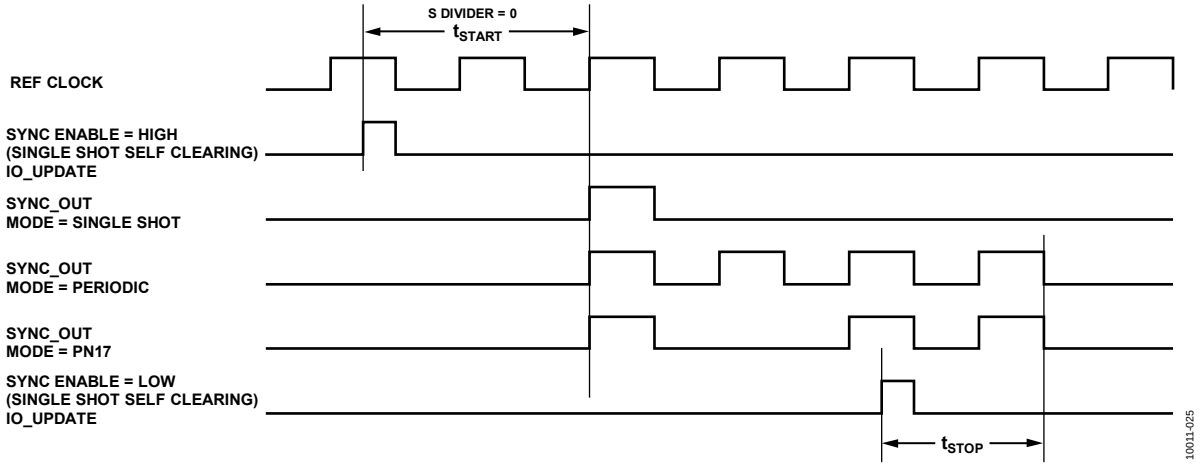


Figure 24. SYNC Output Timing

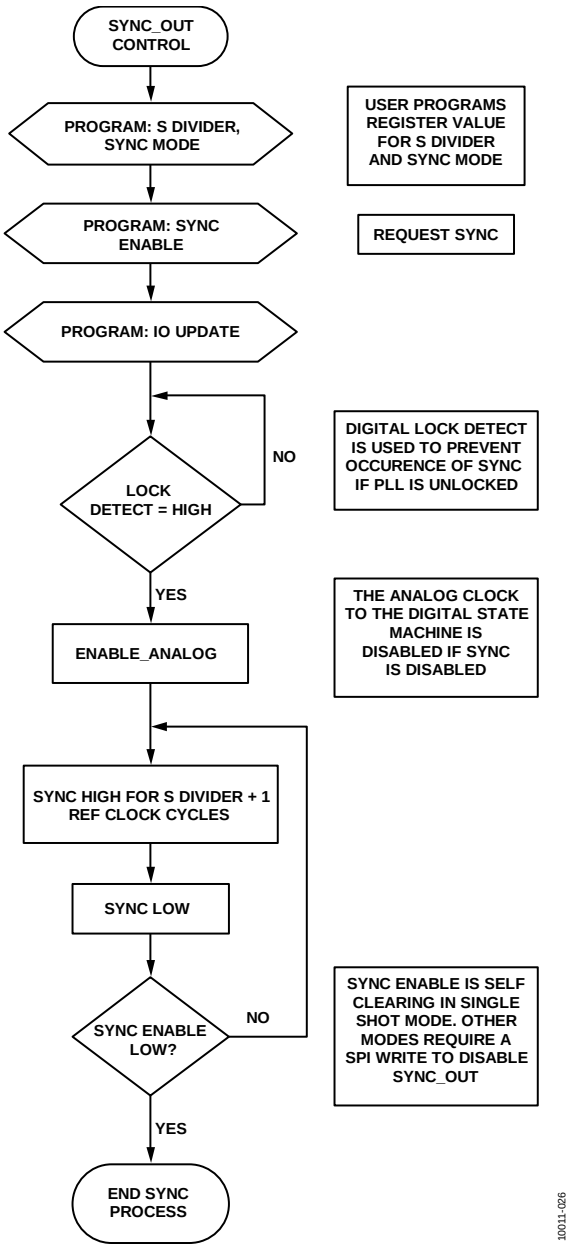


Figure 25. SYNC_OUT Flowchart

RESET MODES

The AD9525 has a power-on reset (POR) and several other ways to apply a reset condition to the chip.

Power-On Reset

During chip power-up, a power-on reset pulse is issued when VDD reaches ~2.6 V (<2.8 V) and restores the chip to the default on-chip setting. It takes ~70 ms for the outputs to begin toggling after the power-on reset pulse signal is internally generated. The default power-on state of the AD9525 is configured as a buffer.

Hardware Reset via the $\overline{\text{RESET}}$ Pin

$\overline{\text{RESET}}$, a hard reset (an asynchronous hard reset is executed by briefly pulling $\overline{\text{RESET}}$ low), restores the chip to the on-chip default register settings. It takes ~2 µs for the outputs to begin toggling after $\overline{\text{RESET}}$ is issued.

Soft Reset via the Serial Port

The serial port control register allows for a soft reset by setting Bit 2 and Bit 5 in Register 0x000. When Bit 5 and Bit 2 are set, the chip enters a soft reset mode and restores the chip to the on-chip setting, except for Register 0x000. Except for the self-clearing bits, Bit 2 and Bit 5, Register 0x000 retains its previous value prior to reset. These bits are self-clearing. However, the self-clearing operation does not complete until an additional serial port SCLK cycle occurs, and the AD9525 is held in reset until that happens.

POWER-DOWN MODES

Chip Power-Down via $\overline{PD}$

The AD9525 can be put into a power-down condition by pulling the $\overline{PD}$ pin low. Power-down turns off most of the functions and currents inside the AD9525. The chip remains in this power-down state until $\overline{PD}$ is brought back to logic high. When taken out of power-down mode, the AD9525 returns to the settings that were programmed into its registers prior to the power-down, unless the registers are changed by new programming while the $\overline{PD}$ pin is held low.

Powering down the chip shuts down the currents on the chip, except for the bias current necessary to maintain the LVPECL outputs in a safe shutdown mode. The LVPECL bias currents are needed to protect the LVPECL output circuitry from damage that can be caused by certain termination and load configurations when tristated. Because this is not a complete power-down, it can be called sleep mode.

When the AD9525 is in a $\overline{PD}$ power-down, the chip is in the following state:

- The PLL is off.
- The CLKIN input buffer is off, but the CLKIN input dc bias circuit is on.
- The reference input buffer is off, but the dc bias circuit is still on.
- All dividers are off.
- All LVPECL outputs are in safe off mode.
- The serial control port is active, and the chip responds to commands.

PLL Power-Down

The PLL section of the AD9525 can be selectively powered down. In this mode, the AD9525 can be used as a 1 to 8 clock buffer by using the CLKIN as the clock input.

Distribution Power-Down

The distribution section can be powered down by writing Register 0x230[4] = 1b, which turns off the bias to the distribution section.

Individual Clock Output Power-Down

Any of the clock distribution outputs can be powered down into safe power-down mode by individually writing to the appropriate registers. The register map details the individual power-down settings for each output. These settings are found in Register 0x0F0[0] to Register 0x0F7[0].

Individual Clock Channel Power-Down

Any of the clock distribution channels can be powered down individually by writing to the appropriate registers. Powering down a clock channel is similar to powering down an individual driver, but it saves more power because additional circuits are also powered down. Powering down a clock channel also automatically powers down the drivers connected to it. The register map details the individual power-down settings for each output channel. These settings are found in Register 0x0F0[4], Register 0x0F2[4], Register 0x0F4[4], and Register 0x0F6[4].

SERIAL CONTROL PORT

The AD9525 serial control port is a flexible, synchronous serial communications port that allows an easy interface with many industry-standard microcontrollers and microprocessors. The AD9525 serial control port is compatible with most synchronous transfer formats, including Motorola® SPI and Intel® SSR protocols. The serial control port allows read/write access to all registers that configure the AD9525.

PIN DESCRIPTIONS

SCLK (serial clock) is the serial shift clock. This pin is an input. SCLK is used to synchronize serial control port reads and writes. Write data bits are registered on the rising edge of this clock, and read data bits are registered on the falling edge. This pin is internally pulled down by a 30 kΩ resistor to ground.

SDIO (serial data input/output) is a dual-purpose pin that acts either as an input only (unidirectional mode) or as an input/output (bidirectional mode). The AD9525 defaults to the bidirectional I/O mode (Register 0x000[7] = 0b).

SDO (serial data out) is used only in the unidirectional I/O mode (Register 0x000[7] = 1b) as a separate output pin for reading back data.

$\overline{CS}$ (chip select bar) is an active low control that gates the read and write cycles. When $\overline{CS}$ is high, SDO and SDIO are in a high impedance state. This pin is internally pulled up by a 30 kΩ resistor to VS.

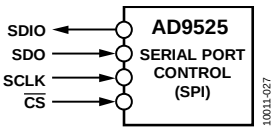


Figure 26. Serial Control Port

GENERAL OPERATION OF SERIAL CONTROL PORT

Single byte or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats. The AD9525 serial control port can be configured for a single bidirectional I/O pin (SDIO only) or for two unidirectional I/O pins (SDIO/SDO). By default, the AD9525 is in bidirectional mode. Short instruction mode (8-bit instruction) is not supported. Only long instruction mode (16-bit instruction) is supported.

A write or a read operation to the AD9525 is initiated by pulling $\overline{CS}$ low.

The $\overline{CS}$ stalled high mode is supported in data transfers where three or fewer bytes of data (plus instruction data) are transferred (see Table 24). In this mode, the $\overline{CS}$ pin can temporarily return high on any byte boundary, allowing time for the system controller to process the next byte. $\overline{CS}$ can go high on byte boundaries only and can go high during either part (instruction or data) of the transfer.

During this period, the serial control port state machine enters a wait state until all data is sent. If the system controller decides to abort the transfer before all of the data is sent, the state machine must be reset, either by completing the remaining transfers or by returning $\overline{CS}$ low for at least one complete SCLK cycle (but fewer than eight SCLK cycles). Raising the $\overline{CS}$ pin on a nonbyte boundary terminates the serial transfer and flushes the buffer.

In the streaming mode (see Table 25), any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented (see the MSB/LSB First Transfers section). $\overline{CS}$ must be raised at the end of the last byte to be transferred, thereby ending streaming mode.

Communication Cycle—Instruction Plus Data

There are two parts to a communication cycle with the AD9525. The first part writes a 16-bit instruction word into the AD9525, coincident with the first 16 SCLK rising edges. The instruction word provides the AD9525 serial control port with information regarding the data transfer, which is the second part of the communication cycle. The instruction word defines whether the upcoming data transfer is a read or a write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer.

Write

If the instruction word is for a write operation, the second part is the transfer of data into the serial control port buffer of the AD9525. Data bits are registered on the rising edge of SCLK.

The length of the transfer (one, two, or three bytes or streaming mode) is indicated by two bits ([W1:W0]) in the instruction byte. When the transfer is one, two, or three bytes but not streaming, $\overline{CS}$ can be raised after each sequence of eight bits to stall the bus (except after the last byte, where it ends the cycle). When the bus is stalled, the serial transfer resumes when $\overline{CS}$ is lowered. Raising the $\overline{CS}$ pin on a nonbyte boundary resets the serial control port. During a write, streaming mode does not skip over reserved or blank registers, and the user can write 0x00 to the reserved register addresses.

Because data is written into a serial control port buffer area, not directly into the actual control registers of the AD9525, an additional operation is needed to transfer the serial control port buffer contents to the actual control registers of the AD9525, thereby causing them to become active. The update registers operation (IO_UPDATE) consists of setting Register 0x232[0] = 1b (this bit is self-clearing). Any number of bytes of data can be changed before executing an update registers. The update registers operation simultaneously actuates all register changes that have been written to the buffer since any previous update.

Read

The AD9525 supports only the long instruction mode. If the instruction word is for a read operation, the next N × 8 SCLK cycles clock out the data from the address specified in the instruction word, where N is 1 to 3 as determined by [W1:W0]. If N = 4, the read operation is in streaming mode, continuing until $\overline{CS}$ is raised. Streaming mode does not skip over reserved or blank registers. The readback data is valid on the falling edge of SCLK.

The default mode of the AD9525 serial control port is the bidirectional mode. In bidirectional mode, both the sent data and the readback data appear on the SDIO pin. It is also possible to set the AD9525 to unidirectional mode (Register 0x000[7] = 1 and Register 0x000[0] = 1). In unidirectional mode, the readback data appears on the SDO pin.

A readback request reads the data that is in the serial control port buffer area or the data that is in the active registers (see Figure 27). Readback of the buffer or active registers is controlled by Register 0x004[0].

The AD9525 uses Register Address 0x000 to Register Address 0x232.

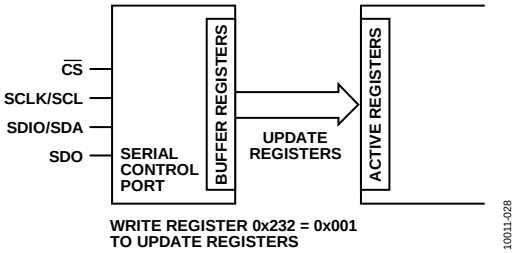


Figure 27. Relationship Between Serial Control Port Buffer Registers and Active Registers

THE INSTRUCTION WORD (16 BITS)

The MSB of the instruction word is R/$\overline{W}$, which indicates whether the instruction is a read or a write. The next two bits ([W1:W0]) indicate the length of the transfer in bytes. The final 13 bits are the address ([A12:A0]) at which to begin the read or write operation.

For a write, the instruction word is followed by the number of bytes of data indicated by Bits[W1:W0] (see Table 24).

Table 24. Byte Transfer Count

W1	W0	Bytes to Transfer
0	0	1
0	1	2
1	0	3
1	1	Streaming mode

Bits[A12:A0] select the address within the register map that is written to or read from during the data transfer portion of the communications cycle. Only Bits[A9:A0] are needed to cover the range of the 0x232 registers used by the AD9525. Bits[A12:A10] must always be 0b. For multibyte transfers, this address is the starting byte address. In MSB first mode, subsequent bytes decrement the address.

MSB/LSB FIRST TRANSFERS

The AD9525 instruction word and byte data can be MSB first or LSB first. Any data written to Register 0x000 must be mirrored; the upper four bits (Bits[7:4]) must mirror the lower four bits (Bits[3:0]). This makes it irrelevant whether LSB first or MSB first is in effect. As an example of this mirroring, see the default setting for Register 0x000, which mirrors Bit 4 and Bit 3. This sets the long instruction mode, which is the default and the only mode that is supported.

The default for the AD9525 is MSB first.

When LSB first is set by Register 0x000[1] and Register 0x000[6], it takes effect immediately because it affects only the operation of the serial control port and does not require that an update be executed.

When MSB first mode is active, the instruction and data bytes must be written from MSB to LSB. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes must follow, in order, from the high address to the low address. In MSB first mode, the serial control port internal address generator decrements for each data byte of the multibyte transfer cycle.

When LSB first is active, the instruction and data bytes must be written from LSB to MSB. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte, followed by multiple data bytes. In a multibyte transfer cycle, the internal byte address generator of the serial port increments for each byte.

The AD9525 serial control port register address decrements from the register address just written toward Register 0x000 for multibyte I/O operations if the MSB first mode is active (default). If the LSB first mode is active, the register address of the serial control port increments from the address just written toward Register 0x232 for multibyte I/O operations.

Streaming mode always terminates when it reaches Register 0x232. Note that unused addresses are not skipped during multibyte I/O operations.

Table 25. Streaming Mode (No Addresses Are Skipped)

Write Mode	Address Direction	Stop Sequence
LSB first	Increment	0x230, 0x231, 0x232, stop
MSB first	Decrement	0x001, 0x000, 0x232, stop

Table 26. Serial Control Port, 16-Bit Instruction Word, MSB First

MSB															LSB
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R/$\overline{W}$	W1	W0	A12 = 0	A11 = 0	A10 = 0	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

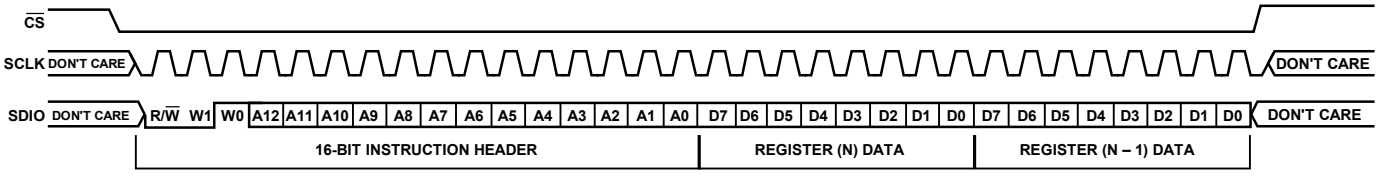


Figure 28. Serial Control Port Write—MSB First, 16-Bit Instruction, Two Bytes of Data

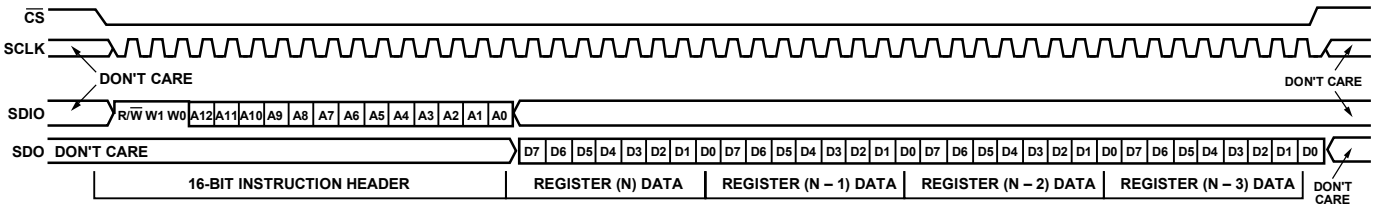


Figure 29. Serial Control Port Read—MSB First, 16-Bit Instruction, Four Bytes of Data

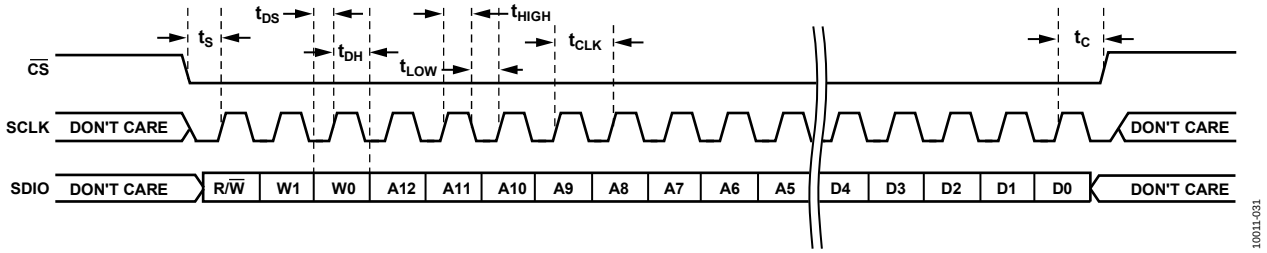


Figure 30. Serial Control Port Write—MSB First, 16-Bit Instruction, Timing Measurements

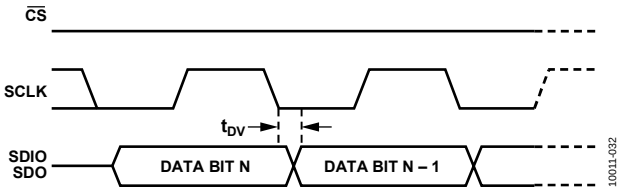


Figure 31. Timing Diagram for Serial Control Port Register Read

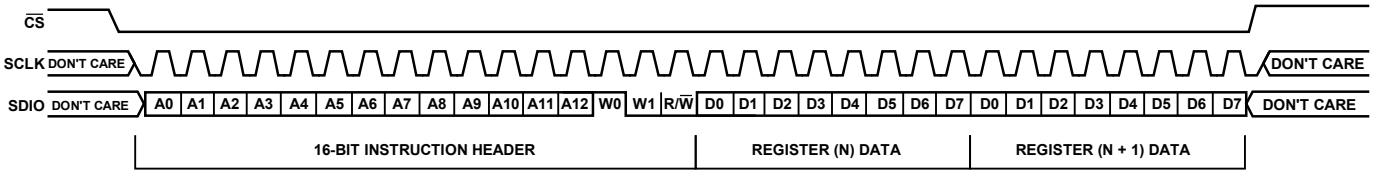


Figure 32. Serial Control Port Write—LSB First, 16-Bit Instruction, Two Bytes of Data

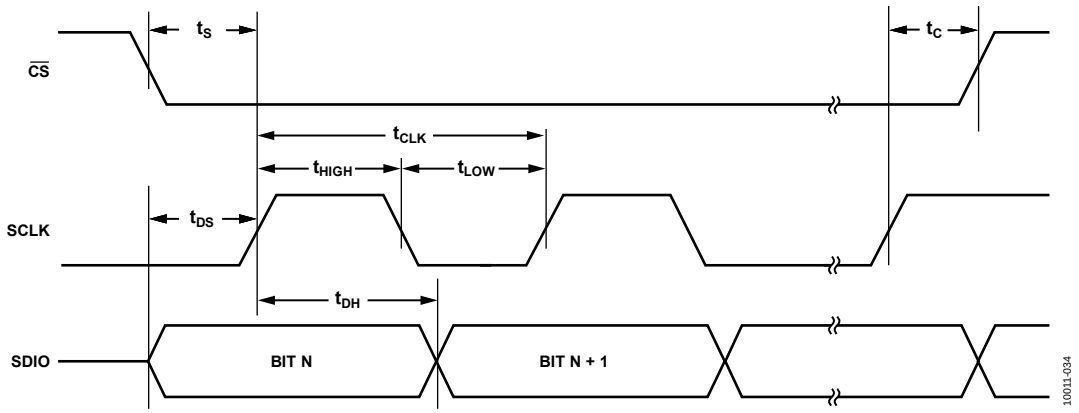


Figure 33. Serial Control Port Timing—Write

Table 27. Serial Control Port Timing

Parameter	Description
t_{DS}	Setup time between data and rising edge of SCLK
t_{DH}	Hold time between data and rising edge of SCLK
t_{CLK}	Period of the clock
t_S	Setup time between the $\overline{CS}$ falling edge and SCLK rising edge (start of communication cycle)
t_C	Setup time between SCLK rising edge and the $\overline{CS}$ rising edge (end of communication cycle)
t_{HIGH}	Minimum period that SCLK should be in a logic high state
t_{LOW}	Minimum period that SCLK should be in a logic low state
t_{DV}	SCLK to valid SDIO and SDO (see Figure 31)

CONTROL REGISTERS

CONTROL REGISTER MAP OVERVIEW

Register addresses that are not listed in Table 28 are not used, and writing to those registers has no effect. Registers that are marked as reserved should never have their values changed.

When writing to registers with bits that are marked reserved, the user should take care to always write the default value for the reserved bits.

Table 28. Control Register Map

Reg. Addr. (Hex)	Register Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)
Serial Port Configuration										
0x000	SPI mode serial port configuration	SDO active	LSB first/ address increase	Soft reset	Don't care	Don't care	Soft reset	LSB first/ address increase	SDO active	0x00
		Don't care	Don't care	Soft reset	Don't care	Don't care	Soft reset	Don't care	Don't care	0x00
0x004	Readback control	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Read back active regs	0x00
PLL Configuration										
0x010	PFD charge pump	PFD polarity	CP current, Bits[2:0]			CP mode, Bits[1:0]		Antibacklash pulse width, Bits[1:0]		0x7D
0x011	R dividers	REFB divider output high cycles, Bits[3:0]				REFB divider output low cycles, Bits[3:0]				0x00
0x012		REFA divider output high cycles, Bits[3:0]				REFA divider output low cycles, Bits[3:0]				0x00
0x013	B divider	B divider output high cycles, Bits[3:0]				B divider output low cycles, Bits[3:0]				0x00
0x014	N divider	Don't care	Don't care	B divider bypass	REFB divider bypass	REFA divider bypass	P divider prescaler, Bits[2:0]			0x00
0x015	Resets	Don't care	Reserved	Reserved	Reserved	B divider reset	REFB divider reset	REFA divider reset	Reset all dividers	0x00
0x016	REFC	REFC enable	REFC divider, Bits[6:0]							0x00
0x017	Status pin	Charge pump pin to VDD_CP/2	STATUS pin divider enable	STATUS output select, Bits[5:0]						0x00
0x018	REF_MON pin control	Don't care	Don't care	Don't care	REF_MON pin control, Bits[4:0]					0x00
0x019	Lock detect	Don't care	Don't care	Don't care	Don't care	Lock detect counter, Bits[1:0]		Digital lock detect window	Digital lock det disable	0x00
0x01A	Ref switchover and monitors	Enable FB clock present monitor	Enable REFA present monitor	Enable REFB present monitor	Disable switchover deglitch	Select REFB (manual register mode)	Stay on REFB	Use REF_SEL pin for reference switchover	Enable automatic reference switchover	0x00
0x01B	Reserved	Reserved = 0	Reserved = 0	Reserved = 0	Reserved = 0	Reserved = 0		Reserved = 0	Reserved = 0	0x00
0x01C	PLL block PD register	N divider ECL 2 CMOS PD	N divider PD	R Divider B ECL 2 CMOS PD	R Divider A ECL 2 CMOS PD	R Divider B PD	R Divider A PD	R Channel B PD	R Channel A PD	0x22
0x01F	PLL readback	Unused	Unused	Unused	Selected reference	Status FB clock	Status REFB	Status REFA	Digital lock detect (DLD)	N/A
PECL/CMOS Outputs										
0x0F0	LVPECL OUT0	Don't care	Don't care	Don't care	Power down Channel 0, Channel 1	Don't care	OUT0 PECL output level, Bits[1:0]		Power down PECL driver	0x04
0x0F1	LVPECL OUT1	Don't care	Don't care	Don't care	Reserved	Don't care	OUT1 PECL output level, Bits[1:0]		Power down PECL driver	0x04
0x0F2	LVPECL OUT2	Don't care	Don't care	Don't care	Power down Channel 2, Channel 3	Don't care	OUT2 PECL output level, Bits[1:0]		Power down PECL driver	0x04
0x0F3	LVPECL OUT3	Don't care	Don't care	Don't care	Reserved	Don't care	OUT3 PECL output level, Bits[1:0]		Power down PECL driver	0x04

Reg. Addr. (Hex)	Register Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)
0x0F4	LVPECL OUT4	Don't care	Don't care	Don't care	Power down Channel 4, Channel 5	Don't care	OUT4 PECL output level, Bits[1:0]		Power down PECL driver	0x04
0x0F5	LVPECL OUT5	Don't care	Don't care	Don't care	Reserved	Don't care	OUT5 PECL output level, Bits[1:0]		Power down PECL driver	0x04
0x0F6	LVPECL OUT6	Don't care	Don't care	Don't care	Power down Channel 6, Channel 7	Don't care	OUT6 PECL output level, Bits[1:0]		Power down PECL driver	0x04
0x0F7	LVPECL OUT7	Don't care	Don't care	Don't care	Reserved	Don't care	OUT7 PECL output level, Bits[1:0]		Power down PECL driver	0x04
0x0F8	Sync output	Don't care	Don't care	Don't care	Power down sync channel	Don't care	SYNC_OUT PECL output level, Bits[1:0]		Power down PECL driver	0x10
0x0F9	Sync output, other control	Don't care	Don't care	Don't care	Polarity CMOS mode	Enable CMOS drivers, Bits[1:0]		CMOS mode	Sync out resampling edge select	0x00
0x0FA	Drivers reserved	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	0x00
SYNC Control										
0x190	Sync clock S divider	Sync clock S divider, Bits[7:0]								0x00
0x191	Sync clock S divider	Sync clock S divider, Bits[15:8]								0x00
0x192	Sync clock control	Don't care	Don't care	Don't care	Sync enable	Sync source, Bits[1:0]		Sync mode, Bits[1:0]		0x00
VCO, Reference and CLK1 Inputs										
0x1E0	VCO divider	Don't care	Don't care	Don't care	Don't care	Don't care	M divider, Bits[2:0]			0x00
Other										
0x230	Power-down	Don't care	Don't care	Don't care	Dist all power-down	CLKIN power-down	M divider power-down	Distribution reference power-down	PLL power-down	0x00
0x232	IO_UPDATE	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care	IO_UPDATE	0x00

REGISTER MAP DESCRIPTIONS

Table 29 through Table 49 provide a detailed description of each of the control register functions. The registers are listed by hexadecimal address.

Table 29. SPI Mode Serial Port Configuration

Reg. Addr. (Hex)	Bits	Bit Name	Description
0x000	7	SDO active	Selects unidirectional or bidirectional data transfer mode. 0: SDIO pin used for write and read; SDO is high impedance (default). 1: SDO used for read; SDIO used for write; unidirectional mode.
	6	LSB first/address increase	SPI MSB or LSB data orientation. 0: data-oriented MSB first; addressing decrements (default). 1: data-oriented LSB first; addressing increments.
	5	Soft reset	Soft reset. 1 (self-clearing): soft reset; restores default values to internal registers.
	4	Unused	Unused.
	[3:0]	Mirror[7:4]	Bits[3:0] should always mirror Bits[7:4] so that it does not matter whether the part is in MSB or LSB first mode (see Register 0x000[6]). Set bits as follows: Bit 0 = Bit 7 Bit 1 = Bit 6 Bit 2 = Bit 5 Bit 3 = Bit 4
0x004	0	Read back active registers	Select register bank used for a readback. 0: reads back buffer registers (default). 1: reads back active registers.

Table 30. PFD Charge Pump

Reg. Addr. (Hex)	Bits	Bit Name	Description			
0x010	7	PFD polarity	Sets the PFD polarity. 0: Positive (higher control voltage produces higher frequency) (default). 1: Negative (higher control voltage produces lower frequency).			
	[6:4]	CP current	Charge pump current (with CPRSET = 5.1 kΩ).			
			Bit 6	**Bit 5**	**Bit 4**	**I_{CP} (mA)**
			0	0	0	0.6
			0	0	1	1.2
			0	1	0	1.8
			0	1	1	2.4
			1	0	0	3.0
			1	0	1	3.6
			1	1	0	4.2
			1	1	1	4.8 (default)
	[3:2]	CP mode	Charge pump operating mode.			
			Bit 3	**Bit 2**	**Charge Pump Mode**	
			0	0	High impedance state	
			0	1	Force source current (pump-up)	
			1	0	Force sink current (pump-down)	
			1	1	Normal operation (default)	
	[1:0]	Antibacklash pulse width	See Table 7 for the maximum operating frequency for each setting.			
			Bit 1	**Bit 0**	**Antibacklash Pulse Width Mode (ns)**	
			0	0	2.9 (default)	
			0	1	1.3	
			1	0	6.0	
			1	1	2.9	

Table 31. REFA, REFB, REFC, B, N, and P Dividers

Reg. Addr. (Hex)	Bits	Bit Name	Description
0x011	[7:4]	REFB divider output high cycles	Divider high cycle word. Normally set to one-half desired divider division minus one: for example, D/2 – 1; therefore, for Divide = 8, set to 0x03 (8/2 – 1). Number of clock cycles (minus 1) of the divider input during which the divider output stays high. A value of 0x7 means that the divider is low for eight input clock cycles (default: 0x0).
	[3:0]	REFB divider output low cycles	Divider low cycle word. Normally set to one-half desired divider division minus one: for example, D/2 – 1; therefore, for Divide = 8, set to 0x03 (8/2 – 1). Number of clock cycles (minus 1) of the divider input during which the divider output stays high. A value of 0x7 means that the divider is low for eight input clock cycles (default: 0x0).
0x012	[7:4]	REFA divider output high cycles	Divider high cycle word. Normally set to one-half desired divider division minus one: for example, D/2 – 1; therefore, for Divide = 8, set to 0x03 (8/2 – 1). Number of clock cycles (minus 1) of the divider input during which the divider output stays low. A value of 0x7 means the divider is high for eight input clock cycles (default: 0x0).
	[3:0]	REFA divider output low cycles	Divider low cycle word. Normally set to one-half desired divider division minus one: for example, D/2 – 1; therefore, for Divide = 8, set to 0x03 (8/2 – 1). Number of clock cycles (minus 1) of the divider input during which the divider output stays high. A value of 0x7 means that the divider is low for eight input clock cycles (default: 0x0).
0x013	[7:4]	B divider output high cycles	Divider high cycle word. Normally set to one-half desired divider division minus one: for example, D/2 – 1; therefore, for Divide = 8, set to 0x03 (8/2 – 1). Number of clock cycles (minus 1) of the divider input during which the divider output stays low. A value of 0x7 means the divider is high for eight input clock cycles (default: 0x0).
	[3:0]	B divider output low cycles	Divider low cycle word. Normally set to one-half desired divider division minus one: for example, D/2 – 1; therefore, for Divide = 8, set to 0x03 (8/2 – 1). Number of clock cycles (minus 1) of the divider input during which the divider output stays high. A value of 0x7 means that the divider is low for eight input clock cycles (default: 0x0).
0x014	[7:6]	Don't care	Don't care.
	5	B divider bypass	Bypasses and powers down the B divider; routes input to divider output. 0: uses divider (default). 1: B divider is set to divide-by-1.
	4	REFB divider bypass	Bypasses and powers down the divider; routes input to divider output. 0: uses divider (default). 1: REFB divider is set to divide-by-1.
	3	REFA divider bypass	Bypasses and powers down the divider; routes input to divider output. 0: use divider (default). 1: REFA divider is set to divide-by-1.
	[2:0]	P divider prescaler	P divider value (B divider prescaler).

Bit 2	Bit 1	Bit 0	Divider Value
0	0	0	1(default)
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	Static
1	1	1	Static

0x015	7	Don't care	Don't care.
	6	Reserved	0 (default).
	5	Reserved	0 (default).
	4	Reserved	0 (default).
	3	B divider reset	Resets B divider. 0: normal operation (default). 1: holds B divider in reset.

Reg. Addr. (Hex)	Bits	Bit Name	Description
	2	REFB divider reset	Resets REFB divider. 0: normal (default). 1: holds REFB divider in reset.
	1	REFA divider reset	Resets REFA divider. 0: normal (default). 1: holds REFA divider in reset.
	0	Reset all dividers	Resets REFA, REFB, B divider (B divider is part of N divider). 0: normal (default). 1: holds REFA, REFB, B divider in reset.
0x016	7	REFC enable	Enables REFC path. 0: disabled (default). 1: enables REFC path.
	[6:0]	REFC divider	7-bit REFC divider. Divide-by-1 to divide-by-127. 0000000, 0000001: both divide-by-1 (default: 0x00).

Table 32. Status Pin and Other

Reg. Addr. (Hex)	Bits	Bit Name	Description							
0x017	7	Charge pump pin to VDD_CP/2	Sets the charge pump pin to one-half of the VDD_CP supply voltage. 0: charge pump normal operation (default). 1: charge pump pin set to VDD_CP/2.							
	6	STATUS pin divider enable	Enables STATUS pin divider. 0: disabled (default). 1: enables divider.							
	[5:0]	STATUS output select	Selects the signal that appears at the STATUS pin. Register 0x017[6] must be set to 0 to for any mode identified as LVL.							
			Bit 5	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Level or Dynamic Signal**	**Signal at STATUS Pin**
			0	0	0	0	0	0	LVL	Ground, dc (default).
			0	0	0	0	0	1	DYN	N divider output.
			0	0	0	0	1	0	LVL	Ground, dc.
			0	0	0	0	1	1	LVL	Ground, dc.
			0	0	0	1	0	0	LVL	Ground, dc.
			0	0	0	1	0	1	DYN	PFD up pulse.
			0	0	0	1	1	0	DYN	PFD down pulse.
			0	X	X	X	X	X	LVL	Ground (dc); for all other cases of 0XXXXX not specified.
										The selections that follow are the same as for the REF_MON pin.
			1	0	0	0	0	0	LVL	Ground (dc).
			1	0	0	0	0	1	DYN	REFA clock.
			1	0	0	0	1	0	DYN	REFB clock.
			1	0	0	0	1	1	DYN	Selected reference clock to PLL.
			1	0	0	1	0	0	DYN	Unselected reference clock to PLL.
			1	0	0	1	0	1	LVL	Both REFA and REFB clocks missing (active high).
			1	0	0	1	1	0	LVL	Ground, dc.
			1	0	0	1	1	1	LVL	REFA present (active high).
			1	0	1	0	0	0	LVL	REFB present (active high).
			1	0	1	0	0	1	LVL	(REFA present) AND (REFB present).

Reg. Addr. (Hex)	Bits	Bit Name	Description							
			Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Level or Dynamic Signal	Signal at STATUS Pin
			1	0	1	0	1	0	LVL	(DLD) AND (selected reference present) AND (feedback clock present).
			1	0	1	0	1	1	LVL	Feedback clock present (active high).
			1	0	1	1	0	0	LVL	Selected reference (low: REFA, high: REFB).
			1	0	1	1	0	1	LVL	DLD; active high.
			1	0	1	1	1	0	LVL	N/A.
			1	0	1	1	1	1	LVL	Ground (dc).
			1	1	0	0	0	0	LVL	VDD3 (PLL power supply).
			1	1	0	0	0	1	DYN	$\overline{\text{REFA}}$ clock.
			1	1	0	0	1	0	DYN	$\overline{\text{REFB}}$ clock.
			1	1	0	0	1	1	DYN	$\overline{\text{Selected reference to PLL.}}$
			1	1	0	1	0	0	DYN	$\overline{\text{Unselected reference to PLL.}}$
			1	1	0	1	0	1	LVL	Status of selected reference (status of differential reference); active low.
			1	1	0	1	1	0	LVL	Both reference clocks missing; active low.
			1	1	0	1	1	1	LVL	REFA present (active low).
			1	1	1	0	0	0	LVL	REFB present (active low).
			1	1	1	0	0	1	LVL	$\overline{\text{(REFA present) AND (REFB present).}}$
			1	1	1	0	1	0	LVL	(DLD) AND (selected reference present) AND (feedback clock present); (active low).
			1	1	1	0	1	1	LVL	$\overline{\text{Feedback clock present}}$
			1	1	1	1	0	0	LVL	Selected reference (low = REFA, high = REFB); active low.
			1	1	1	1	0	1	LVL	DLD (active low).
			1	1	1	1	1	0	LVL	N/A.
			1	1	1	1	1	1	LVL	VDD3 (PLL power supply).

Table 33. REF_MON Pin Control

Reg. Addr. (Hex)	Bits	Bit Name	Description						
0x018	[7:5]	Don't care	Don't care.						
	[4:0]	REF_MON pin control	Selects the signal that is connected to the REF_MON pin.						
			Bit 4	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Level or Dynamic Signal**	**Signal at REF_MON Pin**
			0	0	0	0	0	LVL	Ground (dc).
			0	0	0	0	1	DYN	REFA clock.
			0	0	0	1	0	DYN	REFB clock.
			0	0	0	1	1	DYN	Selected reference clock to PLL.
			0	0	1	0	0	DYN	Unselected reference clock to PLL.
			0	0	1	0	1	LVL	Both reference clocks missing (active high).
			0	0	1	1	0	LVL	Ground (dc).
			0	0	1	1	1	LVL	Status REF A frequency (active high).
			0	1	0	0	0	LVL	Status REF B frequency (active high).
			0	1	0	0	1	LVL	(Status REF A frequency) AND (status REF B frequency).
			0	1	0	1	0	LVL	(DLD) AND (status of selected reference) AND (status of feedback clock).
			0	1	0	1	1	LVL	Status of feedback clock (active high).
			0	1	1	0	0	LVL	Selected reference (low: REFA, high: REFB).
			0	1	1	0	1	LVL	DLD; active high.
			0	1	1	1	0	LVL	N/A.
			0	1	1	1	1	LVL	Ground, dc.
			1	0	0	0	0	LVL	VDD3 (PLL power supply).
			1	0	0	0	1	DYN	$\overline{\text{REFA}}$.
			1	0	0	1	0	DYN	$\overline{\text{REFB}}$.
			1	0	0	1	1	DYN	$\overline{\text{Selected reference to PLL}}$.
			1	0	1	0	0	DYN	$\overline{\text{Unselected reference to PLL}}$.
			1	0	1	0	1	LVL	Status of selected reference (status of differential reference); active low.
			1	0	1	1	0	LVL	Status of unselected reference (not available in differential mode); active low.
			1	0	1	1	1	LVL	Status of REF A frequency (active low).
			1	1	0	0	0	LVL	Status of REF B frequency (active low).
			1	1	0	0	1	LVL	$\overline{\text{(Status of REFA frequency) AND (status of REFB frequency)}}$.
			1	1	0	1	0	LVL	$\overline{\text{(DLD) AND (status of selected reference) AND (status of feedback clock)}}$.
			1	1	0	1	1	LVL	Status of feedback clock (active low).
			1	1	1	0	0	LVL	Selected reference (low: REFA, high: REFB); active low.
			1	1	1	0	1	LVL	DLD (active low).
			1	1	1	1	0	LVL	N/A.
			1	1	1	1	1	LVL	VDD3 (PLL power supply).

Table 34. Lock Detect

Reg. Addr. (Hex)	Bits	Bit Name	Description
0x019	[7:4]	Don't care	Don't care.
	[3:2]	Lock detect counter	Required consecutive number of PFD cycles with edges inside lock detect window before the DLD indicates a locked condition.
			Bit 3 / **Bit 2** / **PFD Cycles to Determine Lock** 0 / 0 / 5 (default) 0 / 1 / 16 1 / 0 / 64 1 / 1 / 255
	1	Digital lock detect window	If the time difference of the rising edges at the inputs to the PFD is less than the lock detect window time, the digital lock detect flag is set. The flag remains set until the time difference is greater than the loss-of-lock threshold. 0: high range (default). 1: low range.
	0	Digital lock detect disable	Digital lock detect operation. 0: normal lock detect operation (default). 1: disables lock detect.

Table 35. Reference Switchover and Monitors

Reg. Addr. (Hex)	Bits	Bit Name	Description
0x01A	7	Enable feedback clock present monitor	Enables feedback clock monitor. The presence of a feedback clock is checked with the selected reference to the PLL. This monitor does not have a valid output if there is no reference to the PLL. 0: disables monitor (default). 1: enables monitor.
	6	Enable REFA present monitor	Enables Reference A clock monitor. The presence of the REFA clock is checked with the feedback clock to the PLL. This monitor does not have a valid output if there is no feedback clock to the PLL. Register 0x01C[4] = 0 (on) for monitor to work. 0: disables monitor (default). 1: enables monitor.
	5	Enable REFB present monitor	Enables Reference B clock monitor. The presence of the REFB clock is checked with the feedback clock to the PLL. This monitor does not have a valid output if there is no feedback clock to the PLL. Register 0x01C[5] = 0 (on) for monitor to work. 0: disables monitor (default). 1: enables monitor.
	4	Disable switchover deglitch	Disables or enables the switchover deglitch circuit. 0: enables switchover deglitch circuit (default). 1: disables switchover deglitch circuit.
	3	Select REFB (manual register mode)	If Register 0x01A[1] = 0, selects reference for PLL. 0: selects REFA. 1: selects REFB.
	2	Stay on REFB	Stays on REFB after switchover. 0: returns to REFA automatically when REFA status is good again. 1: stays on REFB after switchover. Do not automatically return to REFA.
	1	Use REF_SEL pin for reference switchover	If Register 0x01A[0] = 0 (manual), sets method of PLL reference selection. 0: uses Register 0x01A[3] (default). 1: uses REF_SEL pin.
	0	Enable automatic ref switchover	Automatic or manual reference switchover. 0: manual reference switchover. 1: automatic reference switchover.

Table 36. Reserved

Reg. Addr. (Hex)	Bits	Bit Name	Description
0x01B	[7:0]	Reserved	Reserved. 0: default. All bits should be set to 0.

Table 37. PLL Block Power-Down

Reg. Addr. (Hex)	Bits	Name	Description
0x01C	7	N divider ECL 2 CMOS power-down	Turns off the N divider's output clock. This stops the clock to the PFD and the frequency monitors. 0: clock on (default). 1: clock off.
	6	N divider power-down	N divider power-down. 0: N divider on (default). 1: N divider off.
	5	REFB Divider ECL 2 CMOS power-down	This bit stops the clock to the frequency monitors for REFB. If this bit is disabled, the automatic reference switchover does not operate. In some configurations, enabling the REFB divider ECL 2 CMOS may increase reference spurs on clock outputs. 0: on. 1: off (default).
	4	REFA Divider ECL 2 CMOS power-down	This bit stops the clock to the frequency monitors for REFA. If this bit is disabled, the automatic reference switchover does not operate. In some configurations, enabling the REFA Divider ECL 2 CMOS may increase reference spurs on clock outputs. 0: on (default). 1: off.
	3	REFB divider power-down	Powers down REFB divider. The REFB input receiver is still powered up. 0: REFB divider on (default). 1: REFB divider off.
	2	REFA divider power-down	Powers down REFA divider. The REFA input receiver is still powered up. 0: REFA divider on (default). 1: REFA divider off.
	1	REFB channel power-down	Powers down REFB channel. The REFB input receiver is powered down. 0: REFB channel on. 1: REFB channel off (default).
	0	REFA channel power-down	Powers down REFA channel. The REFA input receiver is powered down. 0: REFA channel on (default). 1: REFA channel off.

Table 38. PLL Readback

Reg. Addr. (Hex)	Bits	Bit Name	Description
0x01F	[7:5]	Unused	Unused
	4	Selected reference	Shows the reference used by the PLL 0: REFA 1: REFB
	3	Status feedback clock	Status of the feedback clock, does not have a valid output unless 0x01A[7] = 1 0: missing 1: present
	2	Status REFB	Status of Reference B clock, does not have a valid output unless 0x01A[5] = 1 and 0x01C[5] = 0 0: missing 1: present
	1	Status REFA	Status of Reference A clock, does not have a valid output unless 0x01A[6] = 1 and 0x01C[4] = 0 0: missing 1: present
	0	Digital lock detect (DLD)	Digital lock detect 0: PLL not locked 1: PLL locked

Table 39. LVPECL Drivers OUT0

Reg. Addr. (Hex)	Bits	Bit Name	Description		
0x0F0	[7:5]	Don't care	Don't care		
	4	Power down Channel 0 and Channel 1	Powers down Channel 0 and Channel 1 0: enabled (default) 1: power-down		
	3	Don't care	Don't care		
	[2:1]	OUT0 level	**Bit 1**	**Bit 0**	**V_{OD} (mV)**
			0	0	400
			0	1	600
			1	0	780 (default)
			1	1	960
	0	OUT0 driver power-down	0: enabled (default) 1: power-down		

Table 40. LVPECL Drivers OUT1

Reg. Addr. (Hex)	Bits	Bit Name	Description		
0x0F1	[7:5]	Don't care	Don't care		
	4	Reserved	Reserved, write 0		
	3	Don't care	Don't care		
	[2:1]	OUT1 level	**Bit 1**	**Bit 0**	**V_{OD} (mV)**
			0	0	400
			0	1	600
			1	0	780 (default)
			1	1	960
	0	OUT1 driver power-down	0: enabled (default) 1: power-down		

Table 41. LVPECL Drivers OUT2

Reg. Addr. (Hex)	Bits	Bit Name	Description		
0x0F2	[7:5]	Don't care	Don't care		
	4	Power down Channel 2 and Channel 3	Powers down Channel 2 and Channel 3 0: enabled (default) 1: power-down		
	3	Don't care	Don't care		
	[2:1]	OUT2 level	**Bit 1**	**Bit 0**	**V_{OD} (mV)**
			0	0	400
			0	1	600
			1	0	780 (default)
			1	1	960
	0	OUT2 driver power-down	0: enabled (default) 1: power-down		

Table 42. LVPECL Drivers OUT3

Reg. Addr. (Hex)	Bits	Bit Name	Description		
0x0F3	[7:5]	Don't care	Don't care		
	4	Reserved	Reserved, write 0		
	3	Don't care	Don't care		
	[2:1]	OUT3 level	**Bit 1**	**Bit 0**	**V_{OD} (mV)**
			0	0	400
			0	1	600
			1	0	780 (default)
			1	1	960
	0	OUT3 driver power-down	0: enabled (default) 1: power-down		

Table 43. PECL Drivers OUT4

Reg. Addr. (Hex)	Bits	Bit Name	Description		
0x0F4	[7:5]	Don't care	Don't care		
	4	Power down Channel 4 and Channel 5	Powers down Channel 4 and Channel 5 0: enabled (default) 1: power-down		
	3	Don't care	Don't care		
	[2:1]	OUT4 level	**Bit 1**	**Bit 0**	**V_{OD} (mV)**
			0	0	400
			0	1	600
			1	0	780 (default)
			1	1	960
	0	OUT4 driver power-down	0: enabled (default) 1: power-down		

Table 44. LVPECL Drivers OUT5

Reg. Addr. (Hex)	Bits	Bit Name	Description		
0x0F5	[7:5]	Don't care	Don't care		
	4	Reserved	Reserved, write 0		
	3	Don't care	Don't care		
	[2:1]	OUT5 level	**Bit 1**	**Bit 0**	**V_{OD} (mV)**
			0	0	400
			0	1	600
			1	0	780 (default)
			1	1	960
	0	OUT5 driver power-down	0: enabled (default) 1: power-down		

Table 45. LVPECL Drivers OUT6

Reg. Addr. (Hex)	Bits	Bit Name	Description		
0x0F6	[7:5]		Don't care		
	4	Power down Channel 6 and Channel 7	Power down Channel 6 and Channel 7 0: enabled (default) 1: power-down		
	3		Don't care		
	[2:1]	OUT6 level	**Bit 1**	**Bit 0**	**V_{OD} (mV)**
			0	0	400
			0	1	600
			1	0	780 (default)
			1	1	960
	0	OUT6 driver power-down	0: enabled (default) 1: power-down		

Table 46. LVPECL Drivers OUT7

Reg. Addr. (Hex)	Bits	Bit Name	Description		
0x0F7	[7:5]	Don't care	Don't care		
	4	Reserved	Reserved, write 0		
	3	Don't care	Don't care		
	[2:1]	OUT7 level	**Bit 1**	**Bit 0**	**V_{OD} (mV)**
			0	0	400
			0	1	600
			1	0	780 (default)
			1	1	960
	0	OUT7 driver power-down	0: enabled (default) 1: power-down		

Table 47. SYNC_OUT Control

Reg. Addr. (Hex)	Bits	Bit Name	Description			
0x0F8	[7:5]	Don't care	Don't care.			
	4	SYNC_OUT channel power-down	Powers down SYNC_OUT channel. 0: enabled. 1: power-down (default).			
	3	Sync polarity	Polarity LVPECL mode. 0: noninverting (default). 1: inverting.			
	[2:1]	SYNC_OUT level	**Bit 1**	**Bit 0**	**V_{OD} (mV)**	
			0	0	400 (default)	
			0	1	600	
			1	0	780	
			1	1	960	
	0	SYNC_OUT driver power-down	0: enabled (default). 1: powers down LVPECL SYNC_OUT driver.			
0x0F9	[7:5]	Don't care	Don't care.			
	4	Polarity CMOS mode	Polarity CMOS mode. This bit is also used in conjunction with Register 0x0F8[3] when the driver is in CMOS mode (Register 0x0F9[1] = 1).			
			Reg. 0x0F9[4]	**Reg. 0x0F8[3]**	**SYNC OUT/SYNC OUTB**	
			0	0	Noninverting/noninverting	
			0	1	Inverting/inverting	
			1	0	Noninverting/inverting	
			1	1	Inverting/noninverting	
	[3:2]	Enable CMOS drivers	Sets the CMOS driver output configuration when Register 0x0F9[1] = 1.			
			Bit 3	**Bit 2**	**SYNC_OUT**	**$\overline{\text{SYNC\_OUT}}$**
			0	0	Tristate	Tristate
			0	1	On	Tristate
			1	0	Tristate	On
			1	1	On	On
	1	CMOS mode	Use CMOS mode instead of LVPECL mode for SYNC_OUT. 0: LVPECL mode (default). 1: CMOS mode.			
	0	Sync out resampling edge select	SYNC_OUT resample edge select. Selects the M divider output edge used to resample the sync clock. 0: use rising edge of M clock (default). 1: use falling edge of M clock.			
0x190	[7:0]	Sync clock S divider	16-bit sync S divider, Bits[7:0] (LSB). Cycles of reference clock = S Divider Bits[15:0] + 1. For example, [15:0] = 0 is 1 reference clock cycles, [15:0] = 1 is 2 reference clock cycles … [15:0] = 65535 is 65536 reference clock cycles.			
0x191	[7:0]	Sync clock S divider	16-bit sync S divider, Bits[15:8] (MSB).			
0x192	[7:5]	Don't care	Don't care.			
	4	Sync enable	0: disable SYNC_OUT (default). 1: Enable SYNC_OUT. Note: Self-clearing for single shot sync.			
	[3:2]	Sync source	**Bit 1**	**Bit 0**	**Select Reference for SYNC Clock**	
			0	0	REF: reference input (default)	
			0	1	FB: PLL feedback N divider	
			1	0	Power-down: power down SYNC	
			1	1	Power-down: power down SYNC	
	[1:0]	Sync mode	**Bit 1**	**Bit 0**	**Sync Mode**	
			0	0	Single shot (default)	
			0	1	Periodic	
			1	0	Pseudorandom	
			1	1	Pseudorandom	

Table 48. VCO, Reference, and CLK Inputs

Reg. Addr. (Hex)	Bits	Bit Name	Description			
0x1E0	[7:3]	Don't care	Don't care.			
	[2:0]	M divider	M divider value.			
			Bit 2	**Bit 1**	**Bit 0**	**Divider Value**
			0	0	0	1
			0	0	1	2
			0	1	0	3
			0	1	1	4
			1	0	0	5
			1	0	1	6
			1	1	0	7
			1	1	1	8

Table 49. Other

Reg. Addr. (Hex)	Bits	Name	Description
0x230	[7:5]	Don't care	Don't care.
	4	Dist all power-down	Powers down all of distribution. Puts all drivers in safe power-down mode. 0 (default): enabled. 1: power-down.
	3	CLKIN power-down	Powers down CLKIN, $\overline{\text{CLKIN}}$. 0 (default): enabled. 1: power-down.
	2	M divider power-down	Powers down M divider. 0 (default): enabled. 1: power-down.
	1	Distribution reference power-down	Power down distribution reference. This bit should be asserted only when the drivers do not need the safe power-down mode guidelines. 0 (default): enabled. 1: power-down.
	0	PLL power-down	Power down PLL. 0 (default): enabled. 1: power-down.
232	[7:1]	Don't care	Don't care.
	0	IO_UPDATE	This bit must be set to 1b to transfer the contents of the buffer registers into the active registers. This happens on the next SCLK rising edge. This bit is self-clearing; that is, it does not have to be set back to 0. 1 (self-clearing): update all active registers to the contents of the buffer registers.

APPLICATIONS INFORMATION

FREQUENCY PLANNING USING THE AD9525

The AD9525 is a highly flexible PLL. When choosing the PLL settings and version of the AD9525, the following guidelines should be kept in mind.

The AD9525 has three frequency dividers: the reference (or R) divider, the feedback (or N) divider, and the M divider. When trying to achieve a particularly difficult frequency divide ratio requiring a large amount of frequency division, some of the frequency division can be done by either the M divider or the N divider, thus allowing a higher phase detector frequency and more flexibility in choosing the loop bandwidth.

Choosing a nominal charge pump current in the middle of the allowable range as a starting point allows the designer to increase or decrease the charge pump current and, thus, allows the designer to fine-tune the PLL loop bandwidth in either direction.

ADIsimCLK is a powerful PLL modeling tool that can be downloaded from www.analog.com. It is very accurate in determining the optimal loop filter for a given application.

USING THE AD9525 OUTPUTS FOR ADC CLOCK APPLICATIONS

Any high speed ADC is extremely sensitive to the quality of the sampling clock of the AD9525. An ADC can be thought of as a sampling mixer, and any noise, distortion, or time jitter on the clock is combined with the desired signal at the analog-to-digital output. Clock integrity requirements scale with the analog input frequency and resolution, with higher analog input frequency applications at ≥14-bit resolution being the most stringent. The theoretical SNR of an ADC is limited by the ADC resolution and the jitter on the sampling clock. Considering an ideal ADC of infinite resolution, where the step size and quantization error can be ignored, the available SNR can be expressed, approximately, by

$$SNR(\text{dB}) = 20\log\left(\frac{1}{2\pi f_A t_J}\right)$$

where:
f_A is the highest analog frequency being digitized.
t_J is the rms jitter on the sampling clock.

Figure 34 shows the required sampling clock jitter as a function of the analog frequency and effective number of bits (ENOB).

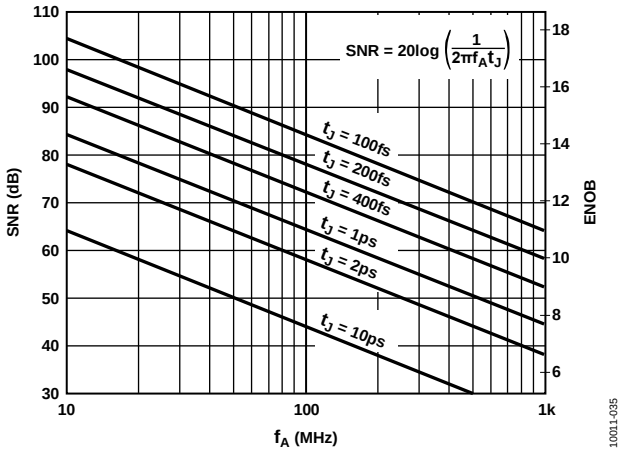


Figure 34. SNR and ENOB vs. Analog Input Frequency

For more information, see the AN-756 Application Note, *Sampled Systems and the Effects of Clock Phase Noise and Jitter*, and the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance*, at www.analog.com.

Many high performance ADCs feature differential clock inputs to simplify the task of providing the required low jitter clock on a noisy PCB. Distributing a single-ended clock on a noisy PCB can result in coupled noise on the sampling clock. Differential distribution has inherent common-mode rejection that can provide superior clock performance in a noisy environment. The differential LVPECL outputs of the AD9525 enable clock solutions that maximize converter SNR performance.

The input requirements of the ADC (differential or single-ended, logic level termination) should be considered when selecting the best clocking/converter solution.

LVPECL CLOCK DISTRIBUTION

The LVPECL outputs (because they are open emitter) require a dc termination to bias the output transistors. The simplified equivalent circuit in Figure 22 shows the LVPECL output stage.

In most applications, a LVPECL far-end Thevenin termination (see Figure 35) or Y-termination (see Figure 36) is recommended. In both cases, VS of the receiving buffer should match VS_DRV (VS_DRV = VDD3). If it does not match, ac coupling is recommended (see Figure 37).

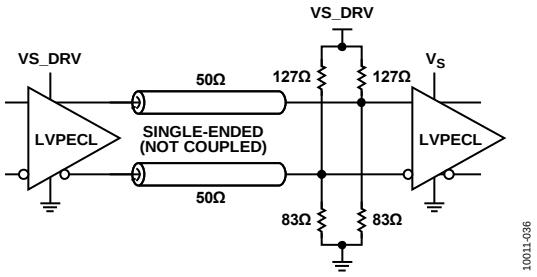


Figure 35. DC-Coupled 3.3 V LVPECL Far-End Thevenin Termination

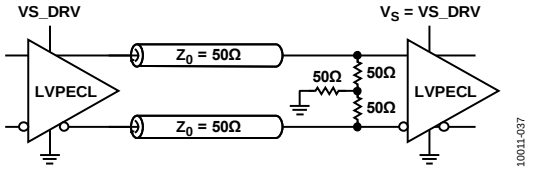


Figure 36. DC-Coupled 3.3 V LVPECL Y-Termination

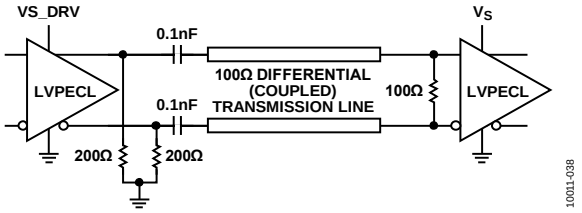


Figure 37. AC-Coupled LVPECL with Parallel Transmission Line

LVPECL Y-termination is an elegant termination scheme that uses the fewest components and offers both odd- and even-mode impedance matching. Even-mode impedance matching is an important consideration for closely coupled transmission lines at high frequencies. Its main drawback is that it offers limited flexibility for varying the drive strength of the emitter-follower LVPECL driver. This can be an important consideration when driving long trace lengths but is usually not an issue.

Thevenin-equivalent termination uses a resistor network to provide 50 Ω termination to a dc voltage that is below V_{OL} of the LVPECL driver. In this case, VS_DRV on the AD9525 should equal V_S of the receiving buffer. Although the resistor combination shown results in a dc bias point of VS_DRV − 2 V, the actual common-mode voltage is VS_DRV − 1.3 V because there is additional current flowing from the AD9525 LVPECL driver through the pull-down resistor.

SYNC_OUT DISTRIBUTION

The SYNC_OUT driver of the AD9525 can be configured as CMOS drivers. When selected for use as CMOS drivers, each output becomes a pair of CMOS outputs, each of which can be individually turned on or off and set as inverting or noninverting. Be sure to note the skew difference of using CMOS mode vs. LVPECL mode.

When single-ended CMOS clocking is used, refer to the guidelines presented in the following paragraphs.

Point-to-point connections should be designed such that each driver has only one receiver, if possible. Connecting outputs in this manner allows for simple termination schemes and minimizes ringing due to possible mismatched impedances on the output trace. Series termination at the source is generally required to provide transmission line matching and/or to reduce current transients at the driver.

The value of the resistor is dependent on the board design and timing requirements (typically 10 Ω to 100 Ω is used). CMOS outputs are also limited in terms of the capacitive load or trace length that they can drive. Typically, trace lengths less than 3 inches are recommended to preserve signal rise/fall times and signal integrity.

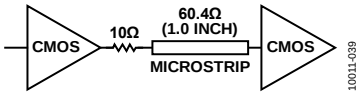


Figure 38. Series Termination of CMOS Output

Termination at the far end of the PCB trace is a second option. The SYNC_OUT CMOS output of the AD9525 does not supply enough current to provide a full voltage swing with a low impedance resistive, far-end termination, as shown in Figure 39. The far-end termination network should match the PCB trace impedance and provide the desired switching point. The reduced signal swing may still meet receiver input requirements in some applications. This can be useful when driving long trace lengths on less critical nets.

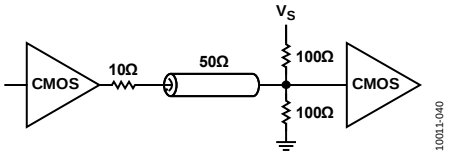


Figure 39. CMOS Output with Far-End Termination

Because of the limitations of single-ended CMOS clocking, consider using differential outputs when driving high speed signals over long traces. The AD9525 offers SYNC_OUT LVPECL outputs that are better suited for driving long traces where the inherent noise immunity of differential signaling provides superior performance for clocking converters.

OUTLINE DIMENSIONS

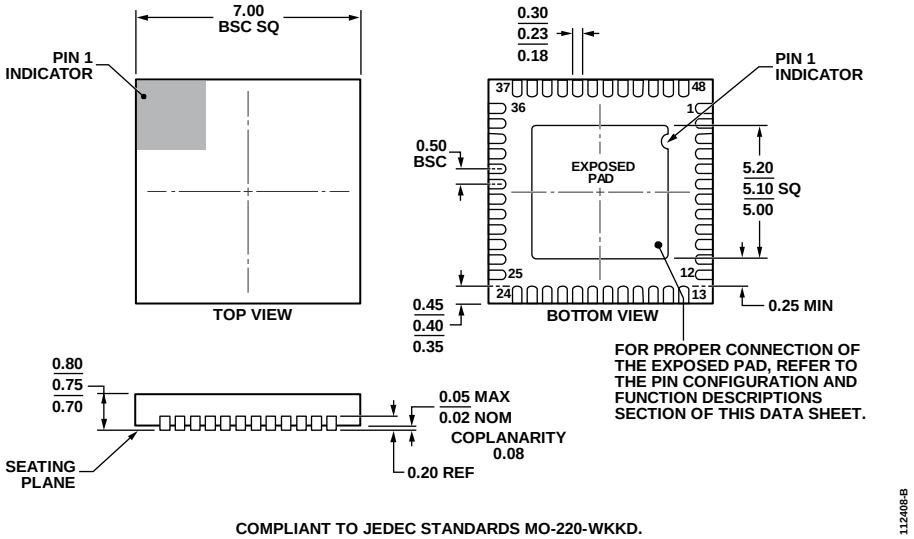


Figure 40. 48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
7 mm × 7 mm Body, Very Very Thin Quad
CP-48-4
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9525BCPZ	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-48-4
AD9525BCPZ-REEL7	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-48-4
AD9525/PCBZ		Evaluation Board, No VCO	
AD9525/PCBZ-VCO		Evaluation Board, 2950 MHz VCO Installed	

[1] Z = RoHS Compliant Part.

NOTES

D10011-0-4/13(A)