CY22381
CY223811

Three-PLL General Purpose Flash Programmable Clock Generator

Features

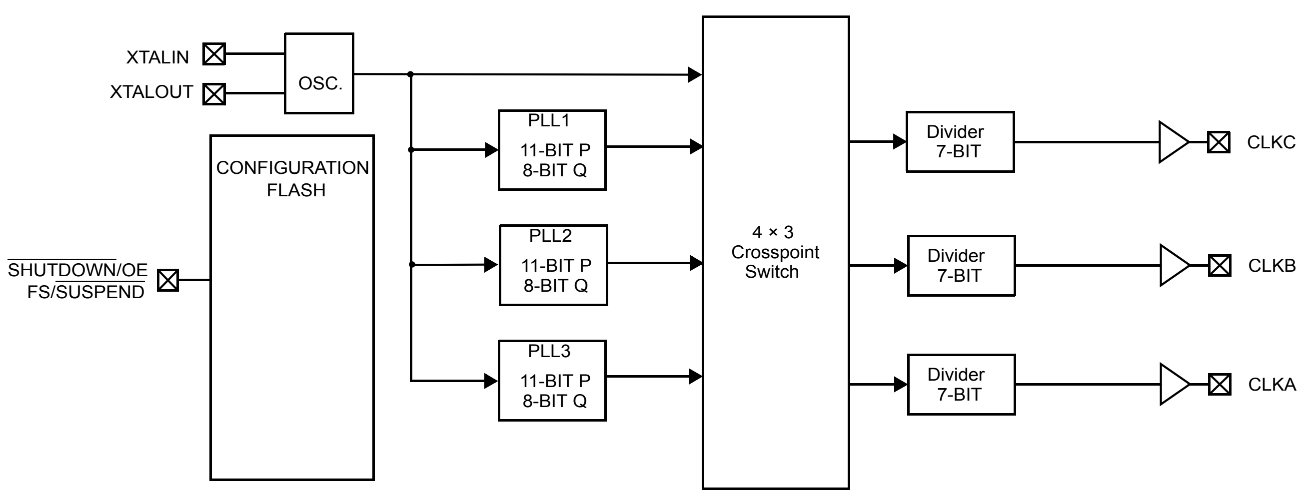
- Three integrated phase-locked loops
- Ultra-wide divide counters (eight-bit Q, eleven-bit P, and seven-bit post divide)
- Improved linear crystal load capacitors
- Flash programmability
- Field programmability
- Low-jitter, high-accuracy outputs
- Power-management options (Shutdown, OE, Suspend)
- Configurable crystal drive strength
- Frequency select option through external LVTTL Input
- 3.3 V operation
- 8-pin small outline integrated circuit (SOIC) package (CY22381)
- 8-pin SOIC package with NiPdAu lead finish (CY223811)
- CyClocks RT™ support

Functional Description

The CY22381 is the next-generation programmable Flash programmable clock for use in networking, telecommunication, datacom, and other general-purpose applications. The CY22381 offers up to three configurable outputs in a 8-pin SOIC, running off a 3.3 V power supply. The on-chip reference oscillator is designed to run off an 8–30-MHz crystal, or a 1–166-MHz external clock signal. The CY22381 has a three PLLs driving 3 programmable output clocks. The output clocks are derived from the PLL or the reference frequency (REF). Output post dividers are available for either. The CY223811 is the CY22381 with NiPdAu lead finish.

For a complete list of related documentation, click here.

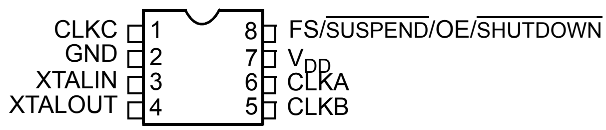
Logic Block Diagram



Contents

Pinouts

Figure 1. 8-pin SOIC pinout



Pin Definitions

Name	Pin Number	Description
CLKC	1	Configurable clock output C
GND	2	Ground
XTALIN	3	Reference crystal input or external reference clock input
XTALOUT	4	Reference crystal feedback (float if XTALIN is driven by external reference clock)
CLKB	5	Configurable clock output B
CLKA	6	Configurable clock output A
V_{DD}	7	Power supply
FS/$\overline{\text{SUSPEND}}$/ $\overline{\text{OE/SHUTDOWN}}$	8	General Purpose Input. Can be Frequency Control, Suspend mode control, Output Enable, or full-chip shutdown.

Operation

The CY22381 is an upgrade to the existing CY2081. The new device has a wider frequency range, greater flexibility, improved performance, and incorporates many features that reduce PLL sensitivity to external system issues.

The device has three PLLs that allow each output to operate at an independent frequencies. These three PLLs are completely programmable.

The CY223811 is the CY22381 with NiPdAu lead finish.

Configurable PLLs

PLL1 generates a frequency that is equal to the reference divided by an eight-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL1 is sent to the crosspoint switch. The frequency of PLL1 can optionally be changed by using the external CMOS general purpose input. See the following section on “General-Purpose Input” for more detail.

PLL2 generates a frequency that is equal to the reference divided by an eight-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL2 is sent to the crosspoint switch.

PLL3 generates a frequency that is equal to the reference divided by an eight-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL3 is sent to the cross-point switch.

General-Purpose Input

The CY22381 features an output control pin (pin 8) that can be programmed to control one of four features.

When programmed as a frequency select (FS), the input can select between two arbitrarily programmed frequency settings. The frequency select can change the following; the frequency of PLL1, the output divider of CLKB, and the output divider of CLKA. Any divider change as a result of switching the FS input is guaranteed to be glitch free.

The general-purpose input can simultaneously control the Suspend feature, turning off a set of PLLs and outputs determined during programming.

When programmed as an output enable (OE) the input forces all outputs to be placed in a three-state condition when LOW.

When programmed as a Shutdown, the input forces a full chip shutdown mode when LOW.

Crystal Input

The input crystal oscillator is an important feature of this device because of its flexibility and performance features.

The oscillator inverter has programmable drive strength. This allows for maximum compatibility with crystals from various manufacturers, processes, performances, and qualities.

The input load capacitors are placed on-die to reduce external component cost. These capacitors are true parallel-plate capacitors for ultra-linear performance. These were chosen to reduce the frequency shift that occurs when non-linear load capacitance interacts with load, bias, supply, and temperature changes. Non-linear (FET gate) crystal load capacitors must not be used for MPEG, communications, or other applications that are sensitive to absolute frequency requirements

The value of the load capacitors is determined by six bits in a programmable register. The load capacitance can be set with a resolution of 0.375 pF for a total crystal load range of 6 pF to 30 pF.

For driven clock inputs the input load capacitors may be completely bypassed. This enables the clock chip to accept driven frequency inputs up to 166 MHz. If the application requires a driven input, then XTALOUT must be left floating.

Crystal Drive Level and Power

Crystals are specified to accept a maximum drive level. Generally, larger crystals can accept more power. The drive level specification in the table below is a general upper bound for the power driven by the oscillator circuit in the CY22381.

For a given voltage swing, power dissipation in the crystal is proportional to ESR and proportional to the square of the crystal frequency. (Note that actual ESR is sometimes much less than the value specified by the crystal manufacturer.) Power is also almost proportional to the square of C_L.

Power can be reduced to less than the DL specification in the table below by selecting a reduced frequency crystal with low C_L and low R_1 (ESR).

Output Configuration

Under normal operation there are four internal frequency sources that may be routed through a programmable crosspoint switch to any of the three outputs through programmable seven-bit output dividers. The four sources are: reference, PLL1, PLL2, and PLL3. The following is a description of each output.

CLKA's output originates from the crosspoint switch and goes through a programmable seven-bit post divider. The seven-bit post divider derives its value from one of two programmable registers controlled by FS.

CLKB's output originates from the crosspoint switch and goes through a programmable seven-bit post divider. The seven-bit post divider derives its value from one of two programmable registers controlled by FS.

CLKC's output originates from the crosspoint switch and goes through a programmable seven-bit post divider. The seven-bit post divider derives its value from one programmable register.

The Clock outputs have been designed to drive a single point load with a total lumped load capacitance of 15 pF. While driving multiple loads is possible with the proper termination, it is generally not recommended.

Power-Saving Features

When configured as OE, the general-purpose input three-states all outputs when pulled LOW. When configured as Shutdown, a LOW on this pin three-states all outputs and shuts off the PLLs, counters, the reference oscillator, and all other active components. The resulting current on the V_{DD} pins is less than 5 µA (typical). After leaving shutdown mode, the PLLs has to relock.

When configured as $\overline{\text{SUSPEND}}$, the general-purpose input can be configured to shut down a customizable set of outputs and/or PLLs, when LOW. All PLLs and any of the outputs can be shut off in nearly any combination. The only limitation is that if a PLL is shut off, all outputs derived from it must also be shut off. Suspending a PLL shuts off all associated logic, while suspending an output forces a three-state condition.

Improving Jitter

Jitter optimization control is useful in mitigating problems related to similar clocks switching at the same moment and causing excess jitter. If one PLL is driving more than one output, the negative phase of the PLL can be selected for one of the outputs. This prevents the output edges from aligning, allowing superior jitter performance.

CyClocks RT Software

CyClocks RT is our second-generation application that allows users to configure this device. The easy-to-use interface offers complete control of the many features of this family including input frequency, PLL and output frequencies, and different functional options. Data sheet frequency range limitations are checked and performance tuning is automatically applied. You can download a free copy of CyClocks RT on Cypress's web site at http://www.cypress.com.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Supply voltage ....–0.5 V to +7.0 V

DC input voltage ....–0.5 V to + (V_{DD} + 0.5 V)

Storage temperature .... –65 °C +125 °C

Junction temperature .... 125 °C

Data retention at Tj = 125 °C ....> 10 years

Maximum programming cycles 100

Package power dissipation .... 250 mW

Static discharge voltage
(per MIL-STD-883, Method 3015) .... ≥ 2000V

Latch up (per JEDEC 17) .... ≥ ±200 mA

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	Supply voltage	3.135	3.3	3.465	V
T_A	Commercial operating temperature, ambient	0	–	+70	°C
	Industrial operating temperature, ambient	–40	–	+85	°C
C_{LOAD_OUT}	Max. load capacitance	–	–	15	pF
f_{REF}	External reference crystal	8	–	30	MHz
	External reference clock [1], Commercial	1	–	166	MHz
	External reference clock [1], Industrial	1	–	150	MHz
t_{PU}	Power up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

Electrical Characteristics

Parameter	Description	Conditions [2]	Min	Typ	Max	Unit
I_{OH}	Output high current [3]	$V_{OH} = V_{DD} - 0.5$, V_{DD} = 3.3 V	12	24	–	mA
I_{OL}	Output low current [3]	V_{OL} = 0.5 V, V_{DD} = 3.3 V	12	24	–	mA
C_{XTAL_MIN}	Crystal load capacitance [3]	Capload at minimum setting	–	6	–	pF
C_{XTAL_MAX}	Crystal load capacitance [3]	Capload at maximum setting	–	30	–	pF
C_{IN}	Input pin capacitance [3]	Except crystal pins	–	7	–	pF
V_{IH}	HIGH-level input voltage	CMOS levels,% of V_{DD}	70%	–	–	V_{DD}
V_{IL}	LOW-level input voltage	CMOS levels,% of V_{DD}	–	–	30%	V_{DD}
I_{IH}	Input HIGH current	$V_{IN} = V_{DD} - 0.3$ V	–	<1	10	µA
I_{IL}	Input LOW current	V_{IN} = +0.3 V	–	<1	10	µA
I_{OZ}	Output leakage current	Three-state outputs	–	–	10	µA
I_{DD}	Total power supply current	3.3 V Power supply; 3 outputs at 50 MHz	–	35	–	mA
		3.3 V Power supply; 3 outputs at 166 MHz	–	70	–	mA
I_{DDS}	Total power supply current in shutdown mode	Shutdown active	–	5	20	µA

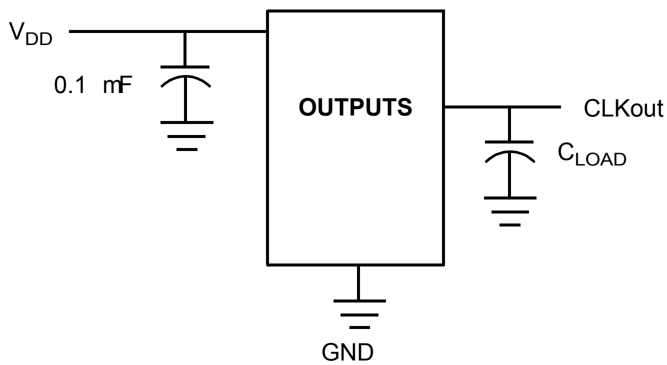
Notes
1. External input reference clock must have a duty cycle between 40% and 60%, measured at V_{DD}/2.
2. Unless otherwise noted, Electrical and Switching Characteristics are guaranteed across these operating conditions.
3. Guaranteed by design, not 100% tested.

Recommended Crystal Specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode	8	–	30	MHz
C_{LNOM}	Nominal load capacitance		8	–	20	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	–	–	50	Ω
DL	Crystal drive level	No external series resistor assumed	–	0.5	2	mW

Test Circuit

Figure 2. Test Circuit



Switching Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$1/t_1$	Output frequency [4, 5]	Clock output limit, commercial	–	–	200	MHz
		Clock output limit, industrial	–	–	166	MHz
t_2	Output duty cycle [4, 6]	Duty cycle for outputs, defined as $t_2 \div t_1$, Fout < 100 MHz, divider >= 2, measured at $V_{DD}/2$	45%	50%	55%	
		Duty cycle for outputs, defined as $t_2 \div t_1$, Fout > 100 MHz or divider = 1, measured at $V_{DD}/2$	40%	50%	60%	
t_3	Rising edge slew rate [4]	Output clock rise time, 20% to 80% of V_{DD}	0.75	1.4	–	V/ns
t_4	Falling edge slew rate [4]	Output clock fall time, 20% to 80% of V_{DD}	0.75	1.4	–	V/ns
t_5	Output three-state timing [4]	Time for output to enter or leave three-state mode after SHUTDOWN/OE switches	–	150	300	ns
t_6	Clock jitter [4, 7]	Peak-to-peak period jitter, CLK outputs measured at $V_{DD}/2$	–	200	–	ps
t_7	Lock time [4]	PLL Lock Time from Power up	–	1.0	3	ms

Notes
4. Guaranteed by design, not 100% tested.
5. Guaranteed to meet 20%–80% output thresholds and duty cycle specifications.
6. Reference Output duty cycle depends on XTALIN duty cycle.
7. Jitter varies significantly with configuration. Reference Output jitter depends on XTALIN jitter and edge rate.

Switching Waveforms

Figure 3. All Outputs, Duty Cycle and Rise and Fall Time

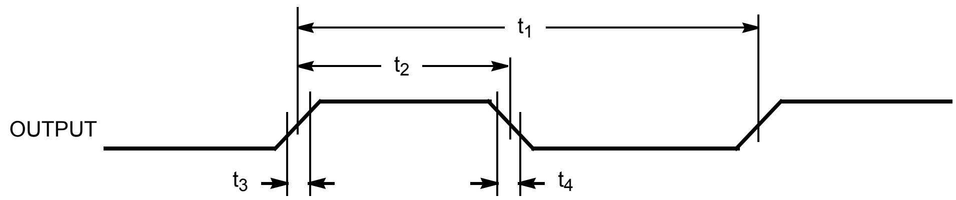


Figure 4. Output Three-State Timing

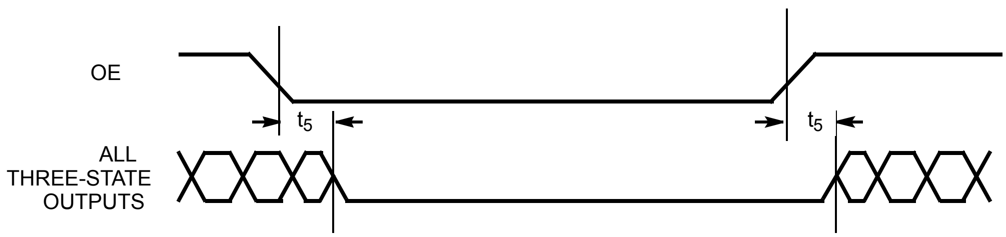


Figure 5. CLK Output Jitter

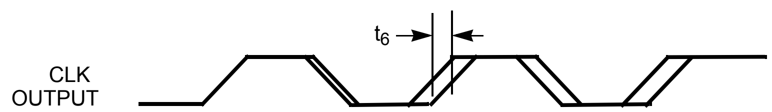
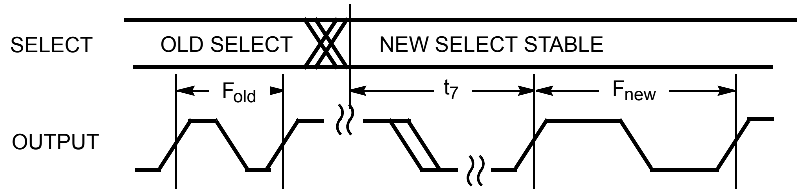


Figure 6. Frequency Change



Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
Pb-free			
CY223811FXI	8-pin SOIC with NiPdAu lead frame	Industrial (T_A = –40 °C to 85 °C)	3.3 V
CY22381FXC[10]	8-pin SOIC	Commercial (T_A = 0 °C to 70 °C)	3.3 V
CY22381FXCT	8-pin SOIC – Tape and Reel	Commercial (T_A = 0 °C to 70 °C)	3.3 V
CY22381FXI	8-pin SOIC	Industrial (T_A = –40 °C to 85 °C)	3.3 V
CY22381FXIT	8-pin SOIC – Tape and Reel	Industrial (T_A = –40 °C to 85 °C)	3.3 V
Programmer			
CY3672-USB	Programmer		
CY3699	CY22381F Adapter for CY3672-USB		

Some product offerings are factory programmed customer specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or Sales Representative for more information.

Possible Configurations

Ordering Code	Package Type	Operating Range	Operating Voltage
CY22381SI-xxxT[8, 9]	8-pin SOIC – Tape and Reel	Industrial (T_A = –40°C to 85°C)	3.3 V
Pb-free			
CY22381SXC-xxx[8]	8-pin SOIC	Commercial (T_A = 0 °C to 70 °C)	3.3 V
CY22381SXC-xxxT[8]	8-pin SOIC – Tape and Reel	Commercial (T_A = 0 °C to 70 °C)	3.3 V
CY22381SXI-xxx[8]	8-pin SOIC	Industrial (T_A = –40 °C to 85 °C)	3.3 V
CY22381SXI-xxxT[8]	8-pin SOIC – Tape and Reel	Industrial (T_A = –40 °C to 85 °C)	3.3 V

Notes

8. The CY22381SI-xxx, CY22381SXC-xxx and CY22381SXI-xxx are factory programmed configurations. Factory programming is available for high-volume design opportunities of 100Ku/year or more in production. For more details, contact your local Cypress FAE or Cypress Sales Representative.
9. Not recommended for new designs.
10. The CY22381FSZC and CY22381FXC are identical. For new designs, use CY22381FXC.

Ordering Code Definitions

CY 22381 X X X X X (-xxx) X

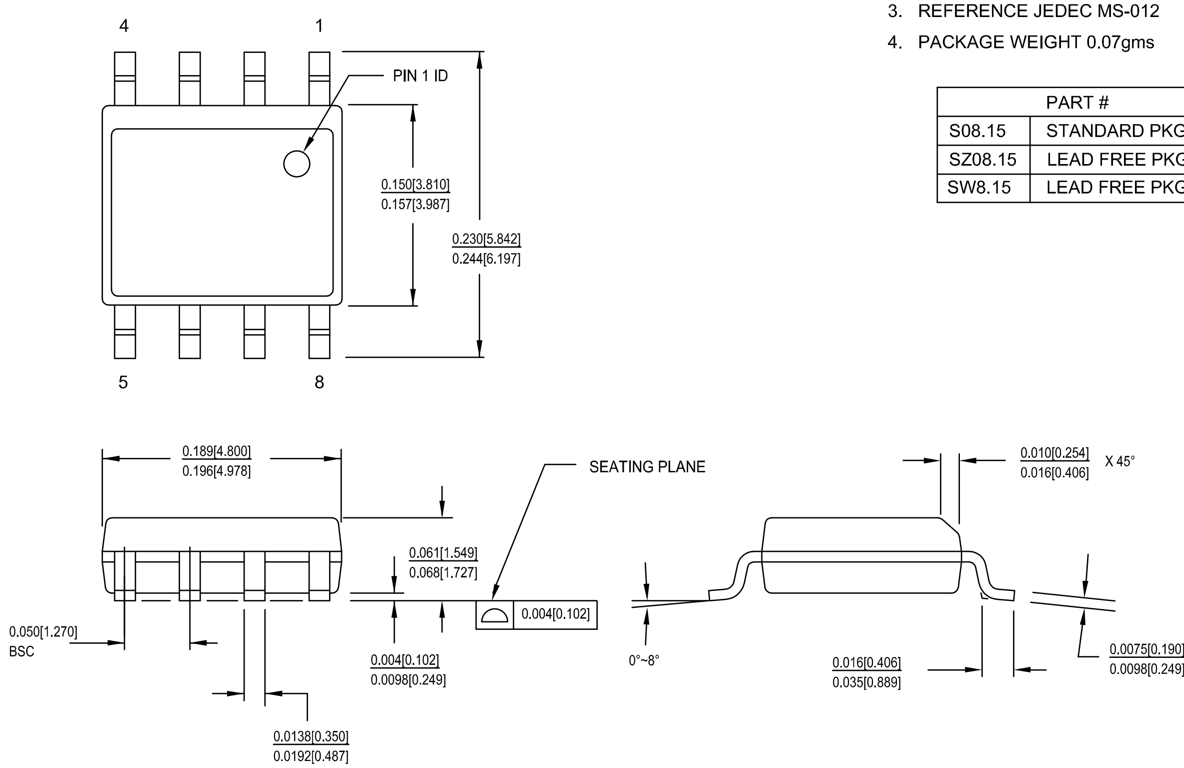
- X = blank or T
  blank = tube; T = tape and Reel
- Configuration specific identifier (factory programmed)
- Temperature Range: X = I or C
  I = Industrial; C = Commercial
- Pb-free
- Package: X = blank or S
  S = 8-pin SOIC
  X = 8-pin SOIC
- X = F or blank
  F = field programmable; blank = factory programmed
- Lead finish: X = 1 or blank
  1 = NiPdAu; blank = unspecified
- Part Identifier
- Company ID: CY = Cypress

Package Drawing and Dimensions

Figure 7. 8-pin SOIC (150 Mils) Package Outline, 51-85066

1. DIMENSIONS IN INCHES[MM] MIN. / MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG



51-85066 *H

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESR	Equivalent Series Resistance
FET	Field Effect Transistor
MPEG	Motion Picture Experts Group
OE	Output Enable
PLL	Phase-Locked Loop
SOIC	Small Outline Integrated Circuit

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µF	microfarad
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
pF	picofarad
ps	picosecond
V	volt

Document History Page

Document Title: CY22381/CY223811, Three-PLL General Purpose Flash Programmable Clock Generator Document Number: 38-07012				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	106737	TLG	07/03/01	New data sheet.
*A	108514	JWK	08/23/01	Updated based on characterization results. Removed "Preliminary" heading Removed soldering temperature rating. Split crystal load into two typical specs representing digital settings range. Changed t_5 max to 300 ns Changed t_6 typical to 200 ps. Changed t_7 typical to 1.0 ms
*B	110053	CKN	12/10/01	Changed status from Preliminary to Final.
*C	121863	RBI	12/14/02	Added power up requirements to Operating Conditions information
*D	279431	RGL	See ECN	Added lead-free devices
*E	2584052	AESA	10/10/08	Added Note 8 and 9. Added part number CY22381FC, CY22381FCT, CY3672-USB, CY3699, CY22381FSZC in ordering information table. Removed part number CY22381FI, CY22381FIT, CY22381SC-xxx, CY22381SC-xxxT, CY22381SI-xxx, and CY22381SI-xxxT in Ordering Information table. Added CY223811FXI (NiPdAu lead finish). Changed Lead-Free to Pb-Free. Updated template.
*F	2620588	KVM / AESA	12/11/08	Add CY223811 to the document title Distinguish between CY22381 and CY223811 in page 1 Features section Add part number CY22381SI-xxxT in Ordering Information table.
*G	2897317	KVM	03/22/10	Removed obsolete parts from Ordering Information table and moved 'xx' parts to Possible Configurations table Updated package diagram
*H	3065190	KVM / BASH	01/17/11	Removed Benefits section and replaced with Functional Description section. Added Crystal Drive Level and Power. Added crystal parameter table. Removed FTG from CY3672. Added Ordering Code Definitions under Ordering Information. Added Acronyms and Units of Measure.
*I	3259420	BASH	05/17/2011	Updated as per template
*J	4392214	AJU	05/28/2014	Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *D to *F. Updated to new template. Completing Sunset Review.
*K	4576237	AJU	11/21/2014	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end.
*L	5804057	TAVA	07/07/2017	Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *F to *H. Updated to new template. Completing Sunset Review.

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