Evaluation Board for AD9513/AD9514/ AD9515 Clock Distribution ICs

AD9513/PCB, AD9514/PCB, AD9515/PCB

EVALUATION BOARD DESCRIPTION

This data sheet describes the evaluation board for the AD9513, AD9514, and AD9515 clock distribution ICs.

To properly use the evaluation board, please also reference the current data sheet for the appropriate part. The current data sheet is available on the Analog Devices' website located at www.analog.com/clocks.

DEVICE DESCRIPTION

The AD9513, AD9514, and AD9515 clock ICs provide multi-output clock distribution in a design that emphasizes low jitter and phase noise to maximize data converter performance. Other applications with demanding phase noise and jitter requirements also benefit from these parts.

The AD9513 offers three independent clock outputs, selectable as either LVDS or CMOS levels. The AD9514 provides three outputs, two of which are LVPECL outputs, while the third can be set to either LVDS or CMOS. The AD9515 offers two independent clock outputs, one as LVPECL, the other is selectable as either LVDS or CMOS levels.

The LVPECL outputs operate to 1.6 GHz, the LVDS outputs operate to 800 MHz, and the CMOS outputs operate to 250 MHz.

Each output has a programmable divider, which can be set to divide by a selected set of integers ranging from 1 to 32. The phase of one clock output relative to another clock output is set by means of a divider phase select function that serves as a coarse timing adjustment.

The LVDS/CMOS outputs feature a delay element with three selectable full-scale delay values (1.8 ns, 6.0 ns, and 11.6 ns), each with 16 steps of fine adjustment.

The AD9513/AD9514/AD9515 clock ICs do not require an external controller for operation or setup. These devices are programmed by means of 11 pins (S0 to S10) using 4-level logic. The required logic levels are provided by the parts.

EVALUATION BOARD DIGITAL PICTURE

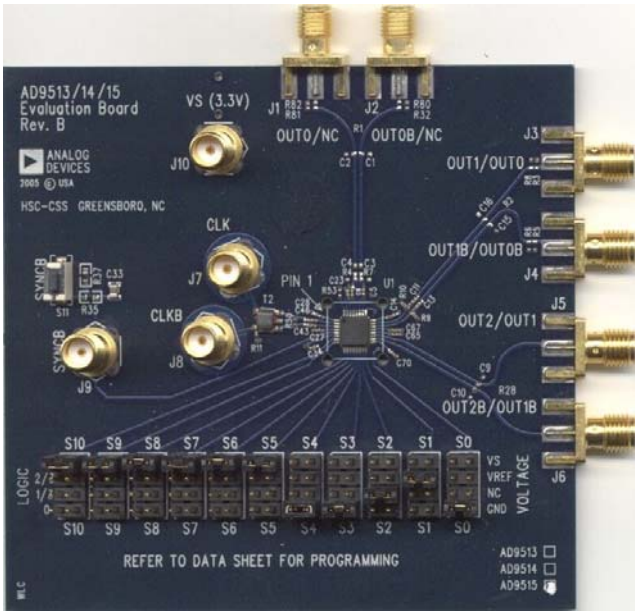

Figure 1.

Rev. 0

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REVISION HISTORY

2/06—Revision 0: Initial Version

SETTING UP THE EVALUATION BOARD

HARDWARE

The AD9513/AD9514/AD9515 evaluation board requires a 3.3 V power supply. Some form of input clock must be provided, usually from a signal generator. A high speed oscilloscope is helpful in order to see the waveforms present at the clock outputs.

SOFTWARE

No software is required to program the AD9513/AD9514/AD9515. All of the programming of the part is provided by the headers and shunts on the evaluation board itself (see the Programming the Board section).

PROGRAMMING THE BOARD

The digital logic on the AD9513/AD9514/AD9515 is completely combinational and controlled by the 11 pins labeled S0 to S10. Each of these pins must be set to one of four voltage levels (four-state logic). A set of four-position headers is provided to allow for programming the part using removable shunts.

Four-State Digital Logic

Table 1 shows the four-state digital logic inputs and their logic levels and voltages.

Table 1. Four-State Digital Logic Voltage Settings

Logic	Input	Voltage	Description
1	V_S	3.3 V	Tie pin to V_S.
⅔	VREF	⅔ (V_S)	Internally generated voltage reference provided at Pin VREF. Can drive up to all of the logic inputs. Do not use for other purposes.
⅓	N/C	⅓ (V_S)	Internal self-bias of pin. Leave pin as no connect.
0	GND	0 V	Tie pin to ground.

The ⅔ (V_S) voltage is set by connecting the input to the VREF pin on the chip. The ⅓ (V_S) voltage is obtained by not driving the input pin at all, thus allowing it to self-bias.

To program the AD9513/AD9514/AD9515 evaluation board, first determine the logic levels/voltages that should be applied to the digital inputs. A programming reference appears in the data sheet. Set each of the programming pins (S0 to S10) to the appropriate logic level by attaching a shunt to the proper position on each of the four-position headers.

To the left of the row of headers, a label indicates the logic level of each row of pins. To the right of the row of headers, a corresponding label indicates the voltage level of each row of pins. Note that the row corresponding to a logic level of ⅓ shows that the connection is N/C. When the ⅓ logic level is needed, the shunt should be placed on the pins, but there is no connection to the device pin for this logic level.

To program the AD9513 to have all outputs on in LVDS mode, for example, the S2 and S1 programming pins must be set to ⅓ (V_S). On the AD9513/AD9514/AD9515 evaluation board, locate the 4-position headers that correspond to digital inputs S2 and S1. Then, referring to the label to the left side of the row of headers, attach the shunts across the pins corresponding to the marking for logic level ⅓. Note that the label to the right of the row of headers indicates that this is an N/C as far as voltage is concerned.

CONFIGURING THE BOARD

INPUTS

Clock Input

The input clock is configured to receive a single-ended signal from bench hardware and convert it to a differential signal at the part. This is done by a balun, terminated with a 50 Ω resistor, followed by coupling capacitors on both the true and complimentary inputs of the part.

SYNCB Circuit

The SYNCB input allows a sync pulse to be produced without requiring external circuitry. The evaluation board is populated with both a momentary switch and an SMA connector labeled SYNCB. To create a SYNCB signal, depress the momentary switch. To release the SYNCB signal, release the momentary switch.

An external SYNCB signal can also be applied to the evaluation board through a cable connected to the SMA connector labeled SYNCB.

OUTPUTS

AD9513

The AD9513 has three LVDS/CMOS outputs. These outputs are all terminated with a 100 Ω resistor on the evaluation board with the assumption that LVDS is selected. To use CMOS outputs, this 100 Ω resistor should be removed.

AD9514

The AD9514 has two LVPECL output and one LVDS/CMOS outputs. OUT0 and OUT1 are both LVPECL. Each LVPECL output is terminated with a 200 Ω resistor to ground, followed by an ac coupling capacitor. There are pads for an alternate termination scheme on the evaluation board. This alternate scheme creates a Thevenin equivalent 50 Ω termination to V_S – 2 V. This scheme is utilized by removing the 200 Ω resistors to ground, replacing the ac coupling cap with a 0 Ω resistor and adding the appropriate termination resistors. These resistors attach to the pads located near the SMA connectors.

The LVDS/CMOS output (OUT2) is terminated with a 100 Ω resistor on the evaluation board with the assumption that LVDS is selected. To use CMOS outputs, this 100 Ω resistor should be removed.

AD9515

The AD9515 has the same default termination scheme and options as the AD9514. The only difference is that the AD9515 has only one LVPECL output, and one LVDS/CMOS output.

SCHEMATICS

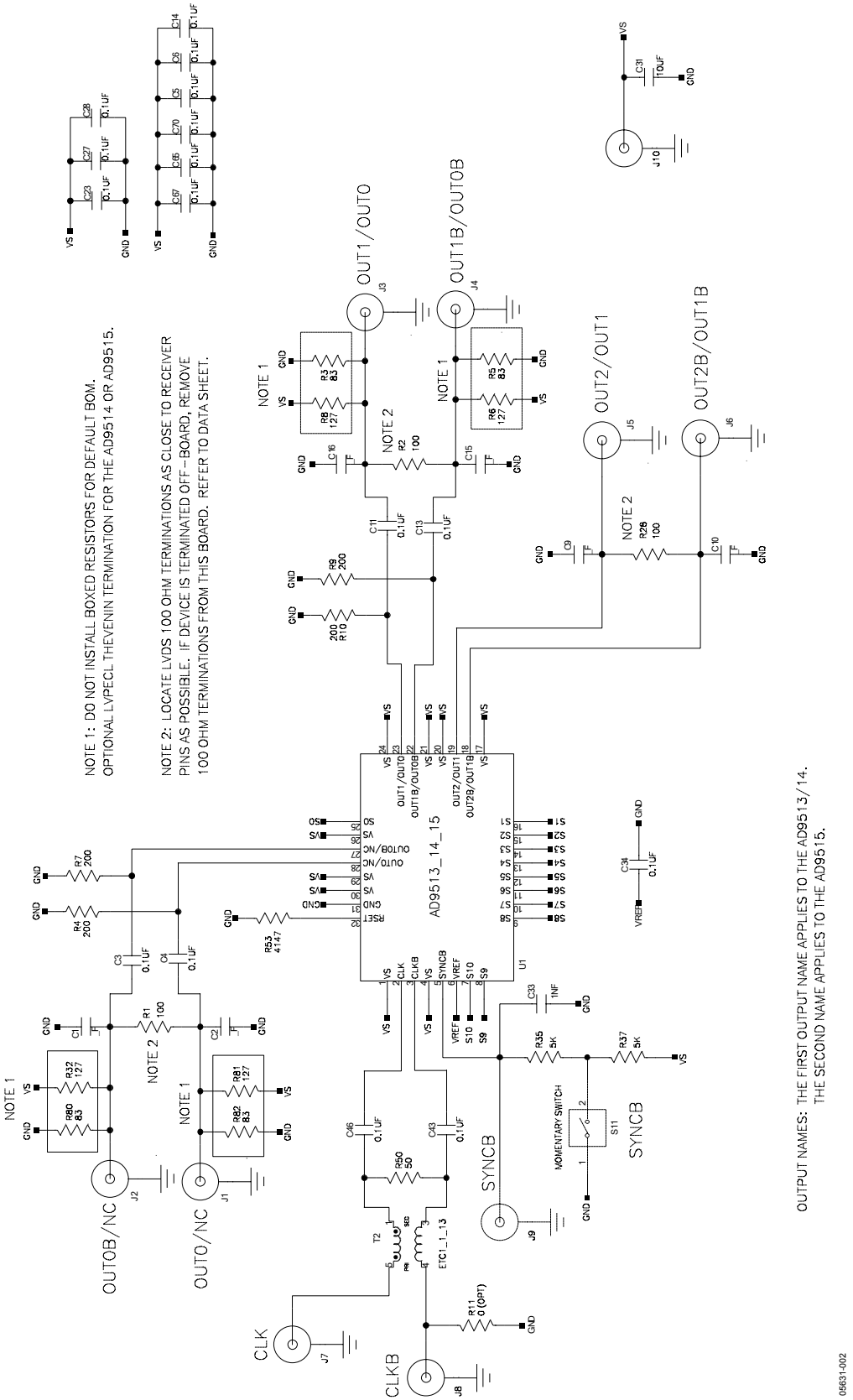

Figure 2. AD9513/AD9514/AD9515 Evaluation Board Schematic, Page 1

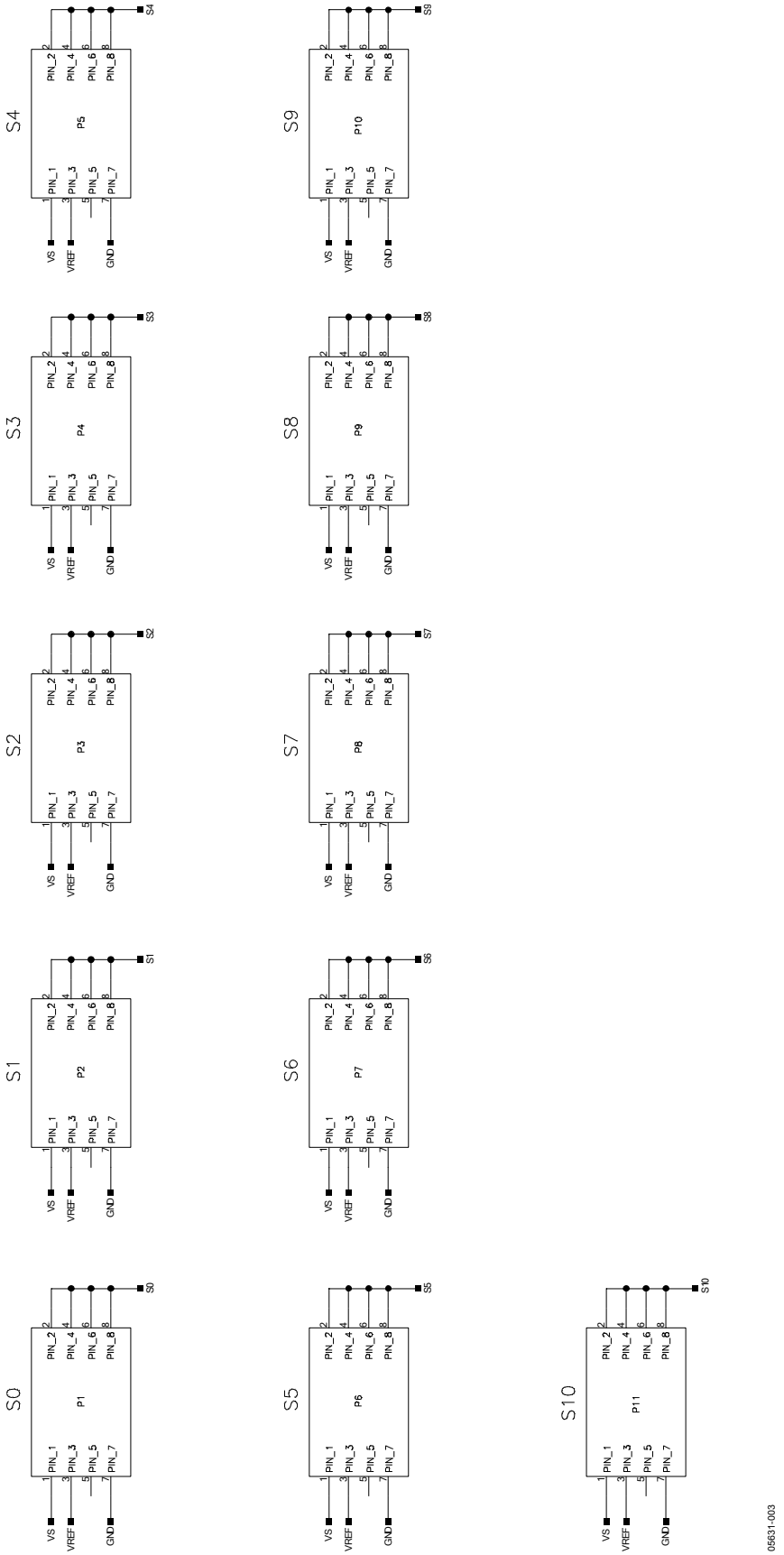

Figure 3. AD9513/AD9514/AD9515 Evaluation Board Schematic, Page 2

ORDERING INFORMATION

ORDERING GUIDE

Model	Description
AD9513/PCB	Evaluation Board
AD9514/PCB	Evaluation Board
AD9515/PCB	Evaluation Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

NOTES

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