12-Bit A/D Converter

AD1671

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. This brochure can be found at: http://www.analog.com/aerospace

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD1671.

2.0 Part Number. The complete part number(s) of this specification follow:

Part Number	Description
AD1671-703D	12-Bit A/D Converter
AD1671-703F	12-Bit A/D Converter
AD1671-713F	12-Bit A/D Converter with radiation test

2.1. Case Outline:

Letter	Descriptive	Designator Case Outline (Lead Finish per MIL-PRF-38535)
D	CDIP2-T28	28-Lead sidebrazed DIP (.6")
F	CDFP3-F28	28-Lead bottom-brazed flatpack

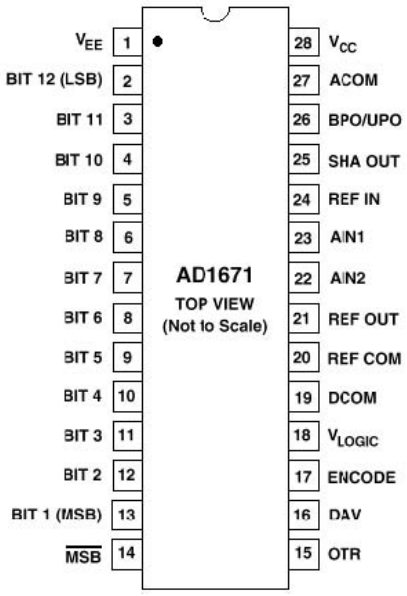

Figure 1 - Terminal connections.

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3.0 Absolute Maximum Ratings. (T_A = 25°C, unless otherwise noted)

V_{CC} to ACOM.....-0.5V to +6.5V
V_{EE} to ACOM.....-6.5V to +0.5V
V_{LOGIC} to DCOM.....-0.5V to +6.5V
ACOM to DCOM.....-1.0V to +1.0V
V_{CC} to V_{LOGIC} .....-6.5V to +6.5V
ENCODE to DCOM.....-0.5V to V_{LOGIC} +0.5V
REF IN, BPO/UPO to ACOM .....-0.5V to V_{CC} +0.5V
AIN to ACOM.....-11V to +11V
Power Dissipation 1000mW
Operating Temperature Range.....-55°C to +125°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (Soldering, 60 sec.) .....+300°C
Junction Temperature (T_J).....+150°C

3.1. Thermal Characteristics:

Thermal Resistance, SBDIP (D) Package
Junction-to-Case (Θ_{JC}) = 28°C/W Max
Junction-to-Ambient (Θ_{JA}) = 60°C/W Max
Thermal Resistance, Bottom brazed (F) Package
Junction-to-Case (Θ_{JC}) = 22°C/W Max
Junction-to-Ambient (Θ_{JA}) = 60°C/W Max

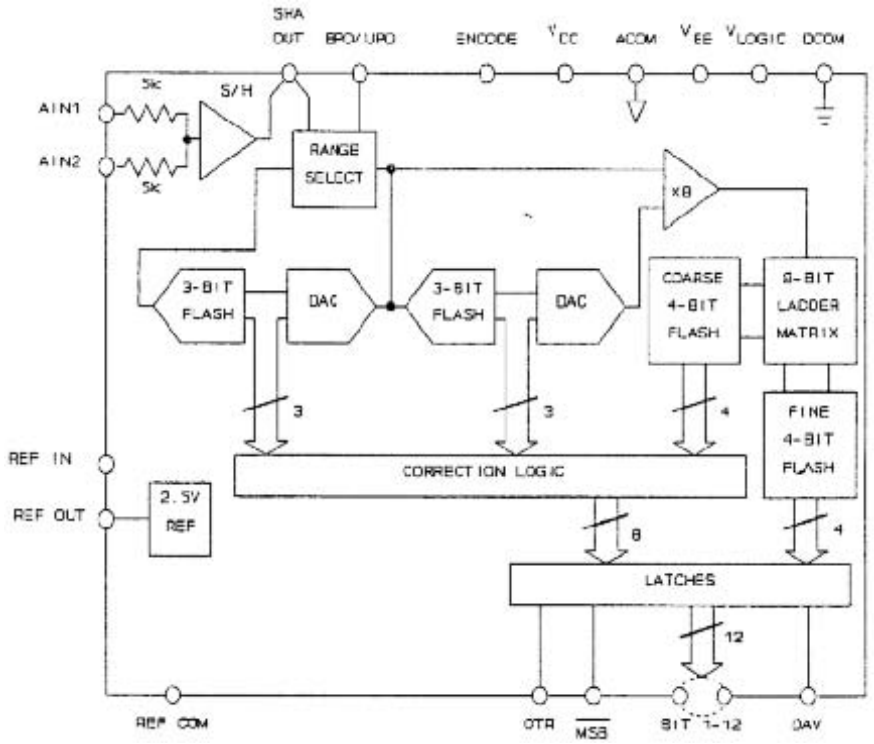


Figure 2. Functional block diagram

4.0 Electric Table:

Table I

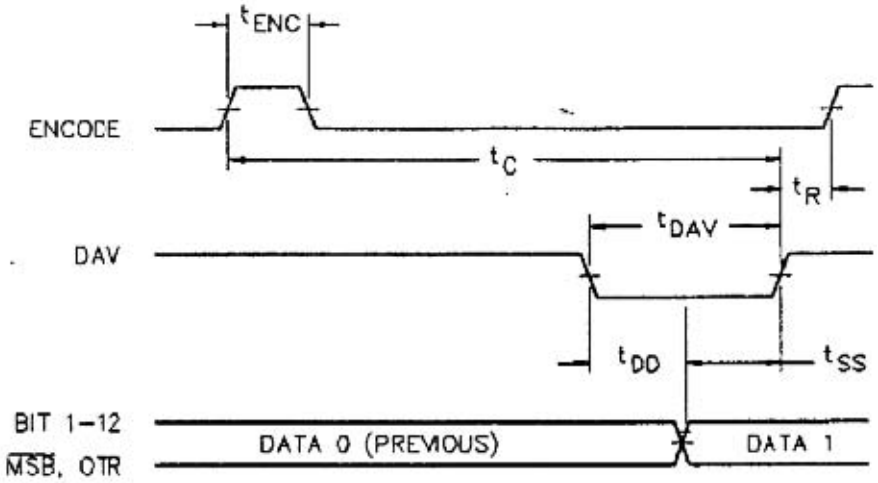
Parameter See notes at end of table	Symbol	Conditions Note 1/		Sub-group	Limit Min	Limit Max	Units
Resolution	RES			1, 2, 3		12	Bits
Integral nonLinearity	INL	All codes histogram		1	-2.5	2.5	LSB
				2, 3	-3	3	LSB
Differential nonLinearity	+DNL	All codes histogram		1, 2, 3	0	2	LSB
	-DNL				-1	0	LSB
Unipolar offset error	V_{OSE}	2.5V, 5V span		1	-9	9	LSB
Unipolar offset drift	TC_{VOS}	2.5V, 5V span T_A = -55ºC, +125ºC		2,3		20	±ppm/° C
Gain Error	A_E	Unipolar & bipolar		1		0.37	%FSR
Gain drift	TC_A	Unipolar & Bipolar T_A = -55ºC, +125ºC		2,3		40	±ppm/° C
Bipolar zero error	B_{POE}	2.5V, 5V span		1	-10	10	LSB
Bipolar zero drift	TC_{BPO}	2.5V, 5V span T_A = -55ºC, +125ºC		2,3		30	±ppm/° C
Analog input ranges	V_{IN}	Unipolar Mode	Rin=10MΩ 3/	1,2,3		2.5	V
			Rin=10KΩ 3/	1,2,3		5	
		Bipolar Mode	Rin=10MΩ 3/	1,2,3		2.5	
			Rin=10KΩ 3/	1,2,3		5	
Reference voltage 4/	V_{RO}	Unipolar & Bipolar 2/		1	2.475	2.525	V
Reference drift	TC_{VRO}	Unipolar & Bipolar 2/ T_A = -55°C, +125°C		2,3		30	±ppm/° C
Reference Current	I_{REF}	Unipolar Mode 2/		1		2.5	mA
		Bipolar Mode 2/		1		1	
Power dissipation	P_D	V_S = ±5.25V, V_{LOGIC} = +5.5V		1,2,3		750	mW
Power Supply Current	I_{CC}	Tested under static conditions		1,2,3		75	mA
	I_{EE}					-75	
	I_{LOGIC}					5	
PSRR	V_{CC}	Full-Scale Change measured		1,2,3	-4	4	LSB
	V_{EE}						
	V_{LOGIC}						
Input Logic voltages	V_{IH}	Encode Input		1,2,3	2.0		V
	V_{IL}					0.8	
Input Logic Current	I_{IH}			1,2,3	-10	10	µA
	I_{IL}						
Output Logic Voltage	V_{OH}	I_{OH} = 500µA		1,2,3	2.4		V
	V_{OL}	I_{OL} = 1.6mA				0.4	
Output Logic Current	I_{OH}			1,2,3		500	µA
	I_{OL}				-1.6		mA
Signal to noise plus distortion	SINAD	f_{IN} = 100KHz, f_S = 1MHz, -0.5 dB input		4,5,6	68		dB
Effective number of bits	ENOB			4	11		Bits
Total harmonic distortion	THD			4,5,6		-73	dB
Peak spurious of peak harmonic component	PS			4,5,6		-75	
Intermodulation distortion	$\Sigma 2^{nd}$	2^{nd} order products		4,5,6		-75	
	$\Sigma 3^{rd}$	3^{rd} order products					
Conversion time	T_{CONV}	See figure 3		9,10,11		800	ns
Sample Rate	Fs	2/		9,10,11		1.25	MSPS

Table I (Continued)

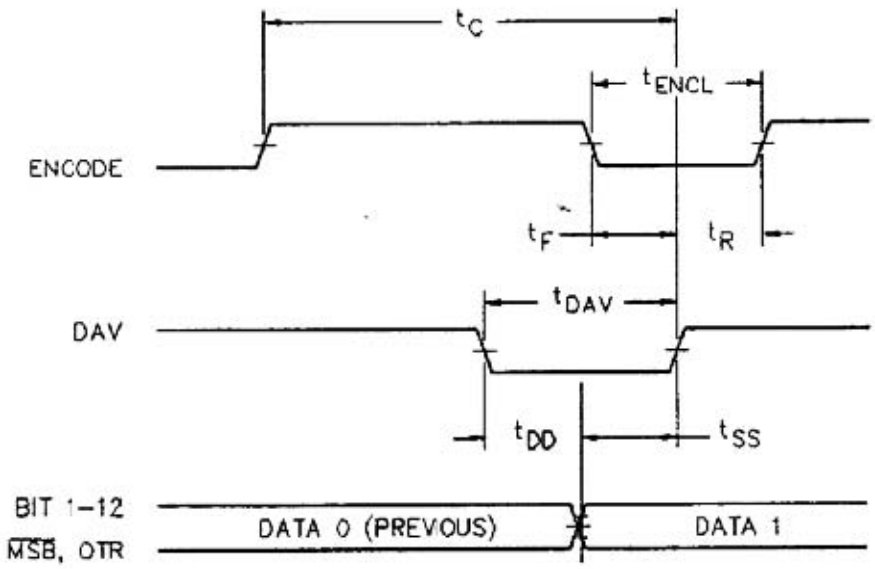
Parameter See notes at end of table	Symbol	Conditions Note 1/	Sub-group	Limit Min	Limit Max	Units
Encode width high (short encode)	t_{ENC}	See figure 3 2/	9,10,11	20	50	ns
Encode width Low (long encode)	t_{ENCL}	See figure 3 2/	9,10,11	20		
DAV pulse width	t_{DAV}	See figure 3	9,10,11	150	300	
Encode falling edge delay	t_F	See figure 3 2/	9	0		
Start new conversion delay	t_R	See figure 3 2/	9	0		
Data and QTR delay from DAV falling edge	t_{DD}	See figure 3 2/	9	20		
Data and OTR delay from DAV rising edge	t_{SS}	See figure 3 2/	9	20		

TABLE I NOTES:

1/	V_{CC} = +5V, V_{EE} = -5V, V_{LOGIC} = +5V, unless otherwise specified.
2/	This parameter is guaranteed, but not necessarily tested.
3/	R_{IN} values are typical values only.
4/	The AD1671 includes an onboard +2.5 V reference. The reference input pin (REF IN) can be connected to reference output pin (REF OUT) or a standard external +2.5 V reference can be selected to meet specific system requirements. Fast switching input dependent currents are modulated at the reference input. The reference input voltage can be held with the use of a capacitor. To prevent the AD1671's onboard reference from oscillating when not connected to REF IN, REF OUT must be connected to +5 V. It is possible to connect REF OUT to +5 V due to its output circuit implementation which shuts down the reference



Encode Pulse High
Figure 3.Timing Diagrams



Encode Pulse Low
Figure 3.Timing diagram.

4.1. Electrical Test Requirements:

Table II	
Test Requirements	**Subgroups (in accordance with MIL-PRF-38535, Table III)**
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3,4,5,6 9, 10, 11 1/ 2/
Group A Test Requirements	1, 2, 3,4,5,6,9, 10, 11
Group C end-point electrical parameters	1 2/
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

1/ PDA applies to Subgroup 1 only. Deltas excluded from PDA.
2/ See table III for delta parameters.

4.2. Table III. Lifetest / Burn-in delta limits.

Table III				
TEST TITLE	**BURN-IN ENDPOINT**	**LIFETEST ENDPOINT**	**DELTA**	**UNITS**
I_{CC}	75	75	± 7.5	mA max
V_{OH}	2.4	2.4	± 0.24	V min
V_{OL}	0.4	0.4	± 0.1	V max

5.0 Life Test/Burn-In Circuit:

5.1 HTRB is not applicable for this drawing.

5.2 Burn-in is per MIL-STD-883 Method 1015, test condition B.

5.3 Steady state life test is per MIL-STD-883 Method 1005, test condition B.

Rev	Description of Change	Date
A	Initiate	Feb. 29, 2000
B	Add flatpack. Add radiation part number. Exclude Delta's from PDA. Delete reference to unused subgroups in table II. Update Table III.	Aug. 21, 2001
C	Update web address.	Feb. 14, 2002
D	Change Table I AC parameters from subgroups 1, 2, 3 to subgroups 9, 10, 11. (SINAD, THD, PS, Σ2nd and Σ 3^{RD})	Jan. 9, 2003
E	Delete burn-in circuit	Aug. 5, 2003
F	Change TCVOS, TCA, TCBPO, TCVRO from subgroups 2, 3 to subgroup 8. Add subgroup 8 to Table II.	Jun. 14, 2004
G	Update header/footer and add to 1.0 Scope description.	Feb. 12, 2008
H	Add Junction Temperature (T_J).....+150°C	April 4, 2008
I	Change subgroup for ENOB to 9	Aug. 3, 2009
J	Match DNL limits and units to actual production test plus this now confirms testing does ensure no missing codes. Minor limit format change for tests with LSB. Update document formatting	Sep. 15, 2011
K	Removed obsolete part number	Nov. 7, 2011
L	Add application note to prevent oscillation	Jan. 18, 2015
M	Corrected Subgroup 8,9,10,11 to 2,3,4,5,6 (TCVOS, TCA, TCBPO, TCVRO,SINAD, THD, PS, Σ2nd and Σ 3RD). Add Fs symbol for Sample Rate.	Oct. 06, 2017

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