LTC7103
105V, 2.3A Low EMI Synchronous Step-Down Regulator

DESCRIPTION

Demonstration circuit 2317A is a 100V monolithic DC/DC step-down regulator featuring the LTC®7103. The demo board is designed for a 5V/2.3A output from a 5V to 100V input at 400kHz switching frequency. The wide input range makes it suitable for automotive, industrial, medical instrument, and telecom applications. This buck regulator has a peak efficiency of 93.5% at $12V_{IN}$, 88.3% at $48V_{IN}$ and 81.5% at $100V_{IN}$ (see Figure 3).

The LTC7103 is a compact, high efficiency synchronous monolithic step-down switching regulator with fast current programming. The power switches, compensation network and other necessary circuits are inside of the LTC7103 to minimize external components and simplify design. The LTC7103 has wide operating range from 4.4V to 105V. A 40ns minimum on-time, together with 100% maximum duty cycle allow practical use at any output voltage between 1V and V_{IN}. The switching frequency can be programmed either via an oscillator resistor or an external clock over a 200kHz to 2MHz range. Additional features include a fast and accurate output current programming and monitoring, and ultralow EMI/EMC emissions.

The demo board has an EMI filter installed. The EMI performance of the board (with EMI filter) is shown in Figure 2. The figure shows that the circuit passes the CISPR 25 radiated emission test with a wide margin. To achieve EMI/EMC performance as shown in Figure 2, the input EMI filter is required and the input voltage should be applied at +VIN_EMI turret pin.

The demo board provides current monitor and output clock signal to interface with an external application circuit. User selectable mode selection (JP1) is provided and Burst Mode® operation position is selected by default. Burst Mode operation increases light load efficiency while pulse-skipping mode allows constant-frequency operation to a lighter load. This demo board allows phase-locked loop (PLL) synchronization to an external clock by selecting SYNC mode on JP1 and by providing a clock signal on CLKIN turret.

The LTC7103 data sheet gives a complete description of the part, operation and application information. The data sheet must be read in conjunction with this demo manual for DC2317A. The LTC7103 is assembled in the 36 (26) lead QFN package. Proper board layout is essential for maximum thermal and electrical performance. See the data sheet sections for details.

Design files for this circuit board are available at http://www.linear.com/demo/DC2317A

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Range		5		100	V
V_{OUT}	Output Voltage			5		V
I_{OUT}	Output Current Range, Continuous	Free Air	0		2.3	A
f_{SW}	Switching (Clock) Frequency			400		kHz
V_{OUTP-P}	Output Ripple	V_{IN} = 100V, V_{OUT} = 5V, I_{OUT} = 2.3A (20MHz BW)		50		mV_{P-P}
P_{OUT}/PIN	Efficiency	V_{IN} = 12V, I_{OUT} = 1A V_{IN} = 48V, I_{OUT} = 1A		92.6 88.1		% %
	Approximate Size	Component Area x Top Component Height		1.0 × 0.7 × 0.3		Inches

QUICK START PROCEDURE

Refer to Figure 1 for proper measurement equipment setup and follow the procedure below.

Note: When measuring the output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the output voltage ripple by touching the probe tip and ground ring directly across the last output capacitor as shown in Figure 1.

1. Place SW1 to ON position.
2. With power off, connect the input power supply to +VIN_EMI and GND. If the EMI/EMC performance is not important, the input EMI filter can be bypassed by connecting the input power supply to $+V_{IN}$ and GND.
3. With power off, connect loads from $+V_{OUT}$ to GND.
4. Turn on the power at the input. Make sure that the input voltage does not exceeds 100V.
5. Check for the proper output voltage using a voltmeter. Output voltage should be within 5.0V ± 0.1V.

   Note: If there is no output, temporarily disconnect the load to make sure that the load is not set too high.
6. Once the proper output voltage is established, adjust the load within the operating ranges and observe the output voltage regulation, ripple voltage, efficiency and other parameters.
7. An external clock can be added to the CLKIN terminal when SYNC mode is used (JP1 on the SYNC position). See the data sheet Frequency Selection and Phase-Locked Loop section for details.

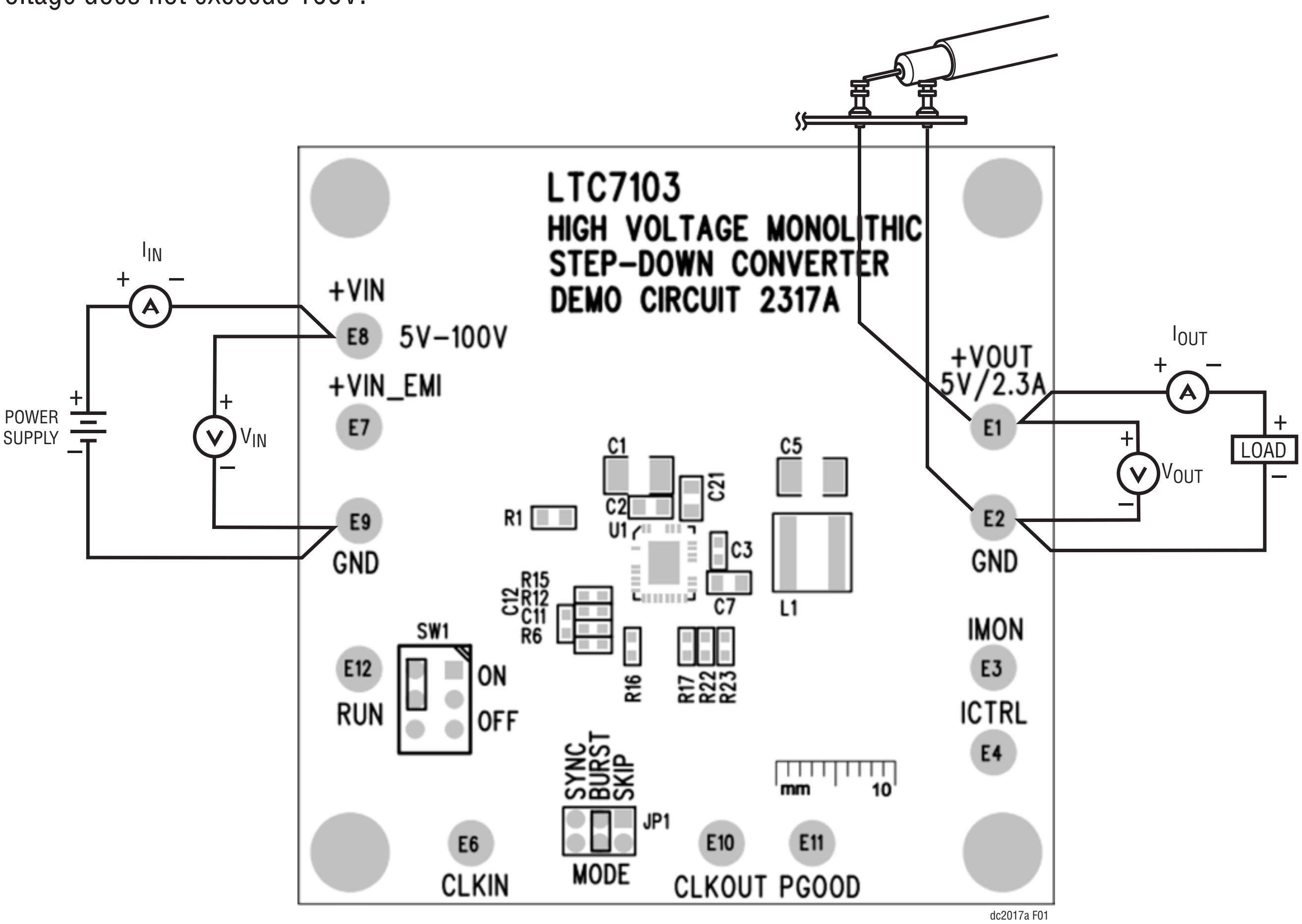
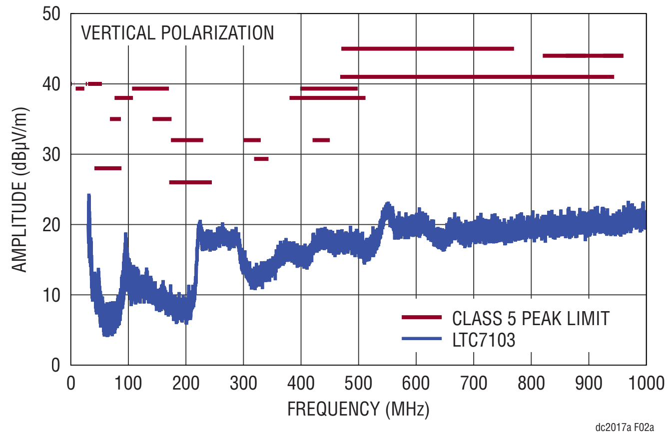


Figure 1. Proper Measurement Equipment Setup

QUICK START PROCEDURE



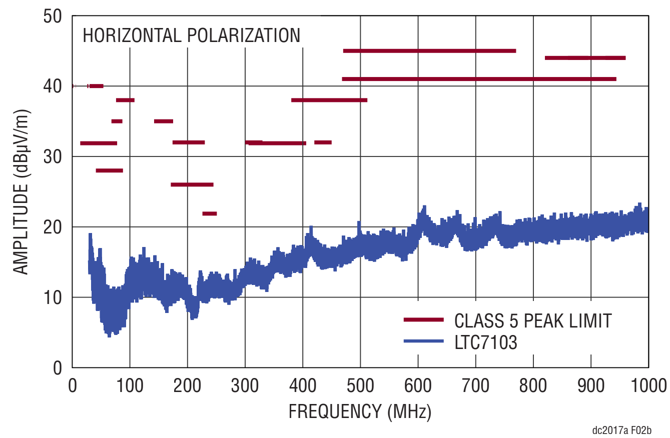
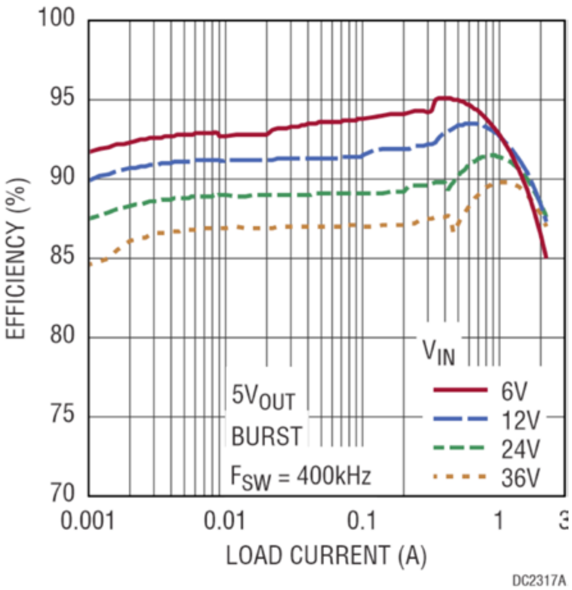


Figure 2. EMI Performance in CISPR 25 Radiated Emission Test (48V_{IN} from +VIN_EMI Turret Pin, 5V_{OUT}/2A, f_{SW} = 400kHz)

QUICK START PROCEDURE



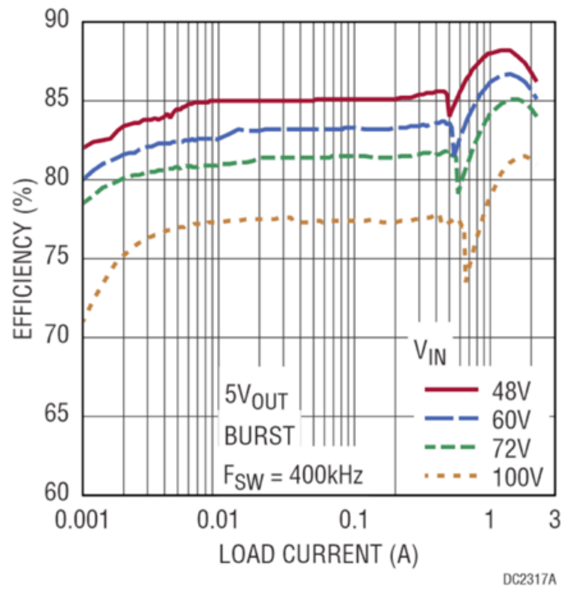
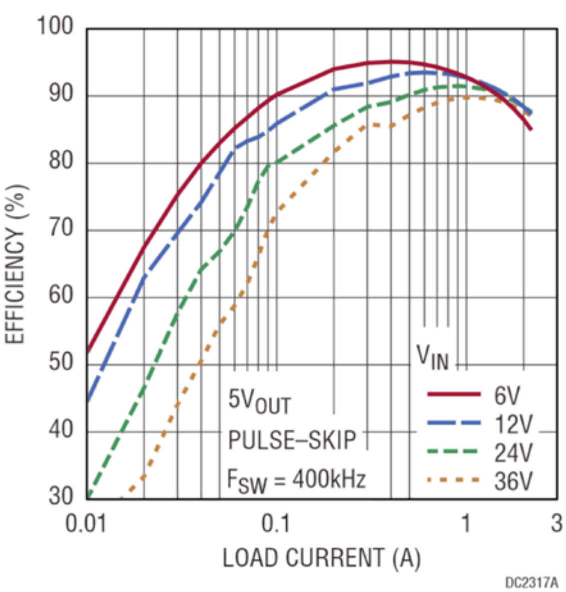


Figure 3. Efficiency at Various Input Voltages (Conditions: Burst Mode Operation)



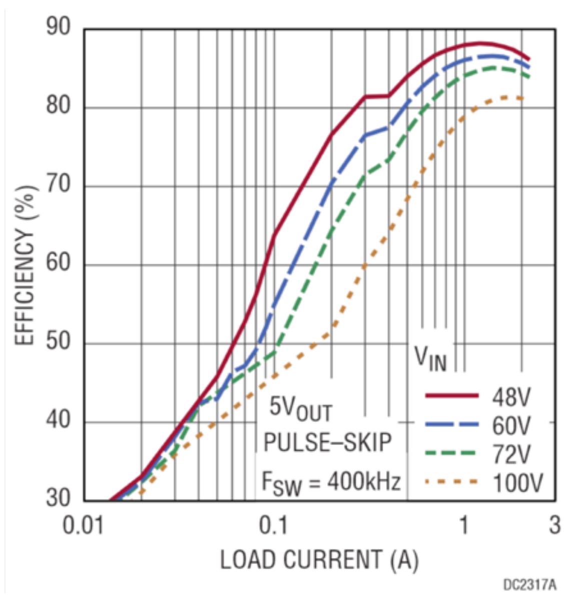


Figure 4. Efficiency at Various Input Voltages (Conditions: Pulse-Skipping Mode)

QUICK START PROCEDURE

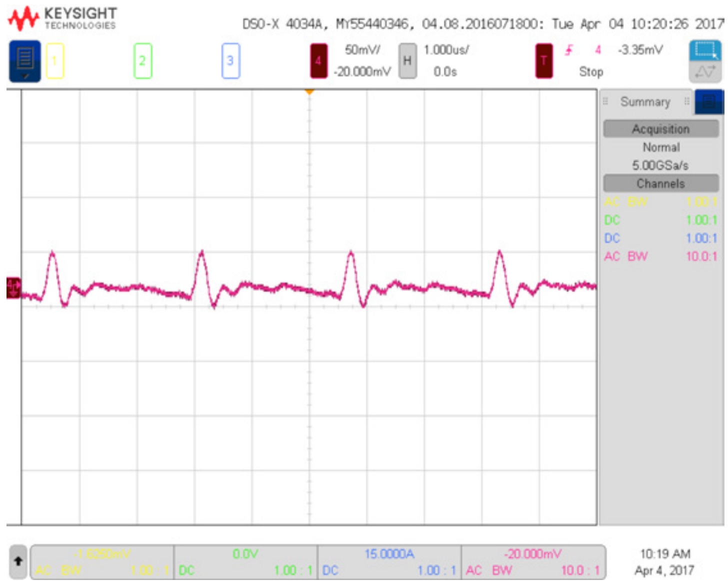


Figure 5. Output Ripple at $100V_{IN}$, $5V_{OUT}$ and $2.3A_{OUT}$ (50mV, 500ns/DIV, 20MHz Bandwidth)

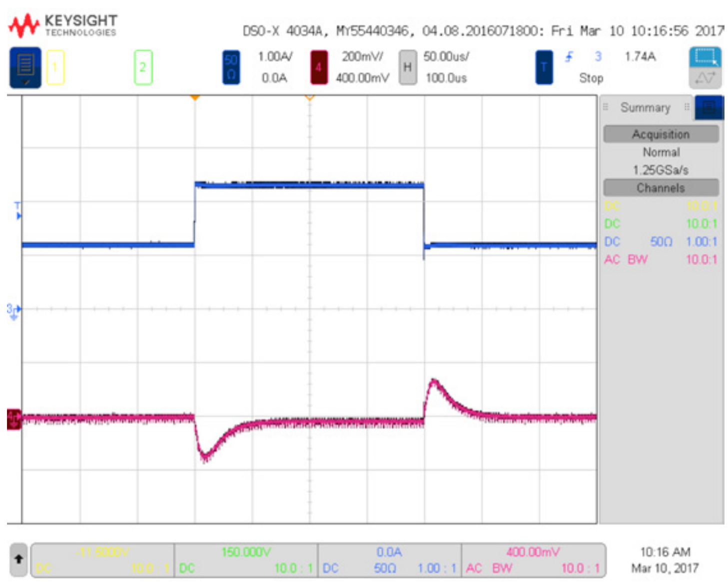
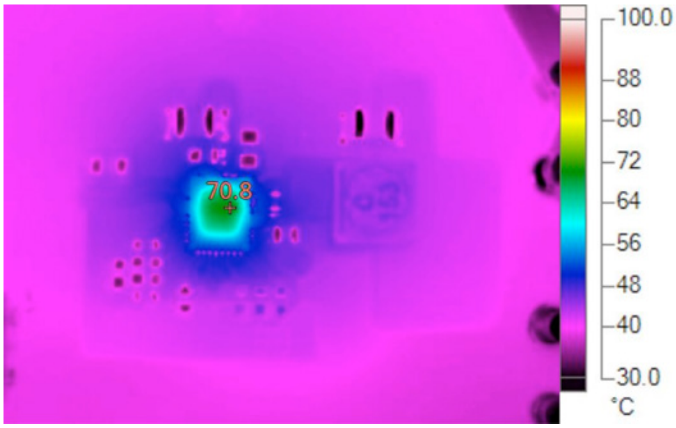
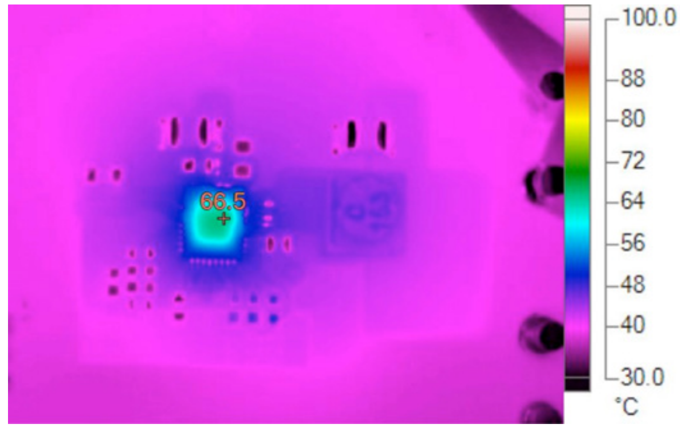


Figure 6. Transient Response Waveform at $48V_{IN}$, $5V_{OUT}$ and $1.1A_{OUT}$ to $2.3A_{OUT}$ to $1.1A_{OUT}$ (1A, 200mV, 50µs/DIV, 20MHz Bandwidth)

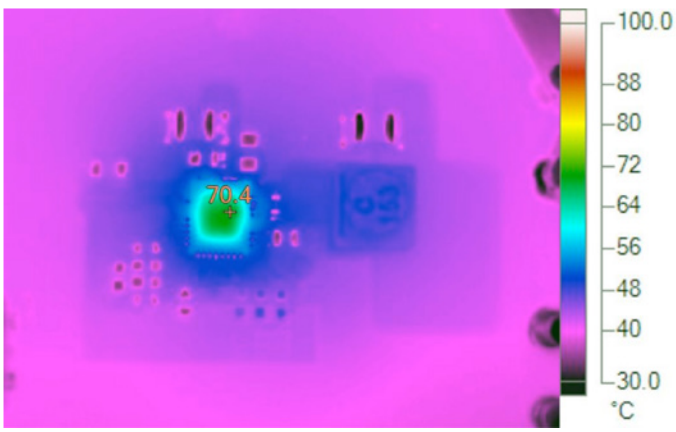
QUICK START PROCEDURE



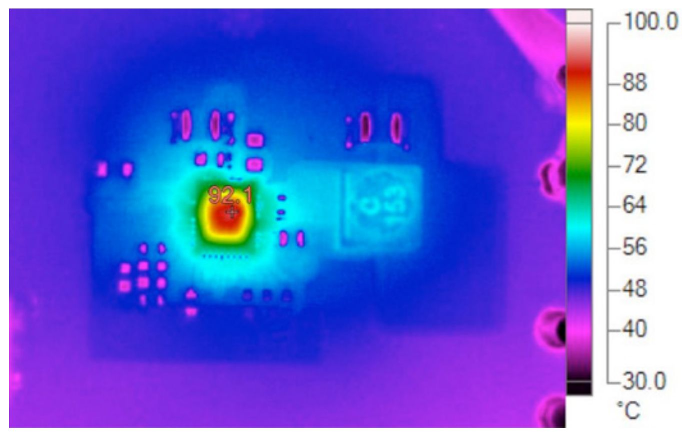
Conditions: 12V_{IN}, 5V_{OUT} at 2.3A_{OUT}



Conditions: 24V_{IN}, 5V_{OUT} at 2.3A_{OUT}



Conditions: 48V_{IN}, 5V_{OUT} at 2.3A_{OUT}



Conditions: 100V_{IN}, 5V_{OUT} at 2.3A_{OUT}

Figure 7. Thermal Plots (without Forced Air)

QUICK START PROCEDURE

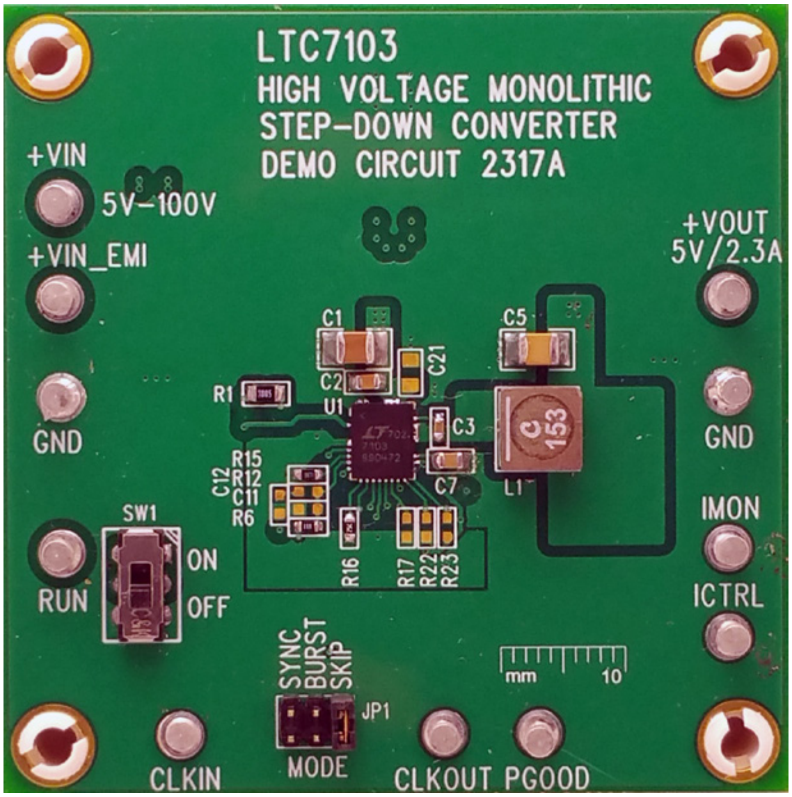
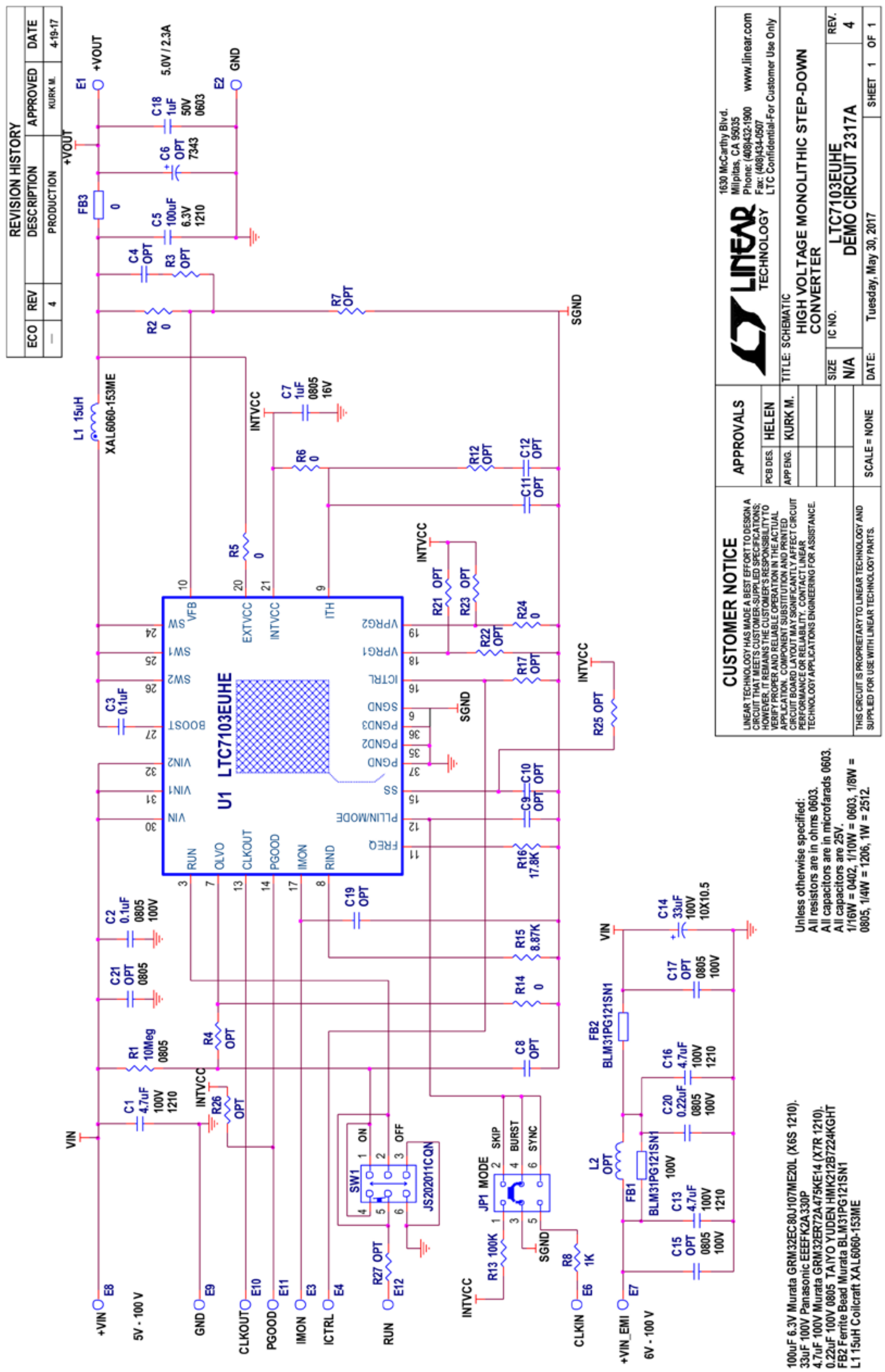


Figure 8. Board Photo

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	3	C1, C13, C16	CAP, X7R 4.7µF, 100V, 10% 1210	MURATA, GRM32ER72A475KE14
2	1	C2	CAP, X7R, 0.1µF, 100V, 10%, 0805	MURATA, GCM21BR72A104KA37L
3	1	C3	CAP, X7R, 0.1µF, 25V, 10%, 0603	MURATA, GRM188R71E104KA01D
4	1	C5	CAP, X6S, 100µF, 6.3V, 20%, 1210	MURATA, GRM32EC80J107ME20L
5	1	C7	CAP, X7R, 1µF, 16V, 10%, 0805	AVX, 0805YC105KAT2A
6	1	C14	CAP, 33µF, 100V, 200mA	PANASONIC, EEEFK2A330P
7	1	C18	CAP, X7R, 1µF, 50V, 10%, 0603	YAGEO.,CC0603KRX7R9BB105
8	1	C20	CAP, X7R, 0.22µF, 100V, 10%, 0805	TAIYO YUDEN,HMK212B7224KGHT
9	1	L1	IND, 15µH	COILCRAFT, XAL6060-153ME
9	0	L1 (ALTERNATE)	IND, 15µH	WURTH, 74439346150
10	1	R1	RES, 10MEG, 1%, 0805	VISHAY, CRCW080510M0FKEA
11	5	R2, R5, R6, R14, R24	RES, 0Ω, JUMPER 0603	VISHAY, CRCW06030000Z0EA
12	1	R8	RES, 1k, 1%, 0603	VISHAY, CRCW06031K00FKEA
13	1	R13	RES, 100k, 1%, 0603	VISHAY, CRCW0603100KFKEA
14	1	R15	RES, 8.87k, 1%, 0603	VISHAY, CRCW06038K87FKEA
15	1	R16	RES, 17.8k, 1%, 0603	NIC, NRC06F1782TRF
16	1	U1	LTC7103EUHE32, QFN 5mm × 6mm	ANALOG DEVICES LTC7103EUHE#PBF
Additional Demo Board Circuit Components				
18	0	C4, C6, C8–C12, C15, C17, C19, C21	CAP, OPTIONAL	OPTIONAL
19	0	L2	IND, OPTIONAL	OPTIONAL
20	0	R3, R4, R7, R12, R17, R21–R23, R25–R27	RES, OPTIONAL	OPTIONAL
Hardware for Demo Board Only				
22	11	E1–E4, E6–E12	TESTPOINT, TURRET 0.095"	MILLMAX, 2501-2-00-80-00-00-07-0
23	2	FB1, FB2	FERRITE BEAD, 120Ω AT 100MHz, 1206	MURATA., BLM31PG121SN1
24	1	FB3	RES, 0Ω, SHUNT,1206	VISHAY, CRCW12060000Z0EA
25	1	JP1	HEADER, 3-PIN DBL ROW 2mm	SULLINS CONNECTOR, NRPN032PAEN-RC
26	1	XJP1	SHUNT	SAMTEC, 2SN-BK-G
27	1	SW1	SWITCHE, SUB MINIATURE SLIDE SWITCHE	C&K.,JS202011CQN
28	4	(STAND-OFFS)	STAND-OFF, NYLON 0.5" TALL	KEYSTONE, 8833 (SNAP ON)
29	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 2317A
30	2		STENCILS TOP AND BOTTOM	STENCIL DC2317A

SCHEMATIC DIAGRAM



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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