30 A Isolated SiC Gate Driver with Slew Rate Control and SPI

Preliminary Technical Data

ADuM4177

FEATURES

30 A peak short circuit (typ) drive output
20 A peak drive current (typ) in typical application
Output power device resistance < 0.4Ω
1500 V peak and dc working voltage to DIN V VDE 0884-11
Slew rate control via SPI interface
Low propagation delay (140 ns typ)
60 ns Minimum Pulse Width
Bi-polar and Uni-polar secondary side supply capability
VDD1: 4.4 V to 7 V
VDD2-GND2: 12 V to 24 V
GND2-VSS2: 0 V to -5.5 V
Protection Features:
DESAT – SiC drain sense, 7 V (typ) threshold
Programmable internal DESAT blanking time
ASC pin, secondary side driver turn-on control, 8 V (typ) threshold
External Miller Clamp
Soft-shutdown, 1 µs capability, adjustable with external resistor
VDD2-VSS2 OVP and programmable VDD2-VSS2 UVP
GND2-VSS2 OVP and UVP
Isolated Fault differentiation through fault reporting pins
SiC Switch Isolated Temperature Sense
1 kHz PWM, and SPI register read
Temperature sense diode stack
Compatible with NTC using external resistor network
SPI Interface
Non-volatile EEPROM registers for configurability
Fault reporting information
Operating junction temperature range (-40 to 150°C)

APPLICATIONS

Switching power supplies
SiC gate drivers
Industrial inverters
Power Factor Correctors

GENERAL DESCRIPTION

The ADuM4177 is an advanced isolated gate driver that provides 5 kVrms isolation employing Analog Devices, Inc. *i*Coupler® technology. The ADuM4177 provides 8.3 mm creepage in a 28-pin wide body SOIC package. The devices are suitable for applications that require insulation against working voltages of 1060 V rms and 1500 V dc for the lifetime of the device. Combining high speed CMOS and monolithic transformer technology, these isolated gate drivers provide outstanding performance characteristics suitable for driving the demanding needs of high performance Silicon Carbide (SiC) switches. SPI communication allows for user programmable operating modes and fault read back.

The ADuM4177 operates with an input voltage range from 4.4 to 7 V. The output voltages can operate with bipolar gate drive of 12 to 24 V positive and -5.5 to -3.25 V for the negative rail. Multiple programmable undervoltage lockout (UVLO) levels can be obtained through SPI communication with the gate driver. In comparison to gate drivers employing high voltage level translation methodologies, the ADuM4177 offers the benefit of true, galvanic isolation between the input and the output.

The ADuM4177 includes many advanced protection features such as the drain monitoring desaturation detection, an active short circuit (ASC) operation, external temperature sensing, and both over voltage protection (OVP) and undervoltage protection (UVP).

Adjustable slew rate control is available to allow for faster edge transitions and higher efficiency when the system operating point can accommodate it. An external miller clamp allows for strong pull-down to prevent unintended Miller injection induced turn on. The ADuM4177 can operate in a wide range of junction temperatures, from -40 to 150°C.

As a result, the ADuM4177 provides reliable control over the switching characteristics of SiC switch configurations over a wide range of switching voltages.

Rev. PrA **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support **www.analog.com**

TABLE OF CONTENTS

FUNCTIONAL BLOCK DIAGRAM

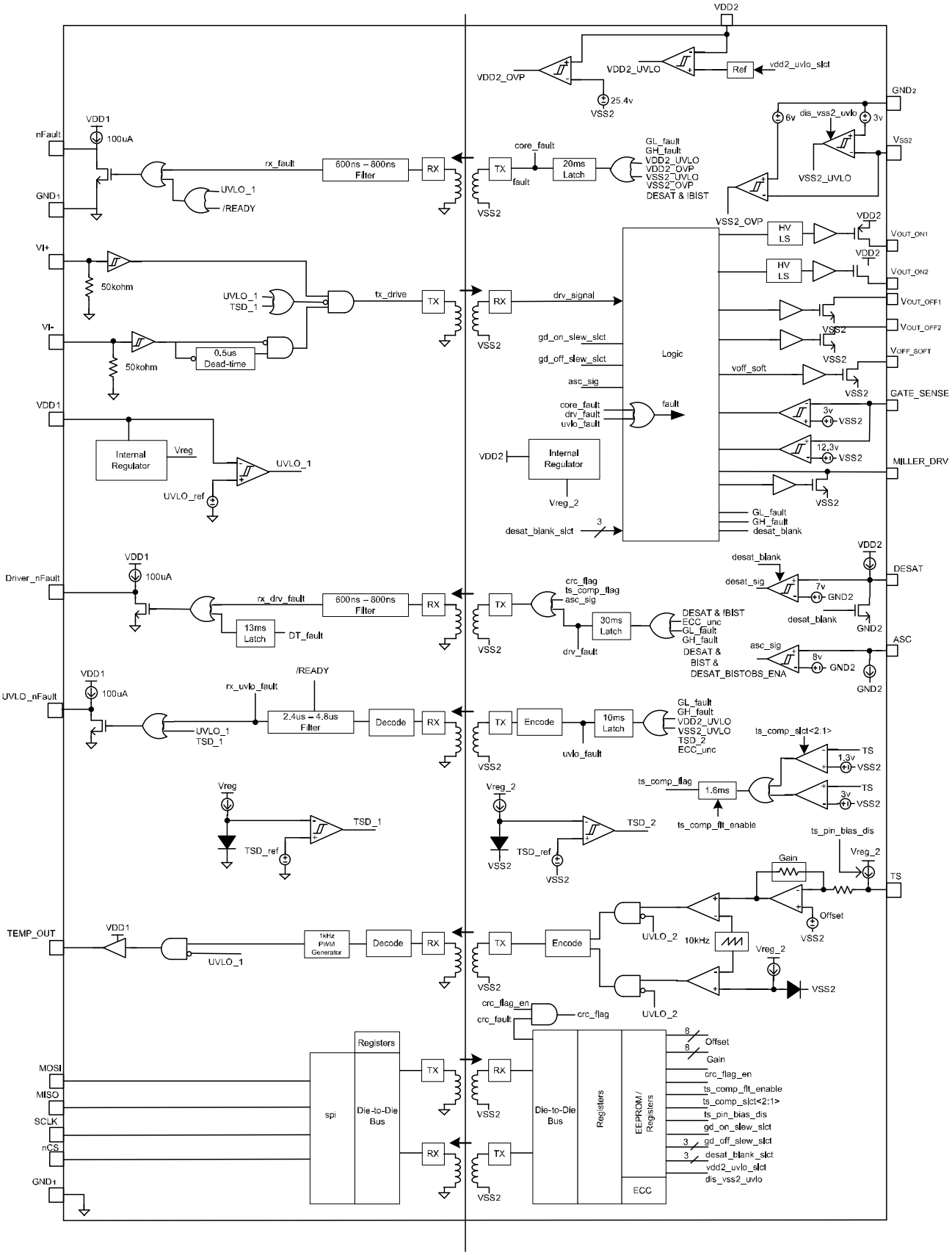

Figure 1.

SPECIFICATIONS

Low-side voltages referenced to GND_1 and high-side voltages referenced to GND_2 unless otherwise noted. V_{DD1} = 4.4 to 7 V, V_{DD2} = 12 to 24 V, V_{SS2} = -5.5 to -3.25 V, T_J = −40°C to +150°C, unless otherwise noted. All minimum and maximum specifications apply over the entire recommended operating junction temperature range, unless otherwise noted. All typical specifications are at T_J = 25°C, V_{DD1} = 5 V, and V_{DD2} = 18 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC Specifications						
Primary Side Power Supply						
V_{DD1} Input Voltage	V_{DD1}	4.4		7	V	
V_{DD1} Input Current, Quiescent	$I_{DD1(Q)}$	TBD	TBD	10	mA	VDD1 = 5 V, VI+ = 0 V, VI+ = 5 V, $\overline{CS}$ = 5 V
V_{DD1} Input Current, SPI active	$I_{DD1(SPI)}$	TBD	TBD	15	mA	VDD1 = 5 V, VI+ = 0 V, VI+ = 5 V, $\overline{CS}$ = 0 V
Secondary Side Power Supply						
V_{DD2} Input Voltage	V_{DD2}	12		24	V	
Input Current, Quiescent for V_{DD2}	$I_{DD2(Q)}$	TBD	15	TBD	mA	V_{DD2} = 25 V, V_{SS2} = -5 V, VI+ = 0 V, $\overline{CS}$ = 5 V
V_{SS2} Input Voltage	$V_{SS2(Q)}$	-5.5		-3.25	V	V_{DD2} = 18 V
UVLO						
Positive Going Threshold						
V_{DD1}	$V_{VDD1UV+}$	TBD	3.8	TBD	V	
V_{SS2}	$V_{VSS2UV+}$	TBD	-3.0	TBD	V	
V_{DD2} (referenced to V_{SS2})	$V_{VDD2UV+0}$	13.76	13.96	14.16	V	VDD2_UVLO_SLCT = '000'
	$V_{VDD2UV+1}$	TBD	15.95	TBD	V	VDD2_UVLO_SLCT = '001'
	$V_{VDD2UV+2}$	TBD	16.93	TBD	V	VDD2_UVLO_SLCT = '010'
	$V_{VDD2UV+3}$	TBD	17.92	TBD	V	VDD2_UVLO_SLCT = '011'
	$V_{VDD2UV+4}$	18.58	18.88	19.18	V	VDD2_UVLO_SLCT = '100'
(default)	$V_{VDD2UV+5}$	TBD	20.87	TBD	V	VDD2_UVLO_SLCT = '101'
	$V_{VDD2UV+6}$	TBD	21.85	TBD	V	VDD2_UVLO_SLCT = '110'
	$V_{VDD2UV+7}$	22.44	22.84	23.14	V	VDD2_UVLO_SLCT = '111'
Negative Going Threshold						
V_{DD1}	$V_{VDD1UV-}$	TBD	3.5	TBD	V	
V_{SS2}	$V_{VSS2UV-}$	TBD	-2.55	TBD	V	
V_{DD2} (referenced to V_{SS2})	$V_{VDD2UV-0}$	13.16	13.36	13.56	V	VDD2_UVLO_SLCT = '000'
	$V_{VDD2UV-1}$	TBD	TBD	TBD	V	VDD2_UVLO_SLCT = '001'
	$V_{VDD2UV-2}$	TBD	TBD	TBD	V	VDD2_UVLO_SLCT = '010'
	$V_{VDD2UV-3}$	TBD	TBD	TBD	V	VDD2_UVLO_SLCT = '011'
	$V_{VDD2UV-4}$	17.76	18.06	18.36	V	VDD2_UVLO_SLCT = '100'
(default)	$V_{VDD2UV-5}$	TBD	TBD	TBD	V	VDD2_UVLO_SLCT = '101'
	$V_{VDD2UV-6}$	TBD	TBD	TBD	V	VDD2_UVLO_SLCT = '110'
	$V_{VDD2UV-7}$	21.41	21.81	22.11	V	VDD2_UVLO_SLCT = '111'
Hysteresis						
V_{DD1}	$V_{VDD1UVH}$		0.3		V	
V_{SS2}	$V_{VSS2UVH}$		0.45		V	
V_{DD2}	$V_{VDD2UVH0}$		0.6		V	VDD2_UVLO_SLCT = '000'
	$V_{VDD2UVH1}$		TBD		V	VDD2_UVLO_SLCT = '001'
	$V_{VDD2UVH2}$		TBD		V	VDD2_UVLO_SLCT = '010'
	$V_{VDD2UVH3}$		TBD		V	VDD2_UVLO_SLCT = '011'
	$V_{VDD2UVH4}$		0.82		V	VDD2_UVLO_SLCT = '100'

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
(default)	$V_{VDD2UVH5}$		TBD		V	VDD2_UVLO_SLCT = '101'
	$V_{VDD2UVH6}$		TBD		V	VDD2_UVLO_SLCT = '110'
	$V_{VDD2UVH7}$		1.03		V	VDD2_UVLO_SLCT = '111'
OVP						
Positive Going Threshold						
V_{DD2}	$V_{VDD2OV+}$	TBD	25.4	TBD	V	Referenced to V_{SS2}.
V_{SS2}	$V_{VSS2OV+}$	TBD	-6.0	TBD	V	Referenced to GND_2.
Negative Going Threshold						
V_{DD2}	$V_{VDD2OV-}$	TBD	24.4	TBD	V	Referenced to V_{SS2}.
V_{SS2}	$V_{VSS2OV-}$	TBD	-5.6	TBD	V	Referenced to GND_2.
Hysteresis						
V_{DD2}	$V_{VDD2OVH}$		1		V	Referenced to V_{SS2}.
V_{SS2}	$V_{VSS2OVH}$		0.4		V	Referenced to GND_2.
PWM Logic Inputs (VI+, VI-, SCLK, nCS, MOSI)						
VI+						
Rising Threshold	$V_{VI+\_th\_R}$	2.7	2.5		V	
Falling Threshold	$V_{VI+\_th\_F}$		1.5	1.3	V	
Hysteresis	$V_{VI+\_th\_H}$		1.0			
Internal Pull-down Resistance	R_{VI+}		50		kΩ	
VI-						
Rising Threshold	$V_{VI-\_th\_R}$	2.7	2.5		V	
Falling Threshold	$V_{VI-\_th\_F}$		1.5	1.3	V	
Hysteresis	$V_{VI-\_th\_H}$		1.0			
Internal Pull-down Resistance	R_{VI-}		50		kΩ	
SCLK						
Rising Threshold	$V_{SCLK\_th\_R}$	2.7	2.5		V	
Falling Threshold	$V_{SCLK\_th\_F}$		1.5	1.3	V	
Hysteresis	$V_{SCLK\_th\_H}$		1.0			
nCS						
Rising Threshold	$V_{nCS\_th\_R}$	2.7	2.5		V	
Falling Threshold	$V_{nCS\_th\_F}$		1.5	1.3	V	
Hysteresis	$V_{nCS\_th\_H}$		1.0			
MOSI						
Rising Threshold	$V_{MOSI\_th\_R}$	2.7	2.5		V	
Falling Threshold	$V_{MOSI\_th\_F}$		1.5	1.3	V	
Hysteresis	$V_{MOSI\_th\_H}$		1.0			
Thermal Shutdown (TSD)						
Primary Side TSD						
Positive Edge	TSD_{POS1}	155			°C	
Negative Edge	TSD_{NEG1}	135			°C	
Secondary Side TSD						
Positive Edge	TSD_{POS2}	155			°C	
Negative Edge	TSD_{NEG2}	135			°C	
Isolated Temperature Sense						
Temperature Sense						
TS Pin Bias Current	I_{TS}	TBD	0.2	TBD	mA	
Operating Frequency	TS_{PWM}	TBD	10	TBD	kHz	
Sense Filter Time	t_{FILT}		TBD		ms	
Maximum TS Pin Voltage	TS_{MAX}			5	V	
TS Comparator Thresholds						
Positive Going Threshold						
Comparator 1	$TS_{COMP\_1\_R}$	1.32	1.38	1.44	V	TS_COMP_SLCT<2:1> = '01'
Comparator 2	$TS_{COMP\_2\_R}$	2.97	3.00	3.03	V	TS_COMP_SLCT<2:1> = '10'

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Negative Going Threshold						
Comparator 1	$TS_{COMP\_1\_F}$	1.26	1.32	1.38	V	TS_COMP_SLCT<2:1> = '01'
Comparator 2	$TS_{COMP\_2\_F}$	2.91	2.94	2.97	V	TS_COMP_SLCT<2:1> = '10'
Hysteresis						
Comparator 1	$TS_{COMP\_1\_H}$		0.06		V	TS_COMP_SLCT<2:1> = '01'
Comparator 2	$TS_{COMP\_2\_H}$		0.06		V	TS_COMP_SLCT<2:1> = '10'
Filter Time	TS_{COMP_FILT}		1.64		ms	TS_COMP_FILT_EN = '10'
TEMP_OUT						
TEMP_OUT Duty Cycle	TO_D		12		%	TS – V_{SS2} = 3.7 V
			88		%	TS – V_{SS2} = 1.3 V
TEMP_OUT Maximum Duty Cycle	TO_{DUTY_MAX}		98		%	
TEMP_OUT Minimum Duty Cycle	TO_{DUTY_MIN}		2.5		%	
TEMP_OUT PMOS R_{DSON}	$R_{DSON\_TO\_P}$		60	TBD	Ω	
TEMP_OUT NMOS R_{DSON}	$R_{DSON\_TO\_N}$		10	TBD	Ω	
PWM Output Frequency	F_{PWM}	TBD	1	TBD	kHz	
Switching Specifications						
Turn on/Turn off R_{DSON}						
V_{OUT_ON1} R_{DSON}	R_{DSON_ON1}		TBD	0.8	Ω	GD_ON_SLEW_SLCT = '0'
V_{OUT_ON2} R_{DSON}	R_{DSON_ON2}		TBD	0.8	Ω	GD_ON_SLEW_SLCT = '0'
V_{OUT_OFF1} R_{DSON}	R_{DSON_OFF1}		TBD	0.8	Ω	GD_ON_SLEW_SLCT = '0'
V_{OUT_OFF2} R_{DSON}	R_{DSON_OFF2}		TBD	0.8	Ω	GD_ON_SLEW_SLCT = '0'
V_{OFF_SOFT} R_{DSON}	R_{DSON_SOFT}		TBD	0.6	Ω	
Miller Clamp						
MILLER_DRV Rdson	R_{DSON_M1}		TBD		Ω	Tested at TBD mA
MILLER_DRVPull-up Current	I_{MC_PU}		10		µA	
Miller Gate Sense Threshold	V_{thM}	TBD	3	TBD	V	Referenced to V_{SS2}
Miller Gate Sense Hysteresis	V_{th_hyst}		0.5		V	Referenced to V_{SS2}
Propagation Delay	t_{PROP}		140	TBD	ns	No gate load
Gate High Sense Threshold	GH_{th}	TBD	12.3	TBD	V	Referenced to V_{SS2}
Gate High Sense Hysteresis	GH_{th_hyst}		TBD		V	Referenced to V_{SS2}
Gate High Error Filter	T_{GH_FILT}	TBD	3.2	TBD	µs	
Gate Low Error Filter	T_{GL_FILT}	TBD	3.2	TBD	µs	
Gate Low Sense Threshold	GH_{th}	TBD	TBD	TBD	V	Referenced to V_{SS2}
Gate Low Sense Hysteresis	GH_{th_hyst}		TBD		V	Referenced to V_{SS2}
Internal Deadtime	T_{DT}	TBD	0.5	TBD	µs	
Common-Mode Transient Immunity (CMTI)	|CM|				kV/µs	
Static CMTI[1]		150				V_{CM} = 1500 V
Dynamic CMTI[2]		150				V_{CM} = 1500 V
Desaturation (DESAT) Detection						
DESAT Pin Current	I_{DESAT_PU}		10		µA	
Comparator Thresholds						
Rising Threshold	V_{DESAT_R}	6.4	7.0	7.6	V	
Falling Threshold	V_{DESAT_F}	6.2	6.8	7.4	V	
Hysteresis	V_{DESAT_H}		0.2		V	
Delay to Soft Turn Off	t_{DESAT_DLY}	75	100	140	ns	
Blanking Switch R_{DSON}	R_{DSON_BLANK}	6	10.6	24	Ω	
DESAT Blanking Time						
Code 000	T_{BLANK_000}	TBD	0	TBD	ns	DESAT_BLANK_SLCT = '000'
Code 001 (default)	T_{BLANK_001}	TBD	100	TBD	ns	DESAT_BLANK_SLCT = '001'
Code 010	T_{BLANK_010}	TBD	200	TBD	ns	DESAT_BLANK_SLCT = '010'
Code 011	T_{BLANK_011}	TBD	300	TBD	ns	DESAT_BLANK_SLCT = '011'
Code 100	T_{BLANK_100}	TBD	400	TBD	ns	DESAT_BLANK_SLCT = '100'

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Code 101	T_{BLANK_101}	TBD	500	TBD	ns	DESAT_BLANK_SLCT = '101'
Code 110	T_{BLANK_110}	TBD	600	TBD	ns	DESAT_BLANK_SLCT = '110'
Code 111	T_{BLANK_111}	TBD	700	TBD	ns	DESAT_BLANK_SLCT = '111'
Active Short Circuit (ASC)						
ASC Pin Current	I_{ASC}	100	150	200	µA	V_{ASC} = 8 V
Comparator Thresholds						
Rising Threshold	V_{ASC_R}	7.4	8.0	8.6	V	
Falling Threshold	V_{ASC_F}	7.2	7.8	8.4	V	
Hysteresis	V_{ASC_H}		0.2		V	
ASC Propagation Delay						
Propagation Delay Rising	t_{PD_ASCr}	70	100	130	ns	
Propagation Delay Falling	t_{PD_ASCf}	90	120	175	ns	
Fault Specifications						
Latch Time						
UVLO_nFAULT	$t_{LATCH\_UVLO\_nFAULT}$	TBD	10	TBD	ms	
Deadtime	t_{LATCH_DT}	TBD	13	TBD	ms	
$\overline{FAULT}$	t_{LATCH_nFAULT}	TBD	20	TBD	ms	
DRIVER_nFAULT	$t_{LATCH\_D\_nFAULT}$	TBD	30	TBD	ms	
Reporting Time						
UVLO _nFAULT	$t_{FDEL\_UVLO\_nFAULT}$		TBD	6.7	µs	
Deadtime	t_{FDEL_DT}		TBD		µs	
$\overline{FAULT}$	t_{FDEL_nFAULT}		TBD	1.1	µs	
DRIVER_nFAULT	$t_{FDEL\_D\_nFAULT}$		TBD	1.1	µs	
DRIVER_nFAULT Pull-up Current	$I_{D\_nFAULT\_PU}$		100		µA	
UVLO_nFAULT Pull-up Current	$I_{UVLO\_nFAULT\_PU}$		100		µA	
$\overline{FAULT}$ Pull-up Current	I_{nFAULT_PU}		100		µA	
DRIVER_nFAULT NMOS R_{DSON}	$R_{DSON\_D\_nFAULT}$		10	TBD	Ω	
UVLO_nFAULT NMOS R_{DSON}	$R_{DSON\_UVLO\_nFAULT}$		10	TBD	Ω	
$\overline{FAULT}$ NMOS R_{DSON}	R_{DSON_nFAULT}		10	TBD	Ω	
SPI Interface						
Minimum SCLK Period	t_{CLK}	2.22	2.50		µs	400 kHz (typ), 450 kHz (max)
Minimum SCLK High Time	t_{HI}	0.45			µs	
Minimum SCLK Low Time	t_{LO}	0.775			µs	
Valid Data Before SCLK Falling Edge	t_{DS}	0.125			µs	
Valid Data After SCLK Falling Edge	t_{DH}	0.125			µs	
					µs	
nCS Falling to First SCLK Rising Edge	t_S	2.5			µs	
nCS Rising Edge to nCS falling Edge		5.5			µs	
EEPROM Program Time	t_{PROG}		1		ms	Single Programming Cycle
				40	ms	40 Programming Cycles
Peak Current Per Output Pin[3]	I_{PEAKIP}		10		A	V_{DD2} = 18 V, 1.5 Ω external resistors
Short Circuit Peak Current Per Pin[1]	I_{PEAKIP_SC}		15		A	V_{DD2} = 18 V, 0 Ω external resistors

[1] Static common-mode transient immunity (CMTI) is defined as the largest dv/dt between V_{SS1} and V_{SS2}, with inputs held either high or low, such that the output voltage remains either above 0.8 × V_{DD2} for output high or below 0.8 V for output low. Operation with transients above recommended levels may cause momentary data upsets. Tested in characterization and not production tested.

[2] Dynamic common-mode transient immunity (CMTI) is defined as the largest dv/dt between V_{SS1} and V_{SS2} with the switching edge coincident with the transient test pulse. Operation with transients above recommended levels may cause momentary data upsets. Tested in characterization and not production tested.

[3] Peak current ratings are tested in characterization and not production tested.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 2.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L (I01)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.7	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		0.017	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303 Part 1
Material Group		I		Material group (DIN VDE 0110, 1/89, Table 1)

RECOMMENDED OPERATING CONDITIONS

Table 3.

Parameter	Value
Operating Junction Temperature Range	−40°C to +150°C
Supply Voltages	
V_{DD1} Referenced to GND_1	4.4 V to 7.0 V
V_{DD2} Referenced to GND_2	12 V to 24 V ($V_{DD2} – V_{SS2} < 24$ V)
V_{SS2} Referenced to GND_2	-5.5 V to -3.25 V ($V_{DD2} – V_{SS2} < 24$ V)

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltages	
V_{DD1}[1]	-0.2 V to 7.5 V
V_{DD2}[2]	-0.2 V to 30 V
V_{SS2}[2]	-7 V to 0.2 V
Primary Side Pins	
VI+[1], VI-[1], MOSI[1], SCLK[1], $\overline{CS}$[1]	-0.2 V to 7.5 V when VDD1 > 4.4 V; -0.2 V to 6 V when VDD1 ≤ 4.4 V
$\overline{FAULT}$[1], DRIVER_nFAULT[1], UVLO_nFAULT[1], TEMP_OUT[1], MISO[1]	-0.2 V to V_{DD1} + 0.2 V
Secondary Side Pins	
TS[3]	-0.2 V to 5.2 V
ASC[2], DESAT[2]	-0.2 V to V_{DD2} V
MILLER_DRV[3], V_{OUT_OFF1}[3], V_{OUT_OFF2}[3], V_{OFF_SOFT}[3], GATE_SENSE[3]	-0.2 V to V_{DD2} V
V_{OUT_ON1}[3], V_{OUT_ON2}[3]	-0.2 V to V_{DD2} + 0.2 V

[1] Referenced to GND_1.
[2] Referenced to GND_2.
[3] Referenced to V_{SS2}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} is the junction to ambient thermal resistance, and Ψ_{JT} is the junction to top characterization parameter.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
RN-28-1	TBD	TBD	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

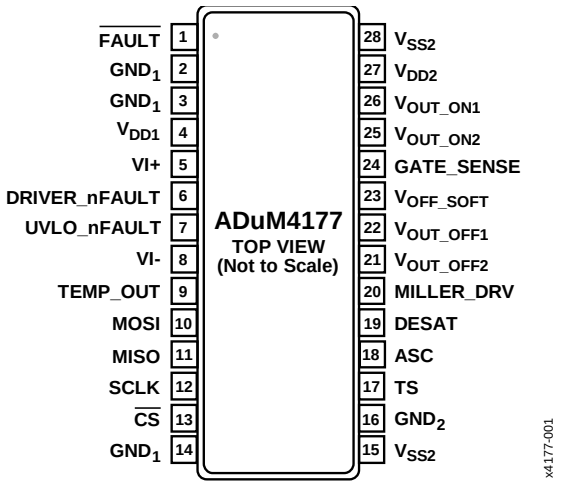

Figure 2.

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{FAULT}}$	Negative logic fault output pin. Negative logic pin that communicates fault state of the gate driver.
2	GND_1	Primary side ground connection. Ground reference for primary side signals.
3	GND_1	Primary side ground connection. Ground reference for primary side signals.
4	V_{DD1}	Primary side power supply input. Provides current to operate the primary side of the gate driver.
5	VI+	Non-inverting input. Connect to non-inverting input of the control signal.
6	DRIVER_nFAULT	Negative logic driver fault pin. Responds to driver related faults.
7	UVLO_nFAULT	Negative logic UVLO fault pin. Responds to UVLO related faults.
8	VI-	Inverting input. Connect to inverted input of control signal.
9	TEMP_OUT	Temperature sense PWM output pin. Returns the PWM encoded temperature sense signal from secondary side.
10	MOSI	SPI master out slave in pin. Data connection pin for SPI communication.
11	MISO	SPI master in slave out pin. Data connection pin for SPI communication.
12	SCLK	SPI reference clock. Clock pin for SPI communication.
13	$\overline{\text{CS}}$	SPI chip select pin. Negative logic chip select pin for SPI communication.
14	GND_1	Primary side ground connection. Ground reference for primary side signals.
15	V_{SS2}	Secondary side negative supply connection. Lowest potential voltage on secondary side of gate driver.
16	GND_2	Secondary side ground connection. Ground reference for secondary side signals.
17	TS	Temperature sense pin. Accepts an analog signal to convert into a PWM signal read out of TEMP_OUT pin.
18	ASC	Active Short Circuit pin. When ASC is brought high, the output of the gate driver goes high.
19	DESAT	Switch Drain protection sense input. Provides desaturation detection of the power device.
20	MILLER_DRV	Open drain miller drive pin. Connect to external Miller clamp to provide strong pull-down of power device.
21	V_{OUT_OFF2}	Gate drive turn off pin 2. Provides strong turn off of power device. Can be toggled with slew rate control by SPI settings.
22	V_{OUT_OFF1}	Gate drive turn off pin 1. Provides strong turn off of power device.
23	V_{OFF_SOFT}	Soft shutdown pin. Provides shut off path for gate during fault conditions requiring a soft shutdown.
24	GATE_SENSE	Switch gate sense pin. Connect directly to power device gate.
25	V_{OUT_ON2}	Gate drive turn on pin 2. Provides strong turn on of power device. Can be toggled with slew rate control by SPI settings.
26	V_{OUT_ON1}	Gate drive turn on pin 1. Provides strong turn off of power device.
27	V_{DD2}	Secondary side positive power supply input pin. Provides positive voltage rail to gate driver.
28	V_{SS2}	Secondary side negative power supply input pin. Provides negative voltage rail to gate driver.

TYPICAL PERFORMANCE CHARACTERISTICS

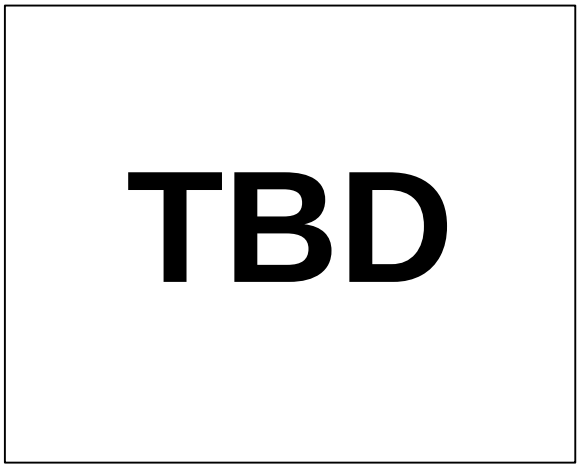

Figure 3

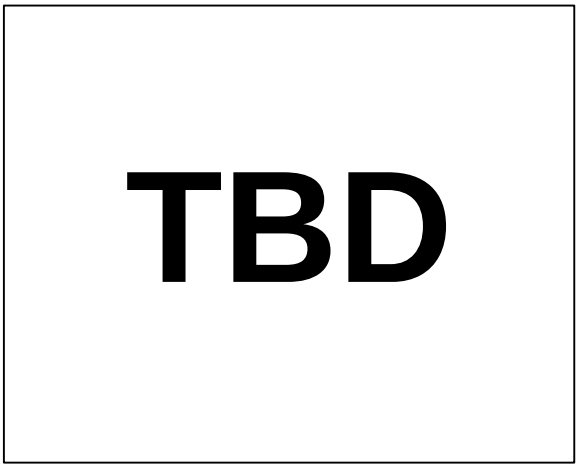

Figure 6

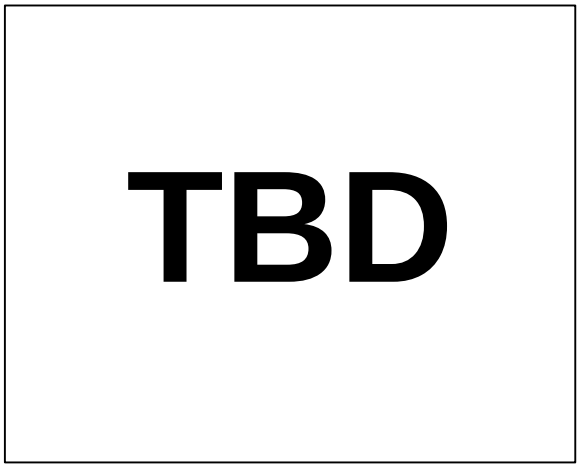

Figure 4

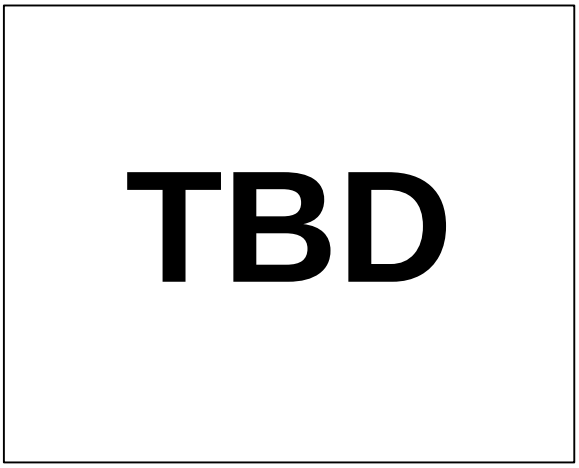

Figure 7

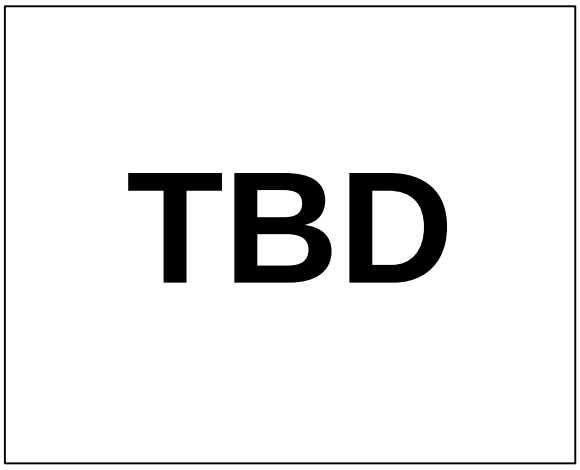

Figure 5

THEORY OF OPERATION

Gate drivers are required in situations where fast rise times of switching device gates are required. The gate signals for enhancement power devices are referenced to a source or emitter node. The gate driver must follow this source or emitter node. As such, isolation is necessary between the controlling signal and the output of the gate driver in topologies where the source or emitter nodes swing, such as a half bridge. Gate switching times are a function of the drive strength of the gate driver. Buffer stages before a complementary metal-oxide semiconductor (CMOS) output reduce the total delay time and increase the final drive strength of the driver.

The ADuM4177 achieves isolation between the control side and the output side of the gate driver using a high frequency carrier that transmits data across the isolation barrier with *i*Coupler® chip scale transformer coils separated by layers of polyimide isolation. The ADuM4177 uses positive logic on/off keying (OOK) encoding, in which a high signal is transmitted by the presence of the carrier frequency across the *i*Coupler chip scale transformer coils. Positive logic encoding ensures that a low signal is seen on the output when the input side of the gate driver is unpowered. A low state is the most common safe state in enhancement mode power devices and can drive in situations where shoot through conditions are present. The architecture of the ADuM4177 is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and differential coil layout. Figure 8 shows the OOK encoding used by the ADuM4177.

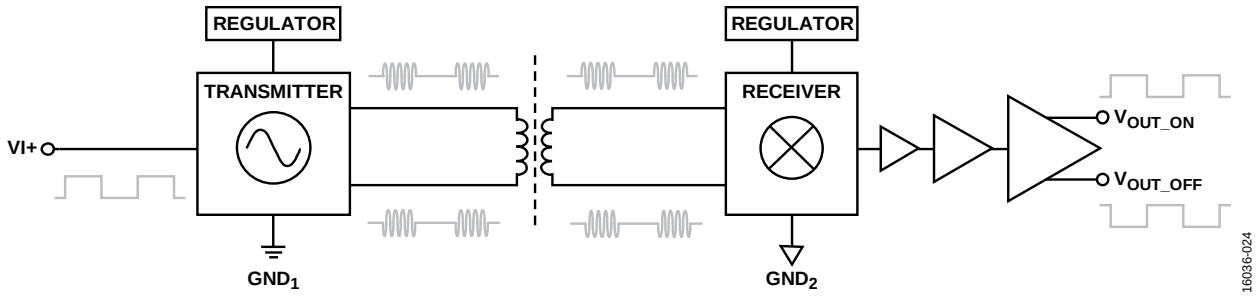

Figure 8. Operational Block Diagram of OOK Encoding

APPLICATIONS

PCB LAYOUT

The ADuM4177 SiC gate driver requires power supply bypassing at the V_{DD1}, V_{DD2} and V_{SS2} supply pins. Use a ceramic capacitor greater than 10 µF on V_{DD1} to GND_1. Add at least 10 µF of capacitance on V_{DD2} to V_{SS2} to provide decoupling to the secondary side circuitry. Separate decoupling capacitors must be placed between V_{DD2} to GND_2 and from GND_2 to V_{SS2}. These capacitors supply the energy to drive the power device gate on and off, and should be at least 10 µF each. Large gate charge power devices may need more capacitance. This capacitance can be provided by multiple parallel capacitors. Avoid using vias on the bypass capacitor or employ multiple vias to reduce the inductance in the bypassing because board vias can introduce parasitic inductance. The total lead length between both ends of the smaller capacitor and the input or output power supply pin should not exceed approximately 5 mm.

To improve robustness against bulk current injection, the input pins (VI+, VI−, MOSI, $\overline{CS}$, and SCLK) can have series 100 Ω resistors placed to limit current. The inclusion of 100 Ω resistors in series with input lines is highly recommended.

POWER SUPPLIES

V_{DD1} Supply

V_{DD1} can be operated between 4.4 V (min) to 7 V (max). The V_{DD1} power supply powers the primary side circuitry. A UVLO is included to prevent underpowered operation. The ADuM4177 will begin to operate once the V_{DD1} voltage exceeds the rising UVLO threshold, 3.8 V (typ), and will continue to operate until the V_{DD1} voltage falls below the falling UVLO threshold, 3.5 V (typ). The ramp rate on the V_{DD1} pin must be kept below 1 V/ms to avoid stress on the primary side silicon. Both startup and operation have this dv/dt rate limitation.

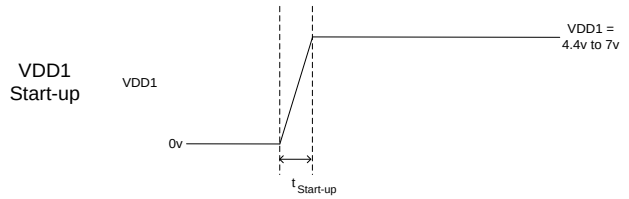

Figure 9. Start-up dv/dt.

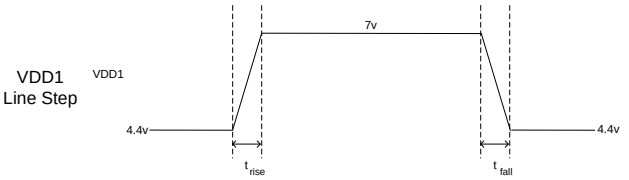

Figure 10. Line-step dv/dt.

V_{DD2}/V_{SS2} Supplies

The ADuM4177 allows for native bipolar output to drive power devices both positively and negatively with respect to their source/emitter node. The secondary side of the ADuM4177 is powered through the V_{DD2}, GND_2, and V_{SS2} pins. The operating range of V_{DD2} to GND_2 is 12 V (min) to 24 V (max). The maximum voltage between V_{DD2} and V_{SS2} is 24 V (max), meaning that if a negative voltage drive is used, the V_{DD2} to GND_2 voltage must be below 24 V. A negative drive can be obtained by supplying a -5.5 V (min) to -3.25 V (max) voltage between V_{SS2} and GND_2.

The ADuM4177 provides secondary side UVLO and OVP protections on both the V_{DD2} and V_{SS2} pins, ensuring that the gate drive is within tight tolerances. The V_{DD2} UVLO and OVP is referenced to V_{SS2}, ensuring a specific total gate voltage swing. The V_{SS2} UVLO and OVP is referenced to GND_2.

The UVLO is programmable through the SPI interface register 0x54 bits <2:0>, VDD2_UVLO_SLCT. The values in register 0x54 are EEPROM programmable, resulting in UVLO options that persist between power cycles.

If the registers of the ADuM4177 are programmed to work in bipolar mode, a negative voltage with the UVLO/OVP range of V_{SS2} is required. In order to operate in unipolar mode (GND_2 = V_{SS2}), VSS2_UVLO_DIS, register 0x52 bits <7:0> must be programmed to '01101101'. This is the only bit configuration that will disable the V_{SS2} UVLO.

Voltage supply excursions outside of the VDD2 and VSS2 UVLO and OVP will issue a fault, shut off the driver output, and enter soft-shutdown. The faults will latch for the prescribed timings, allowing for fault differentiation at the pin reporting level on the primary side.

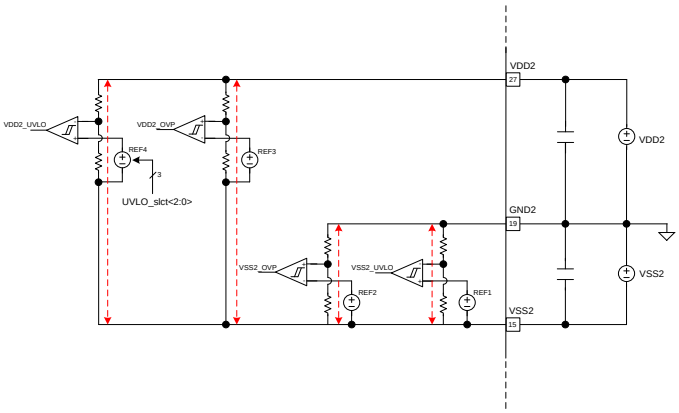

Figure 11. Functional VDD2/VSS2 supply UVLO and OVP

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay describes the time it takes a logic signal to propagate through a component. The propagation delay to a low

output can differ from the propagation delay to a high output. The ADuM4177 specifies the rising propagation delay, t_{DLH} (see Figure 12), as the time between the rising input high logic threshold, V_{IH}, to the output rising 10% threshold. Likewise, the falling propagation delay, t_{DHL}, is defined as the time between the input falling logic low threshold, V_{IL}, and the output falling 90% threshold. The rise and fall times are dependent on the loading conditions and are not included in the propagation delay, which is the industry standard for gate drivers.

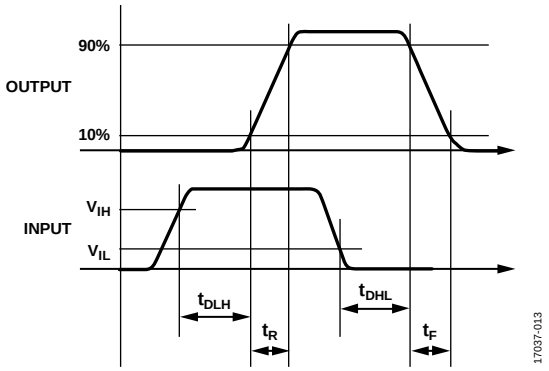

Figure 12. Propagation Delay Parameters

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM4177 components operating under the same temperature, input voltage, and load conditions.

SPI INTERFACE

The SPI interface, consisting of the MOSI, MISO, SCLK and nCS pins, is an independent interface that is active when both the primary side UVLO1 and secondary side V_{DD2}-V_{SS2} voltage is greater than 11.5 V (typ). See Figure 15 for a functional block diagram of the SPI interface. The format for an SPI bit sequence write/read is shown in Figure 13. 24 bits defines a full SPI bit sequence:

Command Field	Address Field	Data Field	CRC Field
<23>	<22:16>	<15:8>	<7:0>
READ(=0)/WRITE(=1)	ADDR<6:0>	Data<7:0>	CRC<7:0>

Figure 13. SPI Register Format (except PWM registers)

Registers 0x08 and 0x09 for the PWM duty cycle information follow a different format for the read back, see Figure 14:

MISO Read		
Data Field	Data Field	CRC Field
<23:20>	<19:8>	<7:0>
0000	Data<11:0>	CRC<7:0>

Figure 14. Register 0x08, 0x09 PWM Format

The PWM register format allows a larger data field to properly send the duty cycle information in a single read step.

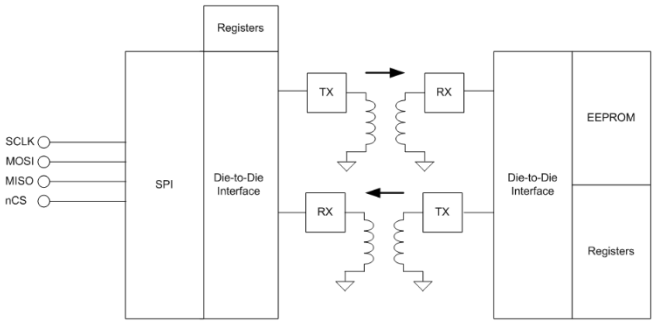

Figure 15. SPI Functional Block Diagram

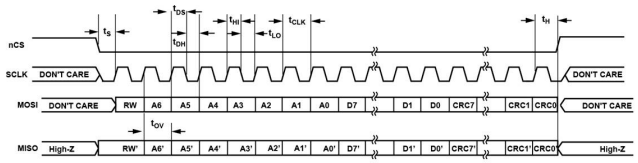

Figure 16. SPI Timing Diagram

CRC is used to ensure proper integrity of a read/write operation. In addition to CRC, ECC is used on both primary side fuse trim and the secondary side EEPROM bits. An ECC_CORR fault occurs if the ECC successfully corrected a single bit error in the secondary side EEPROM. If an ECC_CORR fault occurs, the ADuM4177 will operate normally, but there is a defect present in the part. An uncorrected error will post and shut down operation of the device. On the primary side, an ECC error will only post to the IC Digital Status register, no action is taken to affect operation of the ADuM4177.

A Communication Fault occurs during an SPI write or read operation. A Communication Fault will be posted if either not enough bits were sent during an SPI transfer, or if too many bits were sent during an SPI transfer. In either case, in the event of Communication Fault, the SPI transfer is aborted. A communication fault is posted to the IC1 Digital Status register and the IC3 Digital Status register. A communication fault does not affect normal operation of the ADuM4177.

CRC

The ADuM4177 SPI word is constructed with a CRC field, see Figure 41. The 8 bit CRC word, CRC<7:0>, is set to a specific value which is associated with value of the remaining 16 bits; Data<7:0>, ADDR<6:0> and the READ/WRITE bit.

If the user is performing a write command, the correct CRC<7:0> value must be calculated for the corresponding remaining 16 bits. When performing the write, all data must be transferred to the ADuM4177 device. Internally, the ADuM4177 will take the CRC<7:0> value field and compare it to the remaining 16 bits. If the values correspond correctly, no error is reported. If the values do not correlate, then a CRC_error fault will be issued.

The CRC value is based on the PMBus CRC-8 packet check, which utilizes the polynomial $x^8 + x^2 + x + 1$. Example Verilog code is as follows:

```
Example code in Verilog (data[15] = command, data[14:8] =
address, data[7:0] = value):
// CRC-8
function [7:0] crc8;
input [15:0] data;
integer i;
begin
  crc8 = 0;
  for(i=15;i>=0;i=i-1)
        if ( crc8[7] ^ data[i] )
          crc8 = ( crc8 << 1 ) ^ 8'b00000111;
        else
          crc8 = ( crc8 << 1 );
end
endfunction
```

When writing data to the ADuM4177, the above algorithm should be used to calculate the CRC bit field. Similarly, when performing a read, the above algorithm should be used to confirm the 16 bits of data, address and command against the CRC field read.

Simulating and Programming EEPROM

To simulate trim, or write to registers but not program the available EEPROM bits, both "simulate" bits, bit 0 and bit 1, must be set to '1', and the "program" bit, bit 2, must be set to '0' in the data field. To program trim, or program any EEPROM registers, both "simulate" bits, and the "program" bit, must be set to '1'. This helps prevent false writes by requiring a specific 3 bit sequence to both simulate and program the register space on the secondary side. To summarize:

Simulate register values	→	bits<2:0> = 011
Program eeprom/register values	→	bits <2:0> = 111

Figure 17 provides a flow diagram for both the simulate and program steps for the ADuM4177 secondary side register space. To determine when the programming step is complete, read the IC3 Control register, address 0x42. When bit<2> changes from a '1' to a '0', the programming cycle has completed. A programming step can take up to 40 ms (max) to complete.

During V_{DD1} start-up, the SPI interface will be inactive until the first rising edge of the nCS pin. After the nCS pin goes high for the first time, the SPI interface will respond when the nCS pin if forced low, providing the V_{DD1} UVLO is valid and the V_{DD2}-V_{SS2} supply is greater than 11.5 V (typ).

If during start-up, V_{DD1} is applied while V_{DD2} is 0 V, or if V_{DD2} is lost during normal operation, the SPI interface will continue to operate. The registers located on the primary side can be written to and read from. However, if any register on the secondary side it written to, no value will be accepted without power present on V_{DD2}. If any registers are read on the secondary side, MISO will return all 0's if power is not present on V_{DD2}. With power not present on V_{DD2}, the SPI return receiver will have no signal present, which will return only 0's.

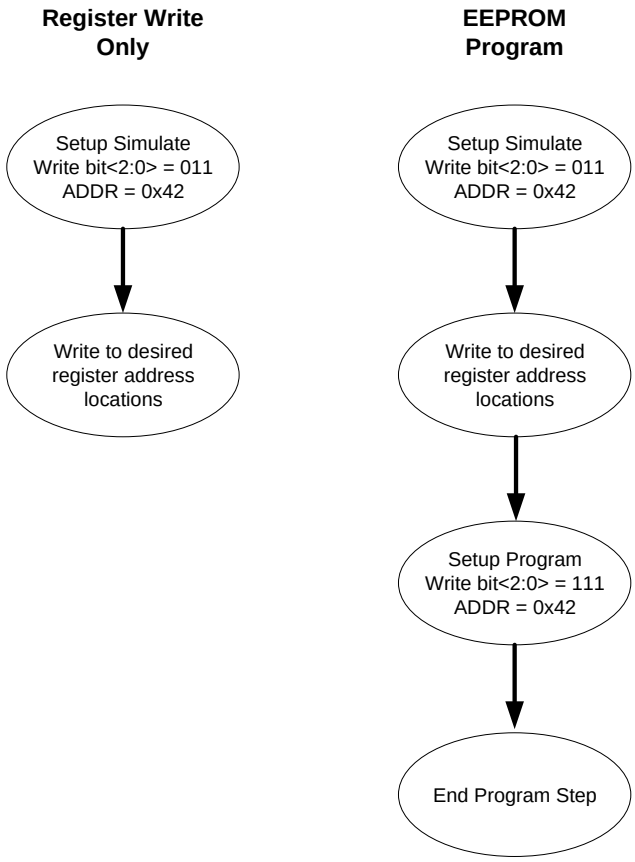

Figure 17. Simulate and Program Flow Diagram

Programming Error Fault

Some faults are written to fault registers for readback. One fault accessible by register read is the "Programming Failed" fault. Figure 18 provides a state diagram for the EEPROM programming flow. After '111' is written to bits <2:0> IC3 Control register, address 0x42, the EEPROM program cycle will start. If at the end of the program cycle, the EEPROM write did not complete successfully, the ADuM4177 will repeat the step automatically. The ADuM4177 will continue this for a total of 40 attempts if any preceding attempt was not successful. After 40 programming attempts, if there continue to be errors, the ADuM4177 will abort the programming cycle and issue a '1' to the Programming Failed bit in the IC3 Digital Status Register.

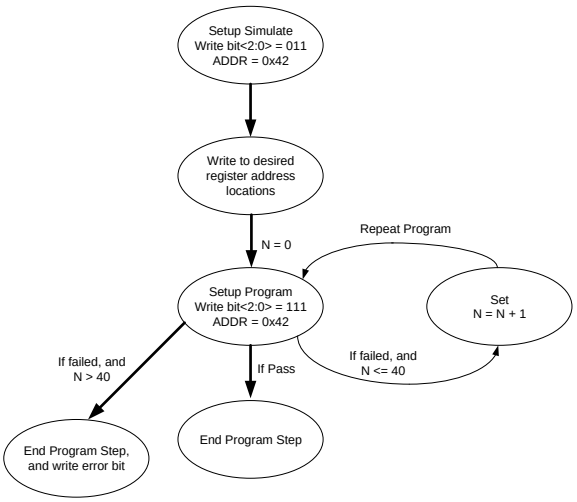

Figure 18. Programming State Diagram

Daisy Chaining ADuM4177

A typical daisy chain configuration for the ADuM4177 is shown in Figure 19. Please note, resistor pull-ups (or pull-downs) should be used on each MOSI pin to avoid high impedance states when the nCS pin is set high, and the MISO pin goes into a Hi-Z output state.

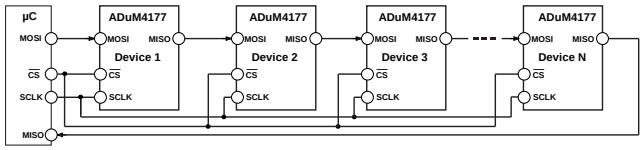

Figure 19. Daisy Chain Diagram

The ADuM4177 is able to be daisy-chained in order to reduce MOSI, MISO, nCS, and SCLK lines interfacing the controller and multiple ADuM4177 units. Please refer to the configuration shown in Figure 20 for the following explanation.

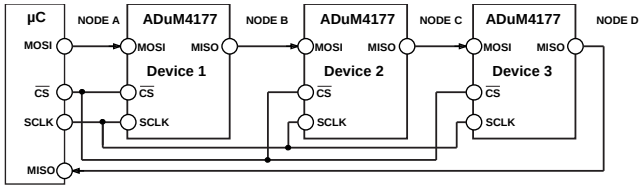

Figure 20. Daisy Chain of Three ADuM4177 Devices

In the configuration shown in Figure 20, three units are shown connected. Each ADuM4177 expects to see some integer multiple of 24 clock cycles per cycle of the nCS pin. If a non-integer number of clock cycles occurs between the falling and rising edges of the nCS pin, the commands are ignored. This is important to note, as the ADuM4177 can be daisy chained with devices that are not ADuM4177 ONLY if the added devices also require an integer number of multiples of 24 cycles.

In this example, because there are three devices daisy chained, each falling and rising edge of nCS will have 24 x 3 cycles on SCLK. This is because three packets of 24 bits needs to be sent. The following is an example transfer, where commands are sent at Node A, and responses are received at Node D.

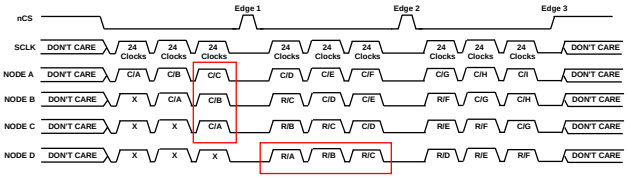

Figure 21. Example SPI transfer of three nCS edges

In Figure 21, there are three separate nCS rising edges. The commands sent are read into each individual ADuM4177 when the rising edge of nCS occurs. "C/" stands for "Command", "R/" stands for response, and "X" stands for unknown. Before the first rising edge, "Edge 1", there are three commands being sent to the devices. The devices repeat the bitstream given to their MOSI pin 24 cycles after. The repeated bitstream appears on the MISO pin. When the rising edge of nCS occurs, the last 24 bits seen on each of the ADuM4177 device's MOSI pin is taken into the device as a command. In this example, command "C" goes to ADuM4177 Device 1, command "B" goes to ADuM4177 Device 2, and command "A" goes to ADuM4177 device "A". During the next falling edge of nCS, the devices are now able to send the responses to the commands, as well as take in the next bitstream of commands. Since ADuM4177 Device 3 is the last in the daisy chain, it is the first to output its response to the controller. This means response "A" is seen on Node "D" first, followed by response "B", and finally response "C".

If a single command is desired to be sent to only one device, a read command can be given to the other devices on the chain. For example, if a "write xxx" command is to be given to ADuM4177 Device 2, then command "B" could be "write xxx", while command "A" and command "C" can be "read xxx". On the rising edge of nCS, the commands will be registered to the devices, and only ADuM4177 Device 2 will have a write command given to it.

There does not need to be an explicit wait time between 24 bit packets. The spaces between the 24 bit packets was drawn for clarity of bit count, and not to show actual timing. It is possible to have a single stream of 72 bits and SCLK periods in this example.

TEMPERATURE SENSE

The ADuM4177 provides the ability to measure internal die temperature of the secondary side die, as well as a remote temperature sense that can be used in conjunction with a diode stack external to the ADuM4177 to measure temperatures outside of the ADuM4177. Remote temperature sensing is performed using the TS pin, and is referred to as TS1 in register names. Internal die temperature of the secondary side ADuM4177 die is reported as TS2 in register names.

External Temperature Sense

The ADuM4177 includes an analog input pin, TS, referenced to the V_{SS2} pin on the secondary side that can report the value of the voltage on TS within a specified range operating at 10 kHz (typ). The reporting occurs on the primary side and is reported both with a 1 kHz (typ) PWM signal on the TEMP_OUT pin, as well as in SPI register 0x08 bits <11:0> PWM_TS1_DUTY.

TEMP_OUT Encoding

The target TEMP_OUT duty cycle vs. TS voltage transfer function follows:

$$TEMP\_OUT(DUTY) = (-31.667) \times V_{TS1} + 129.17$$

Where

TEMP_OUT(DUTY) is the duty cycle of the TEMP_OUT pin.

V_{TS1} is the voltage seen on TS pin.

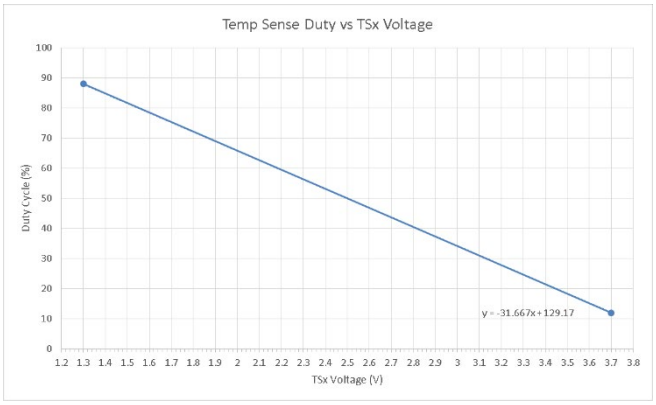

Figure 22. Duty Cycle vs TS Voltage

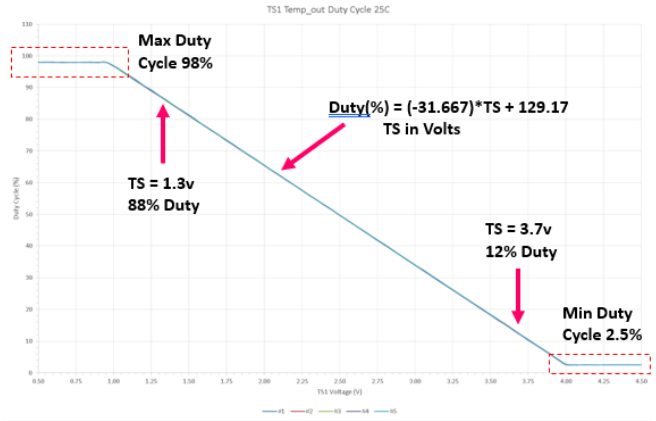

Figure 23. Typical behavior of TS pin vs TEMP_OUT Duty cycle

The target TEMP_OUT duty cycle encoding for the ADuM4177 is -40°C = 12% and 150°C = 88%. The ADuM4177 Temp_out Duty signal has a built in maximum duty cycle, 98% (typ), and minimum duty cycle, 2.5% (typ). If the TS voltage sense pins goes outside the normal range of operation, the Temp_out duty ratio will be fixed by the ADuM4177.

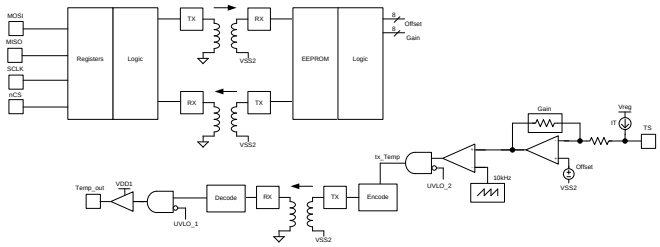

Figure 24. Temperature Sense basic block diagram

The ADuM4177 temperature sense is designed to work with external diode sense stack. An internal 200 µA (typ) bias current is used to bias the external diode stack. The ADuM4177 also contains trim capability to calibrate manufacturing variation in a temperature sense diode stack. The ADuM4177 allows for gain and offset trimming of the duty cycle response of the TS pi to allow for calibration due to variation in temperature sensing diode stacks.

The ADuM4177 TS pin can also be used with an external NTC rather than a diode stack. A resistor network may be needed to ensure the range of operation is within 1.3 V and 3.7 V.

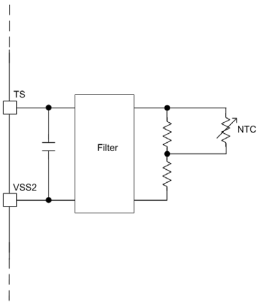

Figure 25. Example NTC Sense Element Configuration

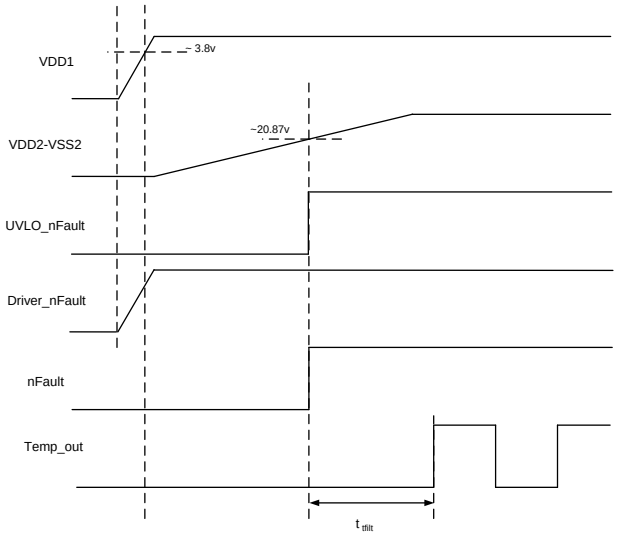

Figure 26. Temperature Sense Start-up Diagram

Figure 26 provides typical start-up diagram for the Temperature Sense output PWM duty cycle. After the V_{DD2}-V_{SS2}

UVLO clears, the TEMP_OUT duty cycle will be valid within time t_{FILT}, 3.15ms (max).

Temperature Sense Duty Cycle Register

In addition to having the Temp_out pin to read the 1kHz (typ) temperature sense duty cycle, the ADuM4177 offers two addressable registers to read the TS pin and an internal secondary side diode via the SPI interface, registers 0x08 and 0x09.

Register 0x08 provides the duty cycle of the TS pin voltage sensed by the diode stack, or NTC.

Register 0x09 provides temperature information for the secondary driver die of the ADuM4177. The data present in register 0x09 is the duty cycle of the equivalent temperature seen on the secondary side die. The temperature is given by the following equation:

$$T = (-6.374) * D + 415.923$$

where D is given as a %, read from register 0x09,

T is given as temperature in C.

The temperature sense on the secondary side operates at 10 kHz (typ). Data is captured on the secondary side for both TS and the internal diode, and transferred to the primary side at the rising edge at the start of the next cycle 10 kHz (typ) clock. ADuM4177 utilizes a "boxcar" filtering technique with the following equation:

$$val = \frac{val_{-1}}{2} + \frac{x}{2}$$

where x is the new temperature sense value obtain,

val_{-1} is the previous calculated average value,

and val is the new average calculation which will be transferred to IC1.

At the end of a data transfer, both TS and the internal diode PWM registers will be updated. Temperatures sense values are updated every 100 µs (typ) and can be obtained by a read through the SPI interface.

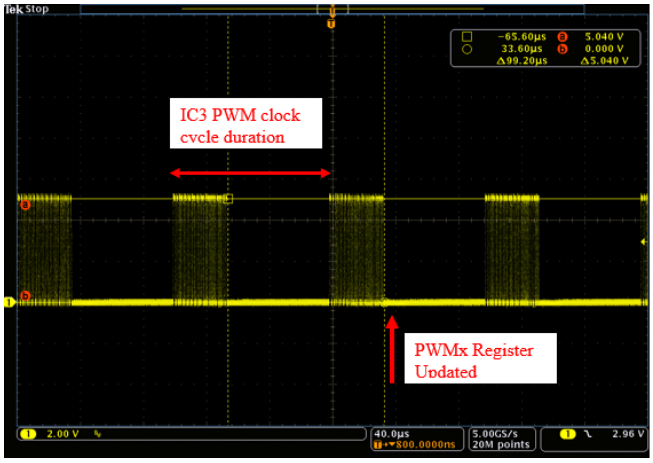

Figure 27. Temperature sense data transfer

TS Analog Input

The ADuM4177 offers to ability to disable the TS pin 200 µA (typ) bias current. This can be done by setting bit <0> in register 0x53. The default value for bit <0> is 0, so the current bias is enabled by default.

Disabling the TS pin current allows the TS pin to be used as a pure analog input. The TS pin voltage can be monitored via the TEMP_OUT duty cycle, or one can read the Temp_out duty cycle using register 0x08. The transfer curve is:

$$TEMP\_OUT(DUTY) = (-31.667) \times V_{TS1} + 129.17$$

Where

TEMP_OUT(DUTY) = duty cycle of the TEMP_OUT pin.

V_{TS1} = voltage seen on TS pin.

TS Comparator Thresholds

Figure 28 provides a detailed block diagram of the ADuM4177 Temperature Sense. The ADuM4177 has built in comparators on the TS pin that can be configured to two different thresholds. The comparator thresholds can be set via the SPI bus writing to register 0x53. Note, only one comparator threshold can be configured at a time. The default configuration is that the TS comparator is disabled. When enabled, the comparator output will map to the Driver_nFault flag. The TS comparator threshold will not create a fault on the secondary side, meaning it will not force the driver in to a soft-shutdown. When enabled, the TS comparator will only flag on the primary side DRIVER_nFAULT pin.

TS comparator threshold 1 is a falling threshold, 1.3v (typ). One application for this threshold is as a TS pin OT threshold.

TS comparator threshold 2 is a rising threshold, 3v (typ). With the TS pin configured as a pure analog input, this threshold can be used as a HV sense threshold.

Using the TS_COMP_FLT_EN bit, the user can enable a 1.64 ms (typ) filter to the TS comparator. Setting TS_COMP_FLT_EN to '0' enables the filter, and '1' disables the filter. This can be used to filter noise seen on the TS pin during sensing. The default state for the TS comparator filter time is '0', meaning filter is enabled.

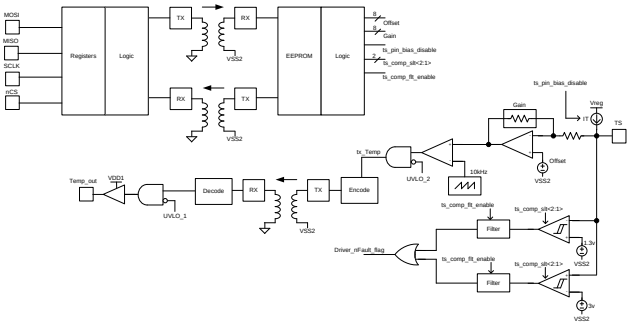

Figure 28. TS pin configurable comparators

TS PWM Update Fault

The primary side of the ADuM4177 requires periodic updates of the TS and internal diode Temperature Sense PWM data. If a PWM update is not received on the primary side within two rising edges of the TEMP_OUT PWM signal, a fault is issued to bit 3 of the primary side Digital Status Register, address 0x01. If a PWM update is received after the fault, the TEMP_OUT PWM signal will resume, but the fault will remain posted in the primary side Digital Status Register until it is cleared by the user.

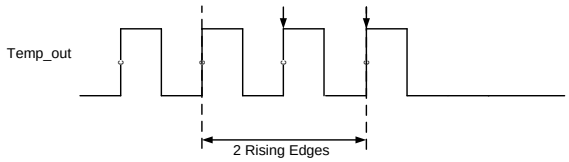

Figure 29. Example TEMP_OUT Watchdog Timing

GATE DRIVE

The ADuM4177 gate drive has integrated low Rdson, 0.4 Ω (typ), power FETs to drive up to 30 A of peak short circuitcurrent. The ADuM4177 has an integrated low Rdson soft-shutdown 0.6 Ω (typ) FET to realize critical shutdown requirements for SiC devices. With an external resistor, the soft-shutdown can be adjusted. Using an open drain drive pin, the ADuM4177 can drive an external Miller clamp device. Utilizing an external Miller switch allows critical component placement to reduce PCB inductance which affects the performance of the SiC device.

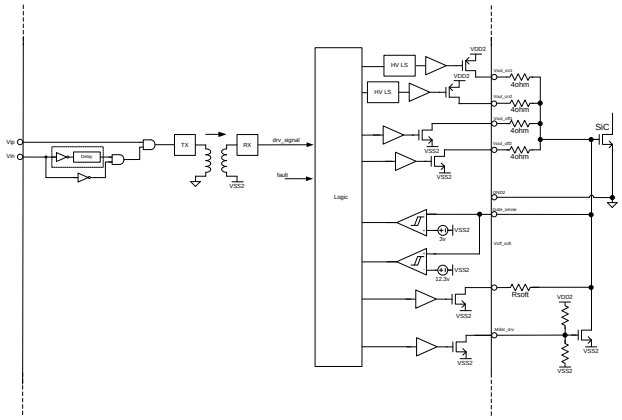

Figure 30. Driver Functional Block Diagram

Slew Rate Control

The ADuM4177 contains a programmable feature via the SPI interface to change the drive strength of the gate driver to change the slew rate of the rise and fall gate waveforms. The rise time and fall time can be modified individually. Figure 31 and Figure 32 provide functional diagrams for the driver output of the ADuM4177. Figure 33 provides typical waveforms for the driver output while configuring the rising gate drive and the falling gate drive.

Since the slew rate control signals will be updated asynchronously to the driver signal, care must be taken to ensure there is no disruption to the drive signal at the SiC gate. As shown in both Figure 31 and Figure 32, the Vout_on and Vout_off slew will not be updated until the first rising edge of the driver signal after either the gd_off_slew_slct and gd_on_slew_slct registers bits have been updated.

Table 8 provides the typical Vout_on and Vout_off Rdson values for configured slew rate settings. The default configuration is for all internal gate drive FETs to be active.

The slew rate settings can be configured in register 0x55 bit <0> of register 0x55 controls the V_{OUT_OFF2} switch. Bit<1> of register 0x55 controls the V_{OUT_ON2} switch.

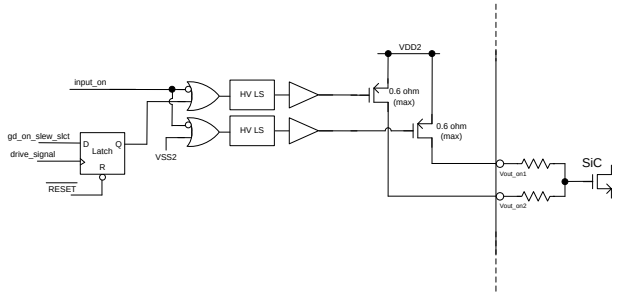

Figure 31. V_{OUT_ONX} Slew Rate Control

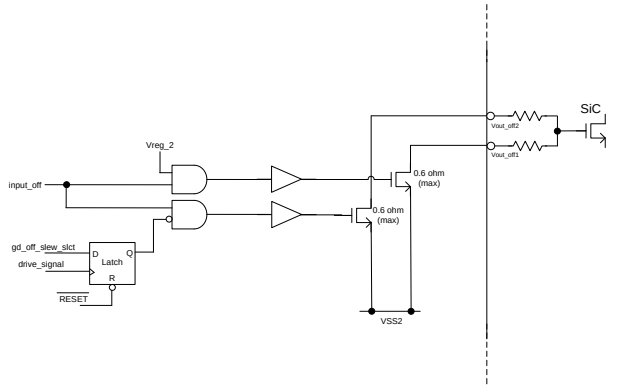

Figure 32. V_{OUT_OFFX} Slew Rate Control

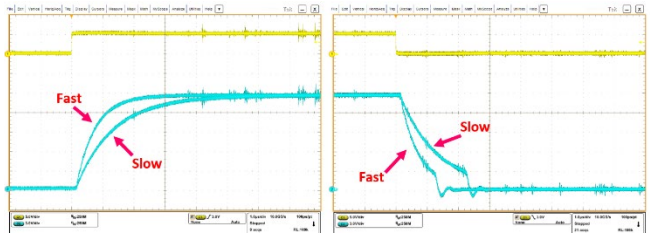

Figure 33. Slew Rate Control Waveforms

PROTECTION FEATURES

Desaturation Detection

The ADuM4177 contains an integrated DESAT function for IGBT and SiC devices. During normal operation, when the

power device is on, the expected drain to source voltage should be below a given value. During high current events, this voltage can rise, allowing for detection of a power device that is under a short circuit situation, or not able to hold the drain to source voltage down. If the drain to source voltage increases higher than the DESAT threshold, the DESAT pin can be pulled up allowing for desaturation event detection. The rising DESAT threshold is 7 V (typ). The DESAT pin charging current is set using an external resistor. An internal pull-up current, 10 µA (typ), is used for open pin detection. The delay from DESAT rising to the start of the soft-shutdown, t_{DESAT_DLY}, is 100 ns (typ).

The ADuM4177 DESAT function includes a gate sense control and programmable delay to blank the DESAT input after Vi+ has commanded the output high. The gate sense control monitors the gate voltage to transition above 12.3V (typ) with respect to VSS2 before initiating the programmable delay. The selected threshold is approximately the end of the miller plateau voltage. The programmable delay is selectable between 0ns and 700ns. Employing both functions adjusts the blanking delay to the switch size and load conditions. Noisier and/or slower switching devices need longer blanking times. The gate sense control can be disabled with the register address 0x53 bit 4 GSR_DESAT_DIS. The programmable delay is adjusted with resister address 0x54 bits 5:3.

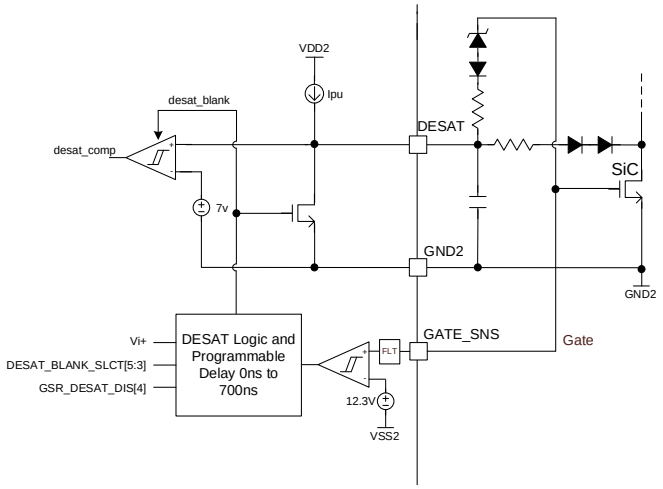

Figure 34. Typical DESAT Configuration

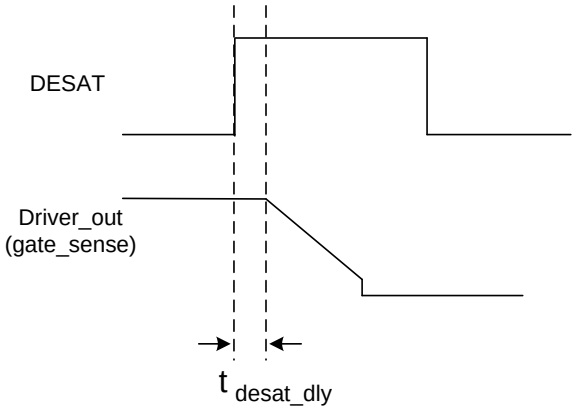

Figure 35. DESAT to Soft-shutdown Delay

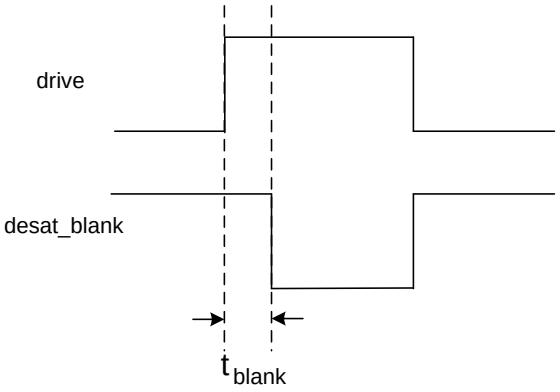

Figure 36. Example DESAT Blanking Time

Non-Overlap Protection

The ADuM4177 has both non-inverting, VI+, and inverting, VI-, input pins to control the driver output. The VI+ and VI- pins can be used to protect the driver path for overlapping signals. If the non-overlap timing between VI+ and VI- is shorter than the externally controlled deadtime, t_{DEXT}, (typically 0.5 µs) a DT_FAULT will be issued to the DRIVER_nFAULT pin, t_{PW} is 13ms (typ).

A functional diagram for the DT_Fault behavior is shown in Figure 40. In addition to monitoring the state of VI+ with respect to VI-, when a DT_FAULT is active and both VI+ and VI- are set low, the fault will clear after a 26 ms (typ) time-out.

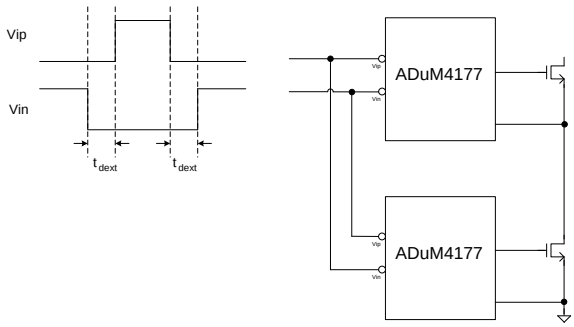

Figure 37. Non-Overlap Protection

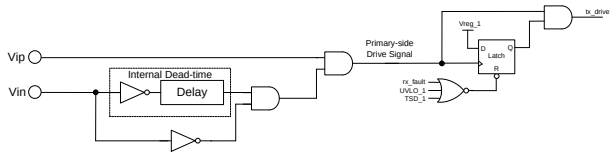

Figure 38. Functional Equivalent Diagram for Deadtime Control

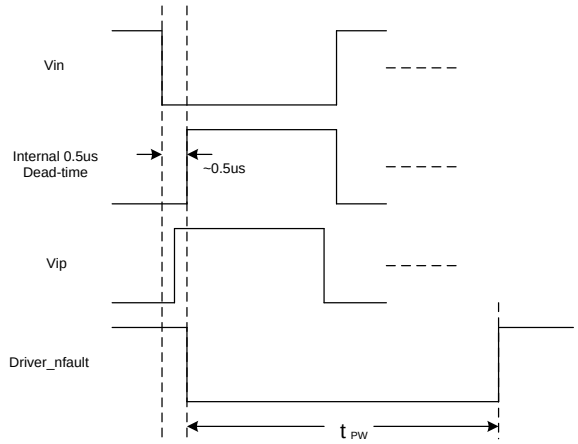

Figure 39. DT_FAULT Timing Diagram

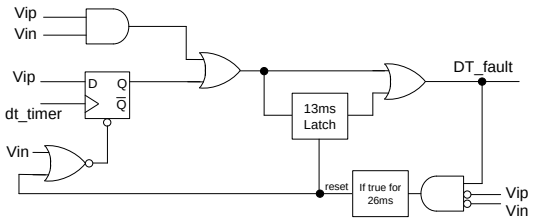

Figure 40. Deadtime Latch

GATE_SENSE, Soft-Shutdown, and Miller Clamping

The ADuM4177 has an integrated soft-shutdown switch with 0.6 Ω (typ) Rdson. This allows the soft-shutdown time to be adjusted with an external resistor, Figure 42 provides a functional diagram for the GATE_SENSE, soft-shutdown and Miller drive pins. With an external resistor, and low Rdson integrated soft-shutdown switch, the turn-off time for SiC switch can be adjusted to meet a 1 µs (typ) shutdown time needed for most SiC devices.

As shown in Figure 41, the ADuM4177 utilizes an external Miller clamp switch. With an external Miller switch, the PCB layout can be optimized to minimize trace inductance which impacts performance with high speed SiC devices. The Miller clamp drive pin utilizes the voltage on the GATE_SENSE pin to determine when to enable the Miller clamp. When the GATE_SENSE pin falls to 3 V (typ), gs_f in Figure 41, the Miller clamp is activated and the external Miller switch will be enabled. The Miller clamp operates in both normal drive operation and soft-shutdown.

With the gs_r and gs_f signals detecting both the rising and falling SiC gate signals, the ADuM4177 can detect short events on the SiC gate. As shown in Figure 42, with the turn-on of the driver output, if the SiC gate does not exceed 12.3 V (typ), with respect to V_{SS2}, after 3.2 µs (typ) the ADuM4177 will issue a Gate Low Fault (GL_FAULT). Similarly, for the turn-off of the driver output, if the SiC gate does not go below 3 V (typ), with respect to V_{SS2}, after 3.2 µs (typ) the ADuM4177 will issue a Gate High Fault (GH_FAULT).

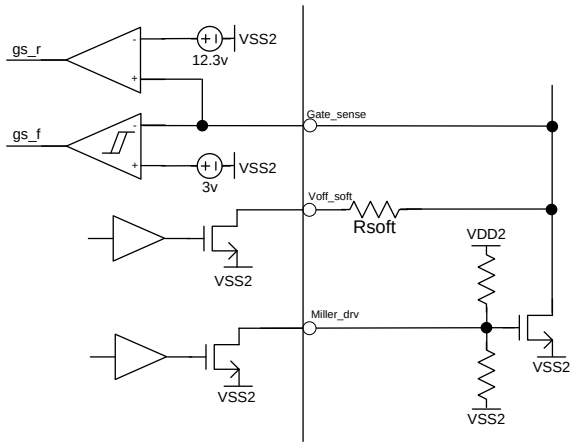

Figure 41. Soft-shutdown and Miller Functions

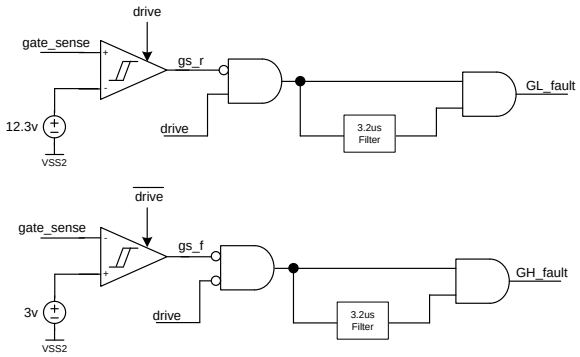

Figure 42. Gate Low and High Fault Detect

ASC – Active Short Circuit

The ADuM4177 is designed with an Active Short Circuit (ASC) pin on the secondary side. The ASC pin can be used to enable the driver output from the secondary side. The threshold of the ASC comparator is 8 V (typ), with an internal 150 µA (typ) pull-down current to prevent false triggering in the event of an open pin, see Figure 43.

Figure 44 provides a logic functional equivalent diagram of the ASC pin control of the drive signal. The asc_sig value is the signal from the ASC comparator output, the drv_signal is the drive signal from the driver receiver channel and drive is the signal which controls the secondary side driver stage. With no fault present, the ASC signal can freely control the driver stage. A fault generated on the secondary side will over-ride the ASC signal, and force the driver stage to enter a soft-shutdown.

To allow the ASC to remain in control of the output in the presence of fault conditions set register 0x53 bit 6 (ASC_DOMIN_ENA). With ASC_DOMIN_ENA set the ASC

input will control VOUT_ON high in the presence of any faults including DESAT. When the ASC signal is high the driver_nFault output is set low in conjunction with any additional faults.

Figure 45 provides a timing diagram for the rising propagation delay, t_{ASC_R}, and the falling propagation delay, t_{ASC_F}. Typical ASC rising propagation delay is 100 ns (typ), while typical ASC falling propagation delay is 120 ns (typ).

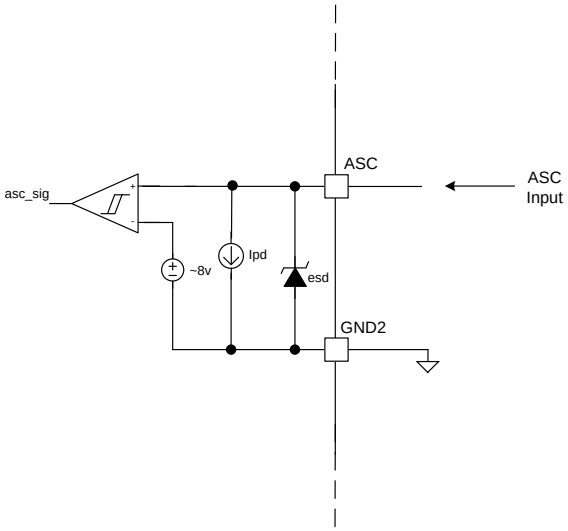

Figure 43. Active Short Circuit Functional Diagram

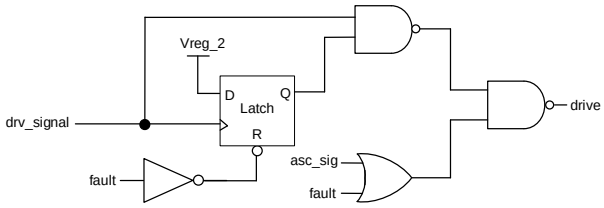

Figure 44. ASC Functional Logic

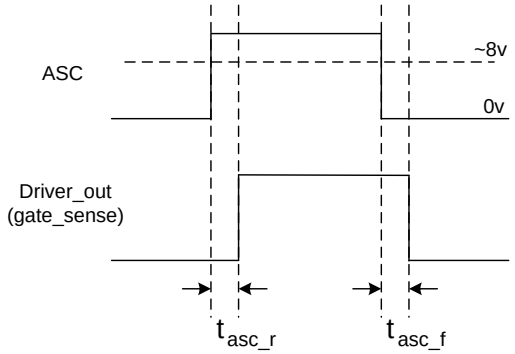

Figure 45. ASC Propagation Delays

Thermal Shutdown

The ADuM4177 contains two thermal shutdowns (TSDs). If the internal temperature of the primary or secondary side of the ADuM4177 exceeds 155°C (typical), the ADuM4177 enters a TSD fault, and the gate drive is disabled by means of a soft shutdown. When a TSD occurs, the ADuM4177 does not leave TSD until the internal temperature has dropped below 135°C (typical). After reaching this temperature, the ADuM4177 exits shutdown. A fault output is available on the primary side during a TSD event on the secondary side by means of the $\overline{\text{FAULT}}$ pin.

The primary side leaves TSD when the internal temperature has dropped below 135°C (typical).

The main cause of overtemperature is driving too large of a load for a given ambient temperature. This type of temperature overload typically affects the secondary side die because this is where the main power dissipation for load driving occurs.

FAULTS

Three fault pins on the primary side allow for fault differentiation; $\overline{\text{FAULT}}$, Driver_nFault and UVLO_nFault, Figure 46 provides functional pin equivalent diagrams for each of the fault pins. The $\overline{\text{FAULT}}$, Driver_nFault, and UVLO_nFault pins have internal active pull-down NMOS devices internal to the ADuM4177, and have integrated 100 µA (typ) pull-up currents.

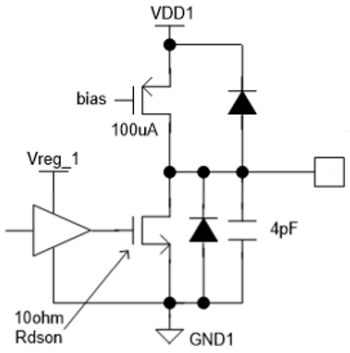

Figure 46. Fault Pin Equivalent Diagrams, $\overline{\text{FAULT}}$, Driver_nFault, and UVLO_nFault

Table 7 provides details on how the faults map to the primary side fault pins. Figure 47 provides a functional diagram for the fault mapping for both the primary and secondary side of the ADuM4177. Please note, the primary side TSD will map to the $\overline{\text{FAULT}}$ pin. The V_{DD1} UVLO will map to both the $\overline{\text{FAULT}}$ and the UVLO_nFault pins. There are no latch times associated with V_{DD1} UVLO and primary side TSD. Both of these faults will de-assert the $\overline{\text{FAULT}}$ and UVLO_nFault pins for as long as the fault persists. As shown in Table 7 and Figure 47, the ASC pin maps to the Driver_nFault. There is no latch time associated with the ASC pin fault flag. The ASC pin will de-assert the Driver_nFault pin for as long as the ASC event persists.

Table 7. Fault Pin Mapping

Fault	$\overline{\text{FAULT}}$	DRIVER_nFAULT	UVLO_nFAULT
Primary Side TSD			Persist
Secondary Side TSD			10 ms
DESAT	20 ms	30 ms	

Gate error	20 ms	30 ms	10 ms
VDD2/VSS2 UVLO	20 ms		10 ms
VDD2/VSS2 OVP	20 ms		
CRC error		Persist	
ECC error		Persist	Persist
ASC		Persist	
DT_Fault		13 ms	

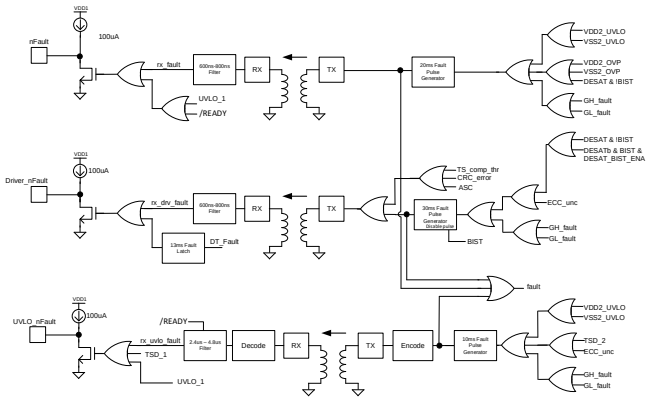

Figure 47. Fault Behavior Functional Diagram

Fault Latch Times

Each fault pin flag has an associated latch time, t_{PW}:

$\overline{\text{FAULT}}$	20 ms (typ)
UVLO_nFault	10 ms (typ)
Driver_nFault	13 or 30 ms (typ)

If a fault occurs, the respective fault pin will latch for the associated latch time. If the fault occurs for less time than t_{PW}, then the fault will hold for only the time t_{PW}, see Figure 48. If a fault occurs, and it lasts longer than t_{PW}, then the fault will hold for as long as the fault persists as shown in Figure 49.

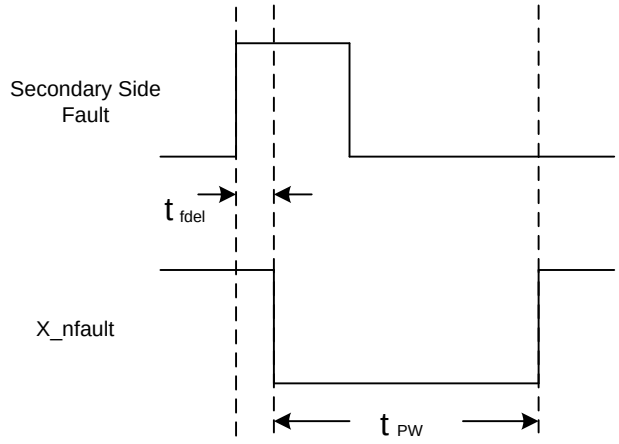

Figure 48. Fault Timing Diagram if Fault Time < t_{PW}

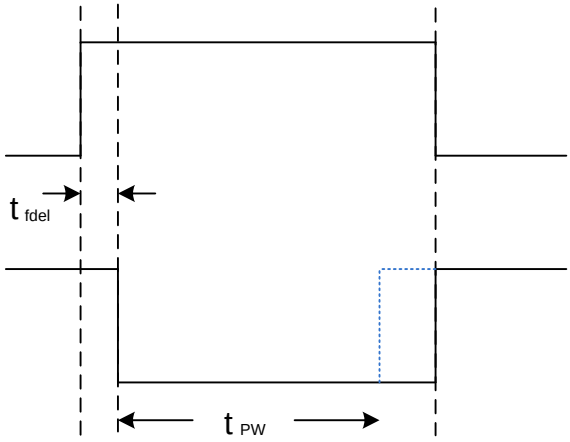

Figure 49. Fault Timing Diagram if Fault Time > tPW

As can be seen in Table 7 and Figure 47, the DT_Fault maps to the Driver_nFault pin. A DT_Fault can be distinguished between other Driver_nFault fault events by the latch time. The DT_Fault latch time is 13 ms (typ), versus the normal 30 ms (typ) Driver_nFault latch time.

The posting time for a fault, t_{fdel}, is the time from the fault event to the falling edge of the fault pin. This time is given as follows for each fault signal:

$\overline{\text{FAULT}}$	t_{PW}	600 – 800 ns (typ)
UVLO_nFault	t_{PW}	2.4 – 4.8 µs (typ)
Driver_nFault	t_{PW}	600 – 800 ns (typ)

The $\overline{\text{FAULT}}$ and Driver_nFault delays are discrete filters based on a 200 ns (typ) clock from a fault signal directly driven from the secondary side. The UVLO_nFault delay is based on a pulse train that is used as a "heart beat" for the secondary side. A secondary side fault will force the pulse train off, indicating a fault on the primary side. In the event of power loss on the secondary side, the primary side is always guaranteed to show a fault at least on the UVLO_nFault and $\overline{\text{FAULT}}$, providing power is present on VDD1.

Configurable Faults

The ADuM4177 has two configurable faults, CRC_error and TS Comparator Threshold. The default state is that both CRC_error and TS Comparator Threshold faults do not map to any fault pin. Each fault can be configured individually. Register 0x53 is used to enable the TS pin threshold, this is done with bit<2:1>. If either TS comparator threshold is enabled, the fault is enabled and mapped to the Driver_nFault pin. Register 0x54 is used to enable the CRC_error fault, this is done with bit<6>. If enabled, the CRC_error will map to the Driver_nFault pin.

Neither the CRC_error nor the TS pin comparator threshold will affect the driver state. The occurrence of either event will only post a flag on the primary side Driver_nFault pin. In

addition, neither the CRC_error, nor the TS pin comparator threshold, are latched. The Driver_nFault low state will only persist for as long as the CRC_error event, or the TS pin comparator event occurs. Figure 50 provides a functional block diagram for the configurable fault signals.

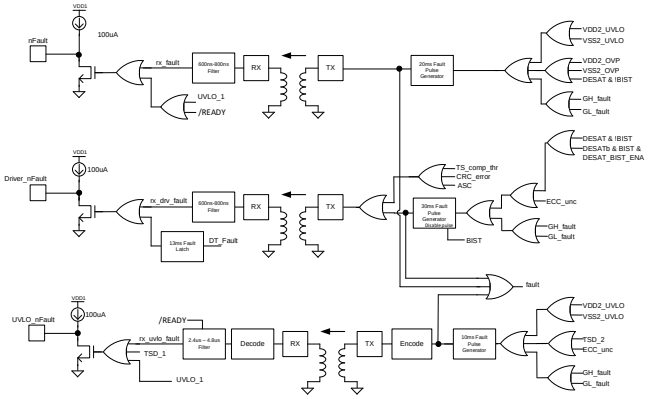

Figure 50. User Configurable Faults

Fault Register Information

There are 4 registers which post faults that occur during the ADuM4177 operation, addresses 0x00, 0x01, 0x40, and 0x41. The information posted to any of these 4 fault registers do not directly affect operation. If a fault occurs, and posts to a specific fault register, the register does not have to be cleared to affect operation. Using the SPI interface, the faults can be monitored digitally, and used for debug purposes in addition to the fault flag pins on the primary side.

The default value for a fault bit is '0'. If a fault occurs, a '1' will be written to the specific bit and register. To clear the information, write a '1' to the fault register and bit location. A flow chart of the fault clearing process is shown in Figure 51.

The fault registers are volatile. If power is lost on either V_{DD1} or V_{DD2}-V_{SS2}, the information stored on the respective register locations will be lost.

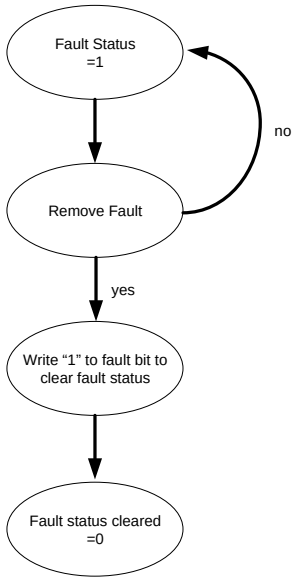

Figure 51. Status Register Flow Chart

BIST

The ADuM4177 has various built in self testing, BIST (Built-in Self Test), features.

For the SPI interface, the CRC is built in to the overall protocol. This will allow the user to ensure data is correct during both an SPI read and write. In addition, the ADuM4177 has a "Communication Fault" feature. If an incorrect number of bits is sent to the ADuM4177, this will indicate an SPI problem. This is particularly important as it will also capture errors during the transfer of data across the die-to-die interface between the primary and secondary dice within the ADuM4177.

The EEPROM on the ADuM4177 has two BIST features; ECC and a "Program Fault". The ECC will correct any single bit error in any of the EEPROM registers. Any corrected, or uncorrected, bit fault will be notified to the user. The ECC is dynamic and will be active not only at start-up, but during normal operation. Also built in to the ADuM4177 EEPROM is a "Program Fault" feature. This will indicate an error during any EEPROM program attempt. During programming, the ADuM4177 takes additional measures to ensure proper operation. To write to a register, the simulate bits must be set to '1', but to program an EEPROM register, both simulate bits must be set to '1' as well as the program bit. This helps prevent false programming to the EEPROM.

During start-up, the ADuM4177 will run a read/write check on the following registers:

0x00 IC1 Analog Status

0x40 IC3 Analog Status

The ADuM4177 will ensure that each bit can be written to and cleared. If this fails, a "BIST Failed" fault will be written to the Digital Status register on both IC1 or IC3.

The DESAT circuitry includes BIST. Prior to the release of the UVLO_nFault during startup, the ADuM4177 internally stimulates the DESAT comparator with high and low inputs as shown in Figure 52. The results are stored in register 0x41, Bit 2, BIST_FAULT. If Register 0x53 bit 5, DESAT_BISTOBS_ENA is set to "1", the DESAT comparator will output the result of the internal comparator excitations, as long as VDD1 has been above 4 V for longer than 50 µs before VDD2 is powered up, allowing the user to observe the comparator going high and low. Three pulses of 8 µs (typ) starting low, then high, then low demonstrate the DESAT comparator is operational. The timing for outputting the comparator results to the DRIVER_nFAULT pin is shown in Figure 54.

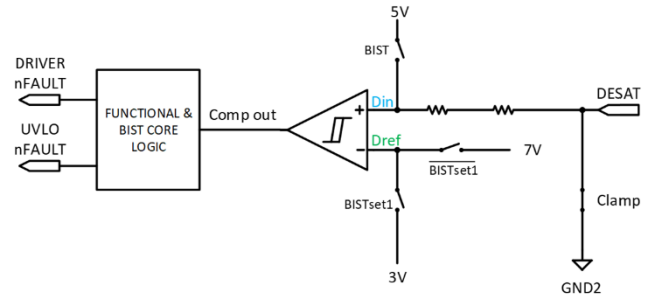

Figure 52. DESAT BIST Functional Block Diagram

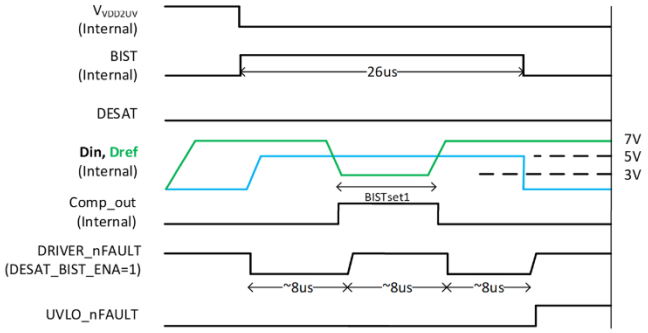

Figure 53. DESAT BIST Sequence Diagram

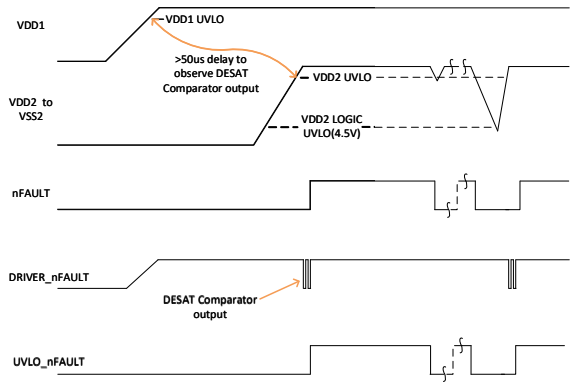

Figure 54. DESAT_BISTOBS_ENA = "1" Output Timing Example

POWER DISSIPATION

When driving a power device gate, the driver must dissipate power. This power can lead to operation outside of specifications, and/or TSD if the following considerations are not made. Total gate charge of the device being driven dictates the loading that occurs during switching. With this value, the estimated total power dissipation (P_{DISS}) in the system due to switching action is given by the following equation:

$$P_{DISS} = Q_{TOT} \times (V_{DD2}\text{-}V_{SS2}) \times f_S$$

where:
Q_{TOT} is the total gate charge of the power device
V_{DD2} is the voltage on the V_{DD2} pin.

V_{SS2} is the voltage on the V_{SS2} pin.

f_S is the switching frequency of power device.

This power dissipation is shared between the internal on resistances of the internal gate driver switches and the external gate resistances, R_{GON} and R_{GOFF}. The ratio of the internal gate resistances to the total series resistance allows the calculation of losses seen within the ADuM4177 chip.

Take the power dissipation found inside the chip due to switching, adding the quiescent power losses, and multiplying it by the θ_{JA} gives the rise above ambient temperature that the ADuM4177 experiences.

$$P_{DISS\_ADUM4177} = P_{DISS} \times 0.5(R_{DSON\_P} \div (R_{GON} + R_{DSON\_P}) + (R_{DSON\_N} \div (R_{GOFF} + R_{DSON\_N})) + P_{QUIESCENT}$$

where:
$P_{DISS\_ADUM4177}$ is the power dissipation of the ADuM4177.
R_{GON} is the external series resistance in the on path.
P_{GOFF} is the external series resistance in the off path.
$P_{QUIESCENT}$ is the quiescent power.

$$T_{ADuM4177} = \theta_{JA} \times P_{DISS\_ADuM4177} + T_{AMB}$$

where:
$T_{ADuM4177}$ is the junction temperature of the ADuM4177.
T_{AMB} is the ambient temperature.

For the ADuM4177 to remain within specification, $T_{ADuM4177}$ cannot exceed 150°C (typical). When $T_{ADuM4177}$ exceeds 155°C (typical), the ADuM4177 enters TSD.

SPI REGISTERS

ADuM4177 Register List:

Address	R/W	Name	Default Setting [14:0]
0x00	R	IC1_ANALOG_STATUS	
0x01	RW	IC1_DIGITAL_STATUS	000 0000 0000 0000
0x08	R	PWM1_DUTY	
0x09	R	PWM2_DUTY	
0x3F	R	IC1_CHIP_ID	
0x40	R	IC3_ANALOG_STATUS	
0x41	RW	IC3_DIGITAL_STATUS	000 0000 0000 0000
0x42	RW	CONTROL	000 0000 0000 0000
0x50	RW	GAIN1	000 0000 0000 0000
0x51	RW	OFFSET1	000 0000 0000 0000
0x52	RW	VSS2_UVLO_DISABLE	000 0000 0000 0000
0x53	RW	USER_CFG1	000 0000 0000 0000
0x54	RW	USER_CFG2	000 0000 0000 1101
0x55	RW	USER_CFG3	000 0000 0000 0000
0x7F	R	IC3_CHIP_ID	

Address: 0x00, Reset: 0x0000, Name: IC1_ANALOG_STATUS

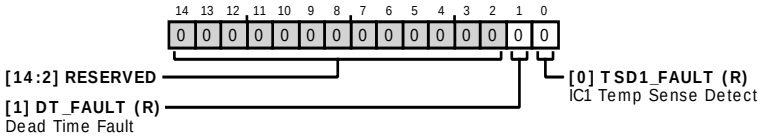

Table 8. Bit Descriptions for IC1_ANALOG_STATUS

Bits	Bit Name	Description	Reset	Access
[14:2]	RESERVED	Reserved.	0x0	R
1	DT_FAULT	Dead Time Fault.	0x0	R
0	TSD1_FAULT	IC1 Temp Sense Detect.	0x0	R

Address: 0x01, Reset: 0x0000, Name: IC1_DIGITAL_STATUS

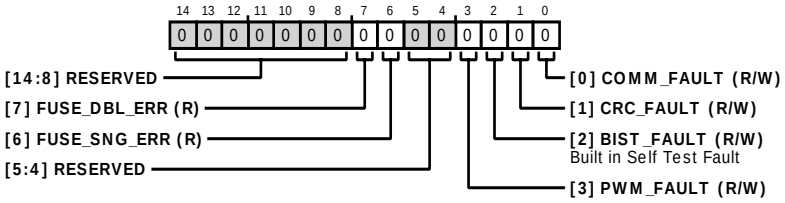

Table 9. Bit Descriptions for IC1_DIGITAL_STATUS

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
7	FUSE_DBL_ERR		0x0	R
6	FUSE_SNG_ERR		0x0	R
[5:4]	RESERVED	Reserved.	0x0	R
3	PWM_FAULT		0x0	R/W

Bits	Bit Name	Description	Reset	Access
2	BIST_FAULT	Built in Self Test Fault.	0x0	R/W
1	CRC_FAULT		0x0	R/W
0	COMM_FAULT		0x0	R/W

Address: 0x08, Reset: 0x0000, Name: PWM1_DUTY

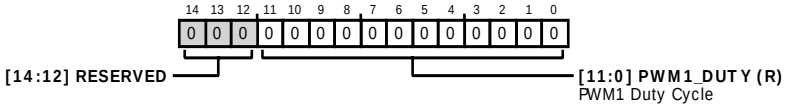

Table 10. Bit Descriptions for PWM1_DUTY

Bits	Bit Name	Description	Reset	Access
[14:12]	RESERVED	Reserved.	0x0	R
[11:0]	PWM1_DUTY	PWM1 Duty Cycle.	0x0	R

Address: 0x09, Reset: 0x0000, Name: PWM2_DUTY

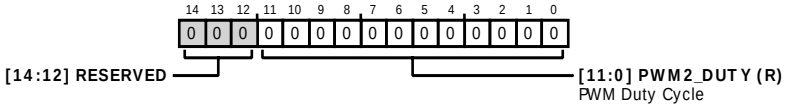

Table 11. Bit Descriptions for PWM2_DUTY

Bits	Bit Name	Description	Reset	Access
[14:12]	RESERVED	Reserved.	0x0	R
[11:0]	PWM2_DUTY	PWM Duty Cycle.	0x0	R

Address: 0x3F, Reset: 0x0000, Name: IC1_CHIP_ID

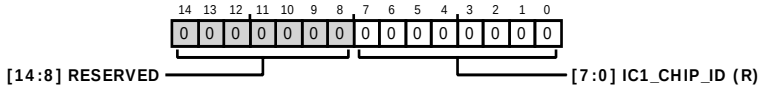

Table 12. Bit Descriptions for IC1_CHIP_ID

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
[7:0]	IC1_CHIP_ID		0x0	R

Address: 0x40, Reset: 0x0000, Name: IC3_ANALOG_STATUS

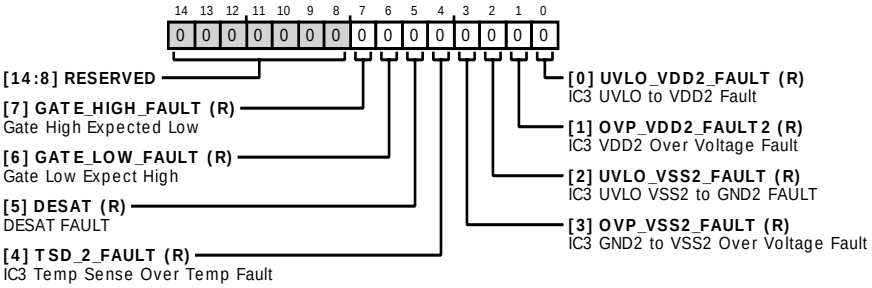

Table 13. Bit Descriptions for IC3_ANALOG_STATUS

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
7	GATE_HIGH_FAULT	Gate High Expected Low.	0x0	R
6	GATE_LOW_FAULT	Gate Low Expect High.	0x0	R
5	DESAT	DESAT FAULT.	0x0	R
4	TSD_2_FAULT	IC3 Temp Sense Over Temp Fault.	0x0	R
3	OVP_VSS2_FAULT	IC3 GND2 to VSS2 Over Voltage Fault.	0x0	R
2	UVLO_VSS2_FAULT	IC3 UVLO VSS2 to GND2 FAULT.	0x0	R
1	OVP_VDD2_FAULT2	IC3 VDD2 Over Voltage Fault.	0x0	R
0	UVLO_VDD2_FAULT	IC3 UVLO to VDD2 Fault.	0x0	R

Address: 0x41, Reset: 0x0000, Name: IC3_DIGITAL_STATUS

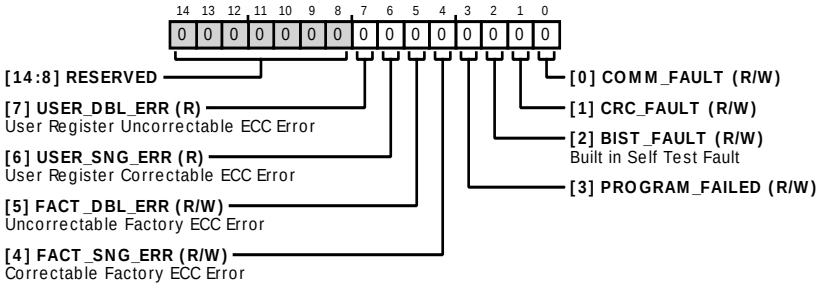

Table 14. Bit Descriptions for IC3_DIGITAL_STATUS

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
7	USER_DBL_ERR	User Register Uncorrectable ECC Error.	0x0	R
6	USER_SNG_ERR	User Register Correctable ECC Error.	0x0	R
5	FACT_DBL_ERR	Uncorrectable Factory ECC Error.	0x0	R/W
4	FACT_SNG_ERR	Correctable Factory ECC Error.	0x0	R/W
3	PROGRAM_FAILED		0x0	R/W
2	BIST_FAULT	Built in Self Test Fault.	0x0	R/W
1	CRC_FAULT		0x0	R/W
0	COMM_FAULT		0x0	R/W

Address: 0x42, Reset: 0x0000, Name: CONTROL

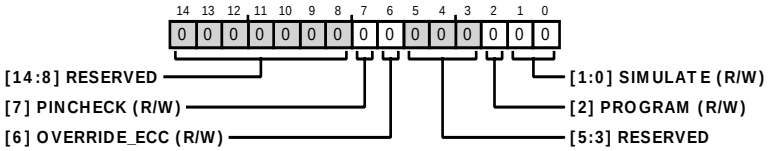

Table 15. Bit Descriptions for CONTROL

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
7	PINCHECK		0x0	R/W
6	OVERRIDE_ECC		0x0	R/W
[5:3]	RESERVED	Reserved.	0x0	R
2	PROGRAM		0x0	R/W
[1:0]	SIMULATE		0x0	R/W

Address: 0x50, Reset: 0x0000, Name: GAIN1

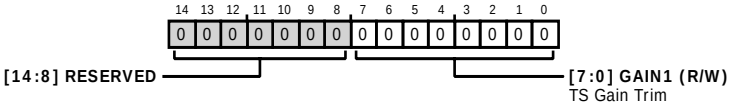

Table 16. Bit Descriptions for GAIN1

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
[7:0]	GAIN1	TS Gain Trim.	0x0	R/W

Address: 0x51, Reset: 0x0000, Name: OFFSET1

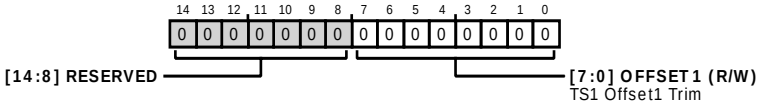

Table 17. Bit Descriptions for OFFSET1

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
[7:0]	OFFSET1	TS1 Offset1 Trim.	0x0	R/W

Address: 0x52, Reset: 0x0000, Name: VSS2_UVLO_DISABLE

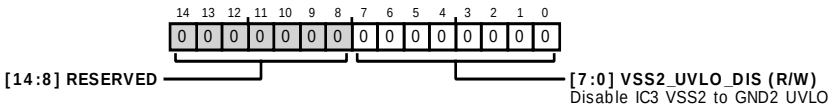

Table 18. Bit Descriptions for VSS2_UVLO_DISABLE

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
[7:0]	VSS2_UVLO_DIS	Disable IC3 VSS2 to GND2 UVLO.	0x0	R/W

Address: 0x53, Reset: 0x0000, Name: USER_CFG1

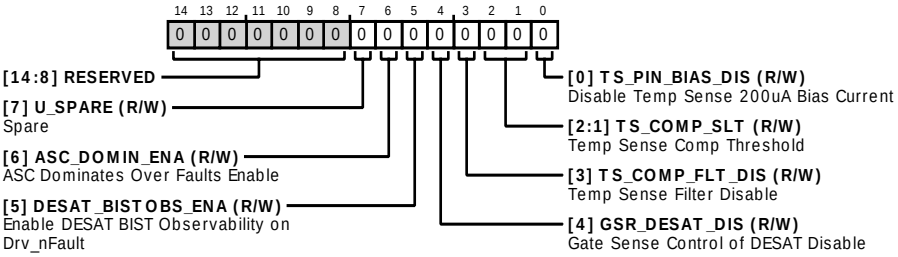

Table 19. Bit Descriptions for USER_CFG1

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
7	U_SPARE	Spare.	0x0	R/W
6	ASC_DOMIN_ENA	Enable ASC Dominates Over Faults and DESAT	0x0	R/W
5	DESAT_BISTOBS_ENA	Enable DESAT BIST Observability on Drv_nFault	0x0	R/W
4	GSR_DESAT_DIS	Gate Sense Control of DESAT Disable	0x0	R/W
3	TS_COMP_FLT_DIS	Temp Sense Filter Disable.	0x0	R/W
[2:1]	TS_COMP_SLT	Temp Sense Comp Threshold.	0x0	R/W
0	TS_PIN_BIAS_DIS	Disable Temp Sense 200 µA Bias Current.	0x0	R/W

Address: 0x54, Reset: 0x0000, Name: USER_CFG2

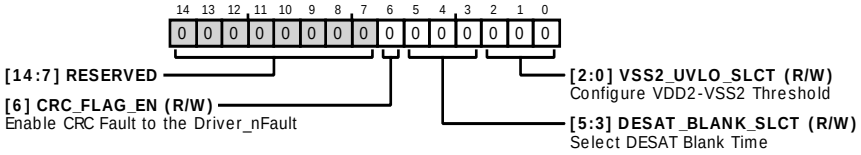

Table 20. Bit Descriptions for USER_CFG2

Bits	Bit Name	Description	Reset	Access
[14:7]	RESERVED	Reserved.	0x0	R
6	CRC_FLAG_EN	Enable CRC Fault to the Driver_nFault.	0x0	R/W
[5:3]	DESAT_BLANK_SLCT	Select DESAT Blank Time.	0x0	R/W
[2:0]	VSS2_UVLO_SLCT	Configure VDD2-VSS2 Threshold.	0x0	R/W

Address: 0x55, Reset: 0x0000, Name: USER_CFG3

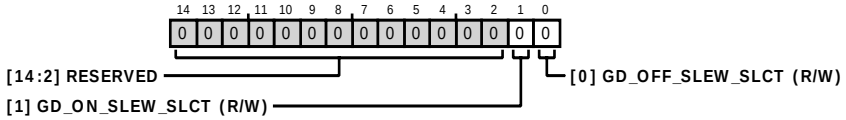

Table 21. Bit Descriptions for USER_CFG3

Bits	Bit Name	Description	Reset	Access
[14:2]	RESERVED	Reserved.	0x0	R
1	GD_ON_SLEW_SLCT		0x0	R/W
0	GD_OFF_SLEW_SLCT		0x0	R/W

Address: 0x7F, Reset: 0x0000, Name: IC3_CHIP_ID

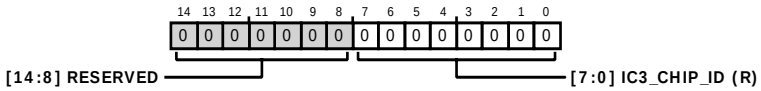

Table 22. Bit Descriptions for IC3_CHIP_ID

Bits	Bit Name	Description	Reset	Access
[14:8]	RESERVED	Reserved.	0x0	R
[7:0]	IC3_CHIP_ID		0x0	R

TYPICAL APPLICATION CIRCUIT

Figure 55 shows a typical application schematic of the ADuM4177. Variations on this schematic are possible.

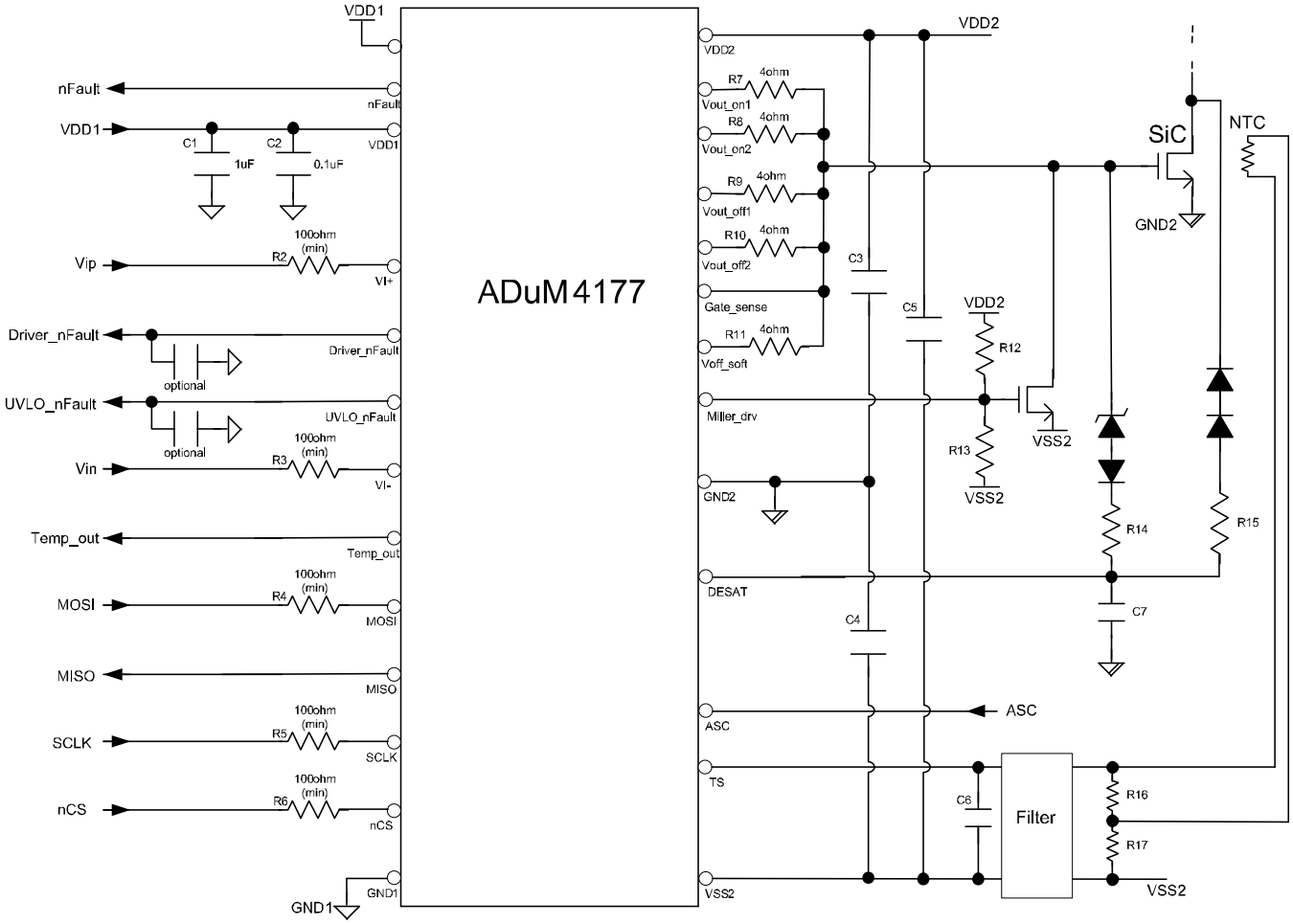

Figure 55. Typical Application Schematic

OUTLINE DIMENSIONS

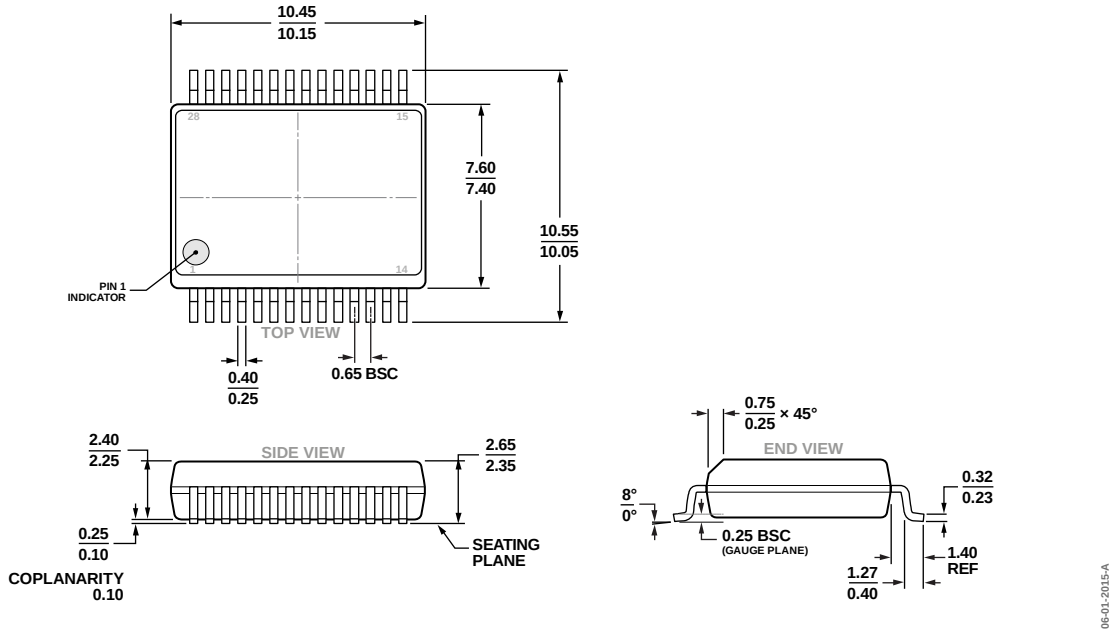

Figure 56. 28-Lead Standard Small Outline, Wide Body with Finer Pitch [SOIC_W_FP]
(RN-28-1)
Dimensions shown in millimeters

PR25543-9/20(PrA)