CY51X7

High-Performance PLL Die for Oscillators

Features

- Low-noise PLL Die for integrated crystal applications
- Differential clock output: Four frequencies selectable, reconfigurable by I^2C
- Output frequency support from 15 MHz to 2.1 GHz
- Fractional N PLL with fully integrated VCO
- Works on third overtone (OT3) of a fixed-frequency crystal, low-frequency fundamental (LFF), high-frequency fundamental (HFF) mode crystal, and low-frequency input
- LVPECL, CML, HCSL, LVDS, and LVCMOS output standards available
- Compatible with 3.3 V, 2.5 V, and 1.8 V supply
- 150 fs typical integrated jitter performance (12 kHz to 20 MHz frequency offsets) for output greater than 150 MHz
- VCXO functionality provided with tunable Total Pull Range (TPR) from ±50 ppm to ±275 ppm
- Die size facilitates integration with several integrated crystal package options

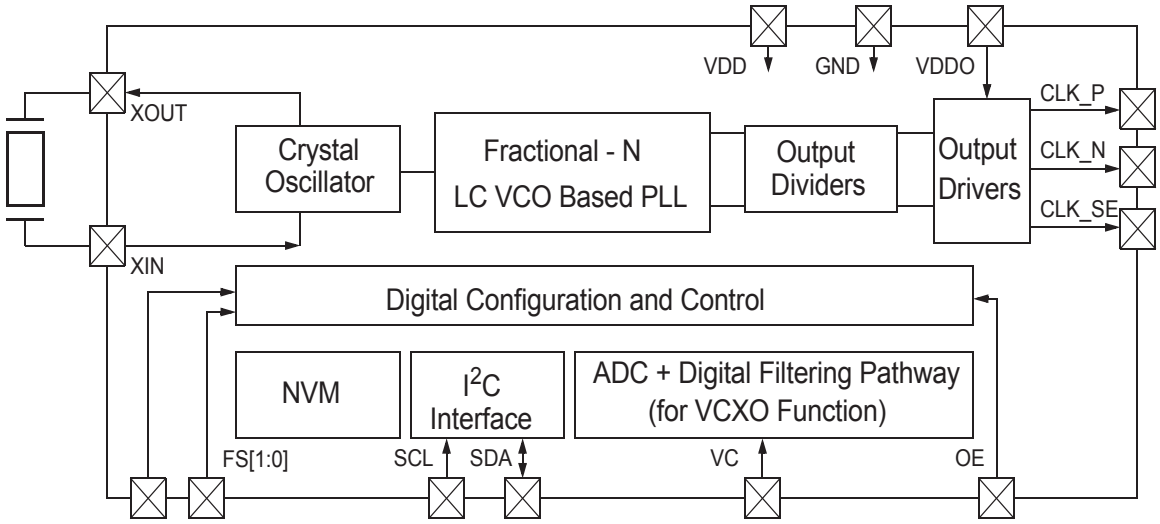
Functional Description

The CY51X7 is a Programmable PLL-based crystal oscillator solution with flexible output frequency options. It is field and factory programmable for any output frequency between 15 MHz and 2.1 GHz. Four frequencies are independently programmable on the differential output with the frequency select (FS) bits. Additionally, other frequency options can be configured with the I^2C interface. Using advanced design technology, it provides excellent jitter performance across the entire output frequency range working reliably at supply voltages from 1.8 V to 3.3 V for junction temperatures from –40 °C to 125 °C. This makes it ideally suited for communications applications (for example, OTN, SONET/SDH, xDSL, GbE, Networking, Wireless Infrastructure), test and instrumentation applications, and high-speed data converters. Additionally, the VCXO function enables the use of CY51X7 in applications requiring a clock source with voltage control and in discrete clocking solutions for synchronous timing applications.

The CY51X7 die configuration can be created using ClockWizard 2.1. For programming support, contact Cypress Technical Support or send an email to clocks@cypress.com.

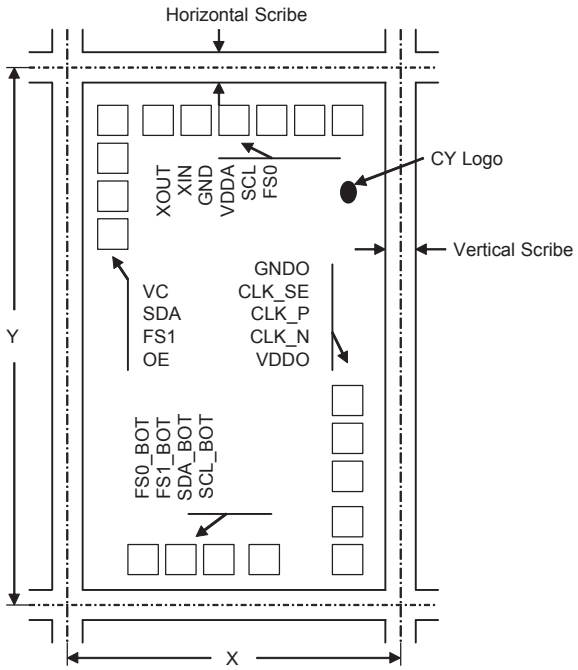
For a complete list of related documentation, click here.

Logic Block Diagram



Contents

Die Pad Description



Note:
Die Size: X = 919.5955 µm
Y = 1399.4 µm
Scribe: Vertical = 79.8955 µm
Horizontal = 80 µm

Die Pad Summary

Pad coordinates are referenced from the seal ring edge (X = 0, Y = 0)

Name	Die Pad	X Coordinate (µm)	Y Coordinate (µm)	Description
VC	1	86.8275	1234.157	VIN for VCXO
SDA	2	86.8275	1133.357	Serial data input/output for I^2C
FS1	3	86.8275	1032.557	Frequency Select input 1 (100 kΩ pull-down)
OE	4	86.8275	931.7565	Output Enable input (configurable 200 kΩ pull-up/ pull-down
FS0_BOT	5	162.063	87.2235	Frequency Select 0 (Alternative) (100 kΩ pull-down)
FS1_BOT	6	262.8765	87.2235	Frequency Select 1 (Alternative) (100 kΩ pull-down)
SDA_BOT	7	363.663	87.2235	Serial data input/output (Alternative)
SCL_BOT	8	464.463	87.2235	Serial clock input for I^2C (Alternative)
V_{DDO}	9	714.627	73.0755	Power supply for output driver
CLK_N	10	714.627	173.8755	Complementary output
CLK_P	11	714.627	305.2755	True output
CLK_SE	12	714.627	393.4755	(Optional) LVCMOS clock output
GNDO	13	714.627	494.2755	Supply Ground for output driver
FS0	14	704.0025	1232.123	Frequency Select input 0 (100 kΩ pull-down)
SCL	15	603.2025	1232.123	Serial clock input for I^2C
V_{DDA}	16	502.4025	1232.123	Power supply for core
GND	17	401.6025	1232.123	Power supply ground
XIN	18	300.8025	1232.123	Crystal reference input
XOUT	19	200.0025	1232.123	Crystal reference output
Note: CLK_SE and (CLK_P, CLK_N) will not be available at the same time. VDDA should equal VDDO.				

Functional Overview

Programmable Features

Table 1. Programmable Features

Feature	Description
Frequency Tuning	Frequency for the PLL
	Oscillator tuning (load capacitance values)
Function	OE polarity
Power Supply	V_{DD} (1.8, 2.5 or 3.3 V)
VCXO	Enable/Disable VCXO
	Kv polarity
	Total pull range
	Modulation bandwidth
Output	LVPECL, LVDS, HCSL, CML, LVCMOS
Function	I^2C address
	4 / 2 / 1 - default frequency
Reference	Crystal (HFF, OT3, LFF) or clock input

Architecture Overview

The CY51X7 is a high-performance programmable PLL die for crystal oscillators supporting multiple functions, multiple output standards, and four user selectable output frequencies. The device has internal one-time programmable (OTP) nonvolatile memory (NVM) that can be partitioned into Common Device Configurations and Frequency Information (see Figure 2). The Common Device Configurations do not change with output frequency and consist of chip power supply, OE polarity, I^2C device address, input reference, output standards, and VCXO. The OTP memory is based on eFuse and the CY51X7 also contains volatile memory (shown as "NVMCopy" in Figure 1) that stores an exact copy of the NVM at the release of reset on Power ON. The chip settings depend on the contents of the volatile memory and the output frequency depends on the configurations, as explained in Figure 1. The volatile memory can be accessed through the I^2C bus and modified.

Figure 1. Conceptual Memory Structure

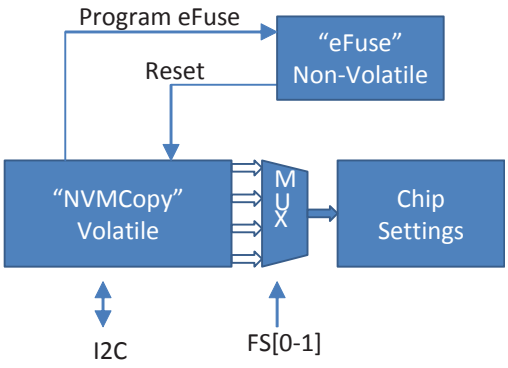
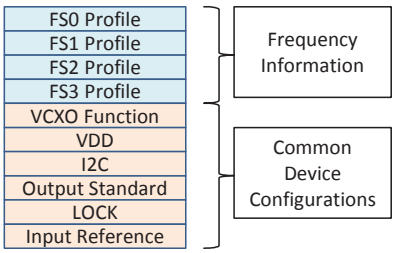


Figure 2 shows the conceptual internal memory structure that consists of Common Device Configurations and Frequency Information.

Figure 2. Memory Structure for Configurations



Description of Settings for the Memory Structure

- Profile[FS0-3]: Frequency information
- VCXO function: VCXO enable/disable, TPR, modulation bandwidth and Kv (Slope for VC vs. Frequency) information
- V_{DD}: 1.8 / 2.5 / 3.3 V range information
- I^2C: enable/disable, I^2C address information
- Output Standards: LVPECL, LVDS, CML, HCSL, LVCMOS
- LOCK pattern: 2-bit pattern to indicate eFuse lock
- Input reference: Crystal (OT3, HFF, LFF) or clock

Internal State Diagram

The CY51X7 contains a state machine, which controls the device behavior. The state machine loads the "eFuse" contents to "NVMCopy" after the reset as indicated in Figure 3 on page 5. The eFuse memory contains a 2-bit pattern "XT-PATTERN" associated with Crystal Blank Tuning.

The state machine enters one of the following states: "Crystal Blank Tuning state", "Command Wait state", or "Active state" according to the XT-PATTERN and/or LOCK. There are two options for the unprogrammed device: one is the XT-PATTERN = "00" or "11" (referred to as non-XT-PAT device hereafter) and the other is XT-PATTERN = "01" or "10" (referred to as XT-PAT device hereafter).

In case of a XT-PAT device, the state machine goes to "Crystal Blank Tuning state" automatically. You may tune the Crystal Blank without shifting any data to the device.

In the case of a non-XT-PAT device, the State Machine goes to "Command Wait state" if the LOCK = "00". In this state, you may access all the registers and read/write the "NVMCopy" contents. The following commands can be used in the "Command Wait state":

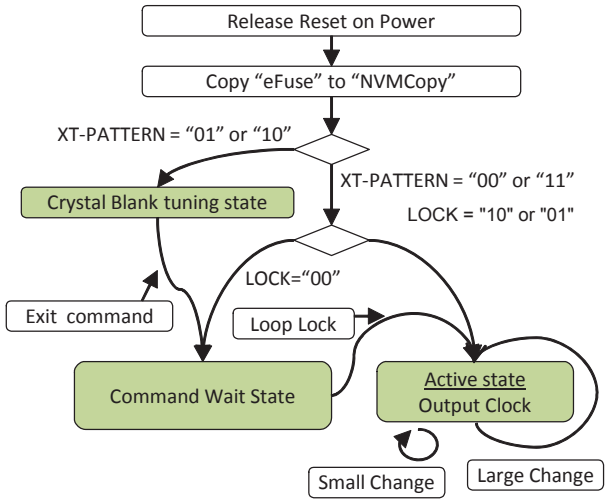
- Program eFuse
  - Selectively Program eFuse
- Copy eFuse to NVMCopy
- Copy NVMCopy to NVMRegister
- Loop Lock
- Exit Command (applicable in the "Crystal Blank tuning state")

You may test the device functionality by issuing the "Loop Lock" command to enter "Active state" without programming the LOCK.

When the LOCK is programmed as “10” or “01”, the device goes to the “Active state” and the output clock will be available after completion of the power-on cycle.

In the “Active state”, you may change the output frequency by applying “Small Change” or “Large Change” commands.

Figure 3. State Diagrams



Small/Large Changes

Small change refers to the case where the frequency is changing within ±500 ppm. The frequency information can be loaded through I^2C and the output frequency will change without any glitch from its original frequency to the new frequency.

Note The small change functionality is not supported in the Integer mode PLL. For more information, see AC Electrical Specifications for LVPECL, LVDS, CML Outputs.

Large change refers to the case where the frequency is changing more than ±500 ppm and is done through an I^2C or FS state change. The device will recalibrate and reconfigure the PLL and the output will be unstable until this process is completed.

Programming Support

The CY51X7 is a software-configurable solution in which Cypress provides a programming specification that defines all necessary configuration bits. The customer uses this information to develop programming software for use with their programmer hardware.

Frequency Configurations

The FS[0-3] setting is done based on the logic levels on the FS0 and FS1 pins as indicated in the Table 2. The frequency configuration consists of the desired output frequency corresponding to each of the FS[0–3] setting. The Fractional-N PLL is loaded with values required to generate the frequency for each of these settings based on the input crystal frequency. The frequency configuration for FS[0–3] is provided in Table 4 on page 6.

Table 2. FS Setting

FS1	FS0	FS Setting
0	0	FS0
0	1	FS1
1	0	FS2
1	1	FS3

Programmable OE Polarity

The CY51X7 contains a bit for OE polarity setting (default is active-low). You can choose active-high or active-low polarity for the OE function. The output will be disabled when OE is deasserted.

Programmable VCXO

The device incorporates a proprietary technique for modulating frequency by modifying VCO frequency according to the VC control voltage. The pull profile is linear and accurate compared to pulling the OT3/HFF reference. Also, the VCXO characteristics are very stable and do not vary over temperature, supply voltage, or process variations.

Kv (slope for frequency versus VC), TPR VC bandwidth, and VCXO on/off are all programmable. Note that the VCXO functionality is not supported in the Integer mode PLL.

Power Supply Sequencing

For start-up, the CY51X7 does not require any specific sequencing and only needs a monotonic V_{DD} ramp specified in the datasheet. After the ramp up, V_{DD} has to be maintained within the limits specified for it in the Recommended Operating Conditions. Brownout detection and protection has to be implemented elsewhere in the system.

Other input signals, such as VC, FS0 or FS1, can power up earlier or later than V_{DD}. There are no timing requirements for those input signals with reference to V_{DD}. The device will operate normally when all of the input signals are settled in the configured state.

If a TCXO or external clock is fed into the XIN/XOUT inputs, a stable input has to be present before start of the V_{DD} ramp-up to the specified level. This is because the on-chip frequency calibration process starts at Power ON and requires a stable reference input to be available at the start of the process.

I^2C Interface

The CY51X7 supports two-wire serial interface and I^2C in Fast Mode (400 kbps) and 7-bit addressing. The device address is programmable and is 55h by default. It supports single-byte access only. The first I^2C access to the device has to be made 5 ms (minimum) after VDD reaches its minimum specified voltage.

Memory Map

Table 3. Common Configurations

Memory Address	Description
50h-57h	Device configurations

Table 4. FSx: Frequency Configurations

Memory Address	Description
10h, 20h, 30h, 40h	DIVO
11h, 21h, 31h, 41h	DIVO, DIVN_INT
12h, 22h, 32h, 42h	ICP,DIVN_INT, PLL_MODE
13h, 23h, 33h, 43h	DIVN_FRAC_L
14h, 24h, 34h, 44h	DIVN_FRAC_M
15h, 25h, 35h, 45h	DIVN_FRAC_H
1xh = FS0, 2xh = FS1, 3xh = FS2, 4xh = FS3	–

Table 5. Miscellaneous Information

Memory Address	Description
00h (Read Only)	Device ID (= 51h)
D4h–D6h	User configurable information

Write all the contents created by the Configuration tool. Partial updates to the device is not allowed.

Access to locations other than those described here may cause fatal error in device operation.

Absolute Maximum Ratings

Exceeding maximum ratings[1] may shorten the useful life of the device. User guidelines are not tested.

Supply voltage to ground potential .....–0.5 V to + 3.8 V
Input voltage .....–0.5 V to + 3.8 V
Storage temperature (non-condensing) ... –55 °C to +150 °C
Junction temperature ..... –40 °C to +125 °C
Programming temperature ..... 0 °C to +125 °C
Programming Voltage .....2.5V ±0.1 V
Supply Current for eFuse Programming ..... 50 mA
Data retention at T_J = 125 °C .....> 10 years
Maximum programming cycles 1
ESD HBM (JEDEC JS-001-2012) ..... 2000 V
ESD MM (JEDEC JESD22-A115B) ..... 200 V
Latch-up current ..... ± 140 mA

Recommended Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}, V_{DDO}	Supply voltage, 1.8-V operating range, 1.8 V ± 5%	1.71	1.89	V
	Supply voltage, 2.5-V operating range, 2.5 V ± 10%	2.25	2.75	V
	Supply voltage, 3.3-V operating range, 3.3 V ± 10%	2.97	3.63	V
f_{RES}	Frequency resolution	–	2	ppb
$T_{PLLHOLD}$	PLL Hold Temperature Range		125	°C

DC Electrical Specifications

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I_{DD}[2]	Supply current[3], LVPECL	V_{DD} = 3.3 V, 2.5 V, 50 Ω to V_{TT} (V_{DDO} – 2.0 V), with common mode current	–	93	106	mA
	Supply current[3], LVPECL	V_{DD} = 3.3 V, 2.5 V, 50 Ω to V_{TT} (V_{DDO} – 2.0 V), without common mode current[4]	–	81	94	
	Supply current[3], LVDS	V_{DD} = 3.3 V, 2.5 V, 1.8 V, 100 Ω between CLKP and CLKN	–	69	81	
	Supply current[3], HCSL	V_{DD} = 3.3 V, 2.5 V, 1.8 V, 33 Ω and 49.9 Ω to GND	–	80	93	
	Supply current[3], CML	V_{DD} = 3.3 V, 2.5 V, 1.8 V, 50 Ω to V_{DDO}	–	73	86	
	Supply current[3], CMOS	V_{DD} = 3.3 V, 2.5 V, 1.8 V, 0 pF load, 33.33 MHz	–	58	70	
	Supply current[3], CMOS	V_{DD} = 3.3 V, 2.5 V, 1.8 V, 10 pF load, 33.33 MHz	–	66	78	
	Supply current, PLL only	V_{DD} = 3.3 V, 2.5 V, 1.8 V	–	59	70	
I_{IH}	Input high current	Logic input, Input = V_{DD}	–	30	50	µA
I_{IL}	Input low current	Logic input, Input = GND	–	30	50	µA
V_{IH}[5]	Input high voltage	OE, FS, SCL, SDA logic level = 1	0.7 × V_{DD}	–	–	V
V_{IL}[5]	Input low voltage	OE, FS, SCL, SDA logic level = 0	–	–	0.3 × V_{DD}	V
V_{IN}	Input voltage level	All input, relative to GND	–0.5	–	3.8	V
R_P	Internal pull-up resistance	OE, configured active High	–	200	–	kΩ
R_D	Internal pull-down resistance	OE, configured active Low	–	200	–	kΩ
		FS0, FS1 pins	–	100	–	kΩ

Notes
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.
2. I_{DD} is the total supply current and is measured with V_{DD} and V_{DDO} shorted together.
3. Maximum current 3 mA lesser with HFF Crystal.
4. In ClockWizard 2.1, setting the output standard to LVPECL2 configures the output to "LVPECL without common mode current". Refer to AN210253 for LVPECL terminations for different use case configurations.
5. I^2C operation applicable for V_{DD} of 1.8 V and 2.5 V only.

DC Specifications for LVDS Output

(V_{DDO} = 1.8 V, 2.5 V, or 3.3 V range)

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OCM}[6]	Output common-mode voltage	V_{DDO} = 2.5-V or 3.3-V range	1.125	1.200	1.375	V
ΔV_{OCM}	Change in V_{OCM} between complementary output states	–	–	–	50	mV
I_{OZ}	Output leakage current	Output off, V_{OUT} = 0.75 V to 1.75V	–20	–	20	µA

DC Specifications for LVPECL Output

(V_{DDO} = 2.5 V or 3.3 V range, with common mode current)

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OH}	Output high voltage	R-term = 50 Ω to V_{TT} (V_{DDO} – 2.0 V)	V_{DDO} – 1.165	–	V_{DDO} – 0.800	V
V_{OL}	Output low voltage	R-term = 50 Ω to V_{TT} (V_{DDO} – 2.0 V)	V_{DDO} – 2.0	–	V_{DDO} – 1.55	V

DC Specifications for CML Output

(V_{DDO} = 1.8 V, 2.5 V, or 3.3 V range)

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OH}	Output high voltage	R-term = 50 Ω to V_{DDO}	V_{DDO} – 0.085	V_{DDO} – 0.01	V_{DDO}	V
V_{OL}	Output low voltage	R-term = 50 Ω to V_{DDO}	V_{DDO} – 0.6	V_{DDO} – 0.4	V_{DDO} – 0.32	V

Note
6. Requires external AC coupling for V_{DDO} = 1.8-V range, as indicated in Figure 8. The common-mode voltage of 1.2V has to be generated and applied externally.

DC Specifications for HCSL Output

(V_{DDO} = 1.8 V, 2.5 V, or 3.3 V range)

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{MAX}[7]	Max output high voltage	Measurement taken from single-ended waveform	–	–	1150	mV
V_{MIN}[7]	Min output low voltage	Measurement taken from single-ended waveform	–300	–	–	mV
V_{OHDIFF}	Differential output high voltage	Measurement taken from differential waveform	150	–	–	mV
V_{OLDIFF}	Differential output low voltage	Measurement taken from differential waveform	–	–	–150	mV
V_{CROSS}[7]	Absolute crossing point voltage	Measurement taken from single-ended waveform	250	–	600	mV
$V_{CROSSDELTA}$[7]	Variation of V_{CROSS} over all rising clock edges	Measurement taken from single-ended waveform	–	–	140	mV

DC Specifications for LVCMOS Output

Parameter[7]	Description	Condition	Min	Typ	Max	Units
V_{OH}	Output high voltage	100-µA load	V_{DDO} – 0.2	–	–	V
		4-mA load, V_{DD} = 1.8 V and 2.5 V	V_{DDO} – 0.4	–	–	
		4-mA load, V_{DD} = 3.3 V	V_{DDO} – 0.3	–	–	
V_{OL}	Output low voltage	100-µA load	–	–	0.2	V
		4-mA load	–	–	0.3	

V_{CXO} Specific Parameters

Parameter[7]	Description	Condition	Min	Typ	Max	Units
TPR	Total pull range	VC range 0.1 × V_{DD} to 0.9 × V_{DD}	± 50	–	± 275	ppm
K_{BSL}	Best-fit straight line (BSL) linearity	Deviation from BSL line	–5	–	5	%
K_{INC}	Incremental linearity	Kv slope deviation	–10	–	10	%
K_{BW}	Bandwidth of Kv modulation	Programmable	5	10	20	kHz
K_{RANGE}	voltage range on the control port permissible	–	0	–	V_{DD}	V
V_{CTYP}	Nominal center VC control voltage	V_{DD} configuration = 1.8 V	–	0.9	–	V
		V_{DD} configuration = 2.5 V	–	1.25	–	V
		V_{DD} configuration = 3.3 V	–	1.65	–	V
R_{VCIN}[8]	Input resistance for VC	–	5	–	–	MΩ
V_{RANGE}	Input voltage range	Range of input possible at control port	0.1 × V_{DD}	–	0.9 × V_{DD}	V

Notes
7. Parameters are guaranteed by design and characterization. Not 100% tested in production.
8. R_{VCIN} is 100% tested.

AC Electrical Specifications for LVPECL, LVDS, CML Outputs

(V_{DD} = 3.3 V and 2.5 V for LVPECL, with common mode current, and V_{DD} = 3.3 V, 2.5 V, and 1.8 V for LVDS and CML outputs)

Parameter[9]	Description	Details/Conditions	Min	Typ	Max	Unit
f_{OUT}	Clock Output Frequency	LVPECL, CML, LVDS output standards	15	–	2100	MHz
t_{RF}	LVPECL Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for PECL outputs.	–	–	350	ps
	CML Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for CML outputs.	–	–	350	ps
	LVDS Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for LVDS outputs.	–	–	350	ps
t_{ODC}	Output Duty Cycle	Measured at differential 50% level, 156.25 MHz.	45	50	55	%
V_P	LVDS output differential peak	15 MHz to 700 MHz	247	–	454	mV
V_P	LVDS output differential peak	700 MHz to 2100 MHz	150	–	454	mV
ΔV_P	Change in VP between complementary output states	–	–	–	50	mV
V_P	LVPECL output differential peak	f_{OUT} = 15 MHz to 325 MHz	450	–	–	mV
V_P		f_{OUT} = 325 MHz to 700 MHz	350	–	–	mV
V_P		f_{OUT} = 700 MHz to 2100 MHz	250	–	–	mv
V_P	CML output differential peak	f_{OUT} = 15 MHz to 700 MHz	250	–	600	mV
V_P	CML output differential peak	f_{OUT} = 700 MHz to 2100 MHz	200	–	600	mV
t_{CCJ}	Cycle to Cycle Jitter	pk, measured at differential signal, 156.25 MHz, over 10k cycles, 100 MHz–130 MHz crystal	–	–	50	ps
t_{PJ}	Period Jitter	pk-pk, measured at differential signal, 156.25 MHz, over 10k cycles, 100 MHz–130 MHz crystal	–	–	50	ps
J_{RMS}	RMS Phase Jitter	f_{OUT} = 156.25 MHz, 12 kHz–20 MHz offset, non-VCXO mode	–	150	250	fs
Non-VCXO Mode						
PN1k	Phase Noise, 1 kHz Offset	100-130 MHz crystal reference, f_{OUT} = 156.25 MHz	–	–	-113	dBc/Hz
PN10k	Phase Noise, 10 kHz Offset	100-130 MHz crystal reference, f_{OUT} = 156.25 MHz	–	–	-127	dBc/Hz
PN100k	Phase Noise, 100 kHz Offset	100-130 MHz crystal reference, f_{OUT} = 156.25 MHz	–	–	-135	dBc/Hz
PN1M	Phase Noise, 1MHz Offset	100-130 MHz crystal reference, f_{OUT} = 156.25 MHz	–	–	-144	dBc/Hz
PN10M	Phase Noise, 10 MHz Offset	100-130MHz crystal reference, f_{OUT} = 156.25 MHz	–	–	–152	dBc/Hz
PN-SPUR	Spur	At frequency offsets equal to and greater than the update rate of the PLL	–	–	–65	dBc/Hz

Note
9. Parameters are guaranteed by design and characterization. Not 100% tested in production.

AC Electrical Specifications for HCSL Output

Parameter[10]	Description	Test Conditions	Min	Typ	Max	Units
f_{OUT}	Output frequency	HCSL	15	–	700	MHz
E_R	Rising edge rate	Measured taken from differential waveform, –150 mV to +150 mV	0.6	–	5.7 [11]	V/ns
E_F	Falling edge rate	Measured taken from differential waveform, –150 mV to +150 mV	0.6	–	5.7 [11]	V/ns
t_{STABLE}	Time before voltage ring back (VRB) is allowed	Measured taken from differential waveform, –150 mV to +150 mV	500	–	–	ps
R-F_MATCHING	Rise-Fall matching	Measured taken from single-ended waveform, rising edge rate to falling edge rate matching, 100 MHz	–100	–	100	ps
t_{DC}	Output duty cycle	Measured taken from differential waveform, f_{OUT} = 100 MHz	45	–	55	%
t_{CCJ}	Cycle to cycle Jitter	Measured taken from differential waveform, 100 MHz	–	–	50	ps
$J_{RMSPCIE}$	Random jitter, PCIE Specification 3.0	100 MHz–130 MHz crystal	–	–	1	ps (RMS)

AC Electrical Specifications for LVCMOS Output

(Load: 10 pF < 100 MHz, 7.5 pF < 150 MHz, 5 pF > 150 MHz)

Parameter[10]	Description	Test Conditions	Min	Typ	Max	Unit
f_{OUT}	Output frequency		15	–	250	MHz
t_{DC}	Output duty cycle	Measured at 1/2 V_{DDO}, loaded, f_{OUT} < 100 MHz	45	–	55	%
		Measured at 1/2 V_{DDO}, loaded, f_{OUT} > 100 MHz	40	–	60	%
t_{RFCMOS}	Rise/Fall time	V_{DDO} = 1.8 V, 20%–80%	–	–	2	ns
		V_{DDO} = 2.5 V, 20%–80%	–	–	1.5	ns
		V_{DDO} = 3.3 V, 20%–80%	–	–	1.2	ns
t_{CCJ}	Cycle to cycle Jitter	pk, Measured at 1/2V_{DDO} over 10k cycle, f_{OUT} = 156.25 MHz	–	–	50	ps
t_{PJ}	Period Jitter	pk, Measured at 1/2V_{DDO} over 10k cycle, f_{OUT} = 156.25 MHz	–	–	100	ps

Notes
10. Parameters are guaranteed by design and characterization. Not 100% tested in production.
11. Edge rates are higher than 4 V/ns due to jitter performance requirements.

HFF Crystal Specifications

Parameter[12]	Description	Test Conditions	Min	Typ	Max	Unit
f_{XTAL}	Crystal frequency range	–	100	–	130	MHz
C0	Crystal shunt capacitance	–	–	–	2	pF
CL	Crystal load capacitance	–	–	5	–	pF
ESR	Crystal equivalent series resistance	ESR = Rm (1 + C0/CL) ^ 2 Rm = Crystal motional resistance	–	20	–	Ω
DL	Drive level	–	–	–	200	µW

OT3 Crystal Specifications

Parameter[12]	Description	Test Conditions	Min	Typ	Max	Units
f_{XTAL}	Crystal frequency range	–	100	–	130	MHz
C0	Crystal shunt capacitance	–	–	–	2	pF
CL	Crystal load capacitance	–	–	5		pF
ESR	Crystal equivalent series resistance	ESR = Rm (1 + C0/CL) ^ 2 Rm = Crystal motional resistance	–	60	90	Ω
DL	Drive level	–	–	–	200	µW

LFF Crystal Specifications

Parameter[12]	Description	Test Conditions	Min	Typ	Max	Units
f_{XTAL}	Crystal frequency range	–	50	–	60	MHz
C0	Crystal shunt capacitance	–	–	–	2	pF
CL	Crystal load capacitance	–	–	–	8	pF
ESR	Crystal equivalent series resistance	ESR = Rm (1 + C0/CL) ^ 2 Rm = Crystal motional resistance	–	–	90	W
DL	Drive level	–	–	–	200	µW

LF Low Frequency Reference

(TCXO reference input)

Parameter[12]	Description	Test Conditions	Min	Typ	Max	Units
f_{IN}	Input frequency	–	50	–	60	MHz
t_{DC}	Input duty cycle	Measured at 1/2 input swing	40	–	60	%
V_{PP}	pk-pk input swing	AC coupled input	0.8	–	1.2	V
V_{IL}	Input low voltage	DC coupled input	–	–	0.2	V
V_{IH}	Input high voltage	DC coupled input	0.8	–	1.2	V
t_R	Input rise time	20%–80% of input	–	–	1.5	ns
t_F	Input fall time	20%–80% of input	–	–	1.5	ns
PN_{10K}	Input phase noise	10-kHz offset	–	–	–151	dBc/Hz
PN_{100K}	Input phase noise	100-kHz offset	–	–	–155	dBc/Hz
PN_{1M}	Input phase noise	1-MHz offset	–	–	–156	dBc/Hz

Note
12. Parameters are guaranteed by design and characterization. Not 100% tested in production.

Timing Parameters

Parameter[13]	Description	Min	Max	Unit
t_{PU}	Supply ramp time (0.5 V to $V_{DD(min)}$).	0.01	3000	ms
t_{WAKEUP}[14]	Time from minimum specified power supply to <± 0.1 ppm accurate output frequency clock, programmable (Clock stable within 2.2 ms (max) from V_{DDX} Level, refer to Input Clock Measurement Point)	–	10	ms
	Time from minimum specified power supply to <± 0.1 ppm accurate output frequency clock, programmable (Clock stable within 5.8 ms (max) from V_{DDX} Level, refer to Input Clock Measurement Point)	–	15	
t_{OEEN}	Time from OE edge to output enable	–	2.5	ms
t_{OEDIS}	Time for OE edge to output disable	–	10	µs
t_{FS}	Time form FS change to new frequency	–	2.5	ms
t_{FSAMLL}	Frequency change time for small trigger (≤ ±500 ppm)	–	400	µs
t_{FLARGE}	Frequency change time for large trigger (> ±500 ppm)	–	2.5	ms
t_{CLOCK}	Clock stable time delay from V_{DD} ramp (see Figure 5), normal configuration	–	2.2	ms
	Clock stable time delay from V_{DD} ramp (see Figure 5), delay programmed	–	5.8	

Input Clock Measurement Point

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{DDX}[13, 14]	t_{CLOCK} Measurement Point	Supply voltage 1.8 V	1.4	–	–	V
		Supply voltage 2.5 V	1.8	–	–	
		Supply voltage 3.3 V	2.3	–	–	

Notes
13. Parameters are guaranteed by design and characterization. Not 100% tested in production.
14. Applies to TCXO/External Clock Input.

Phase Jitter Characteristics

(12 kHz to 20 MHz Integration Bandwidth)

Parameter[15]	Description	Condition	Min	Typ	Max	Units
Non VCXO functionality						
J_{RMS}	RMS jitter	f_{OUT} = 644.53 MHz	–	110	–	fs
J_{RMS}	RMS jitter	f_{OUT} = 622.08 MHz	–	120	–	fs
J_{RMS}	RMS jitter	f_{OUT} = 156.25 MHz	–	145	–	fs
J_{RMS}	RMS jitter	f_{OUT} = 2.105 GHz	–	145	–	fs
Modulation bandwidth = 10 kHz, V_{DD} = 3.3 V, f_{OUT} = 622.08 MHz						
J_{RMS}	RMS jitter	T_{PR} = 50 ppm, Kv = 37.9 ppm/V	–	151	–	fs
J_{RMS}	RMS jitter	T_{PR} = 155 ppm, Kv = 117.4 ppm/V	–	158	–	fs
J_{RMS}	RMS jitter	T_{PR} = 275 ppm, Kv = 208.3 ppm/V	–	170	–	fs
Modulation bandwidth = 10 kHz, V_{DD} = 2.5 V, f_{OUT} = 622.08 MHz						
J_{RMS}	RMS jitter	T_{PR} = 50 ppm, Kv = 50 ppm/V	–	152	–	fs
J_{RMS}	RMS jitter	T_{PR} = 155 ppm, Kv = 155 ppm/V	–	160	–	fs
J_{RMS}	RMS jitter	T_{PR} = 275 ppm, Kv = 275 ppm/V	–	175	–	fs
Modulation bandwidth = 10 kHz, V_{DD} = 1.8 V, f_{OUT} = 622.08 MHz						
J_{RMS}	RMS jitter	T_{PR} = 50 ppm, Kv = 69.4 ppm/V	–	153	–	fs
J_{RMS}	RMS jitter	T_{PR} = 155 ppm, Kv = 215.3 ppm/V	–	166	–	fs
J_{RMS}	RMS jitter	T_{PR} = 275 ppm, Kv = 381.9 ppm/V	–	190	–	fs

I^2C Bus Timing Specifications

Parameter[15, 16]	Description	Min	Typ	Max	Units
f_{SCL}	SCL clock frequency	–	–	400	kHz
$t_{HD:STA}$	Hold time START condition	0.6	–	–	µs
t_{LOW}	Low period of SCL	1.3	–	–	µs
t_{HIGH}	High period of SCL	0.6	–	–	µs
$t_{SU:STA}$	Setup time for a repeated START condition	0.6	–	–	µs
$t_{HD:DAT}$	Data hold time	0	–	–	µs
$t_{SU:DAT}$	Data setup time	100	–	–	ns
t_R	Rise time	–	–	300	ns
t_F	Fall time	–	–	300	ns
$t_{SU:STO}$	Setup time for STOP condition	0.6	–	–	µs
t_{BUF}	Bus-free time between STOP and START conditions	1.3	–	–	µs

Notes
15. Parameters are guaranteed by design and characterization. Not 100% tested in production.
16. I^2C operation applicable for V_{DD} of 1.8 V and 2.5 V only.

Voltage and Timing Definitions

Figure 4. Differential Output Definitions

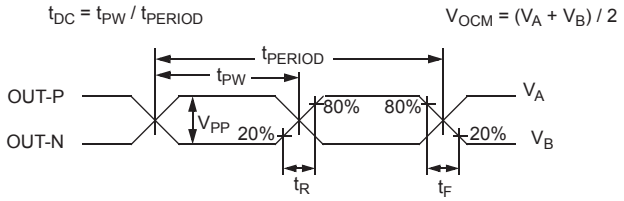


Figure 5. Input Clock Stable Time

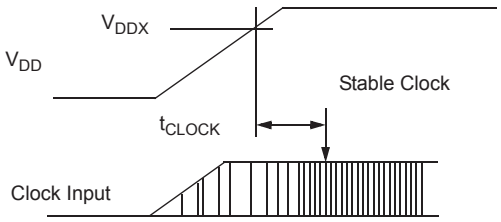


Figure 6. Output Enable/Disable/Frequency Select Timing

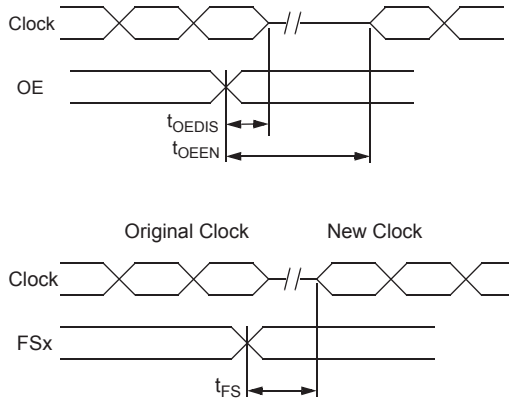


Figure 7. Power Ramp and PLL Lock Time

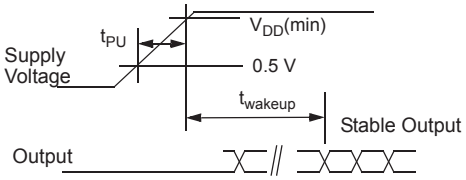


Figure 8. Output Termination Circuit

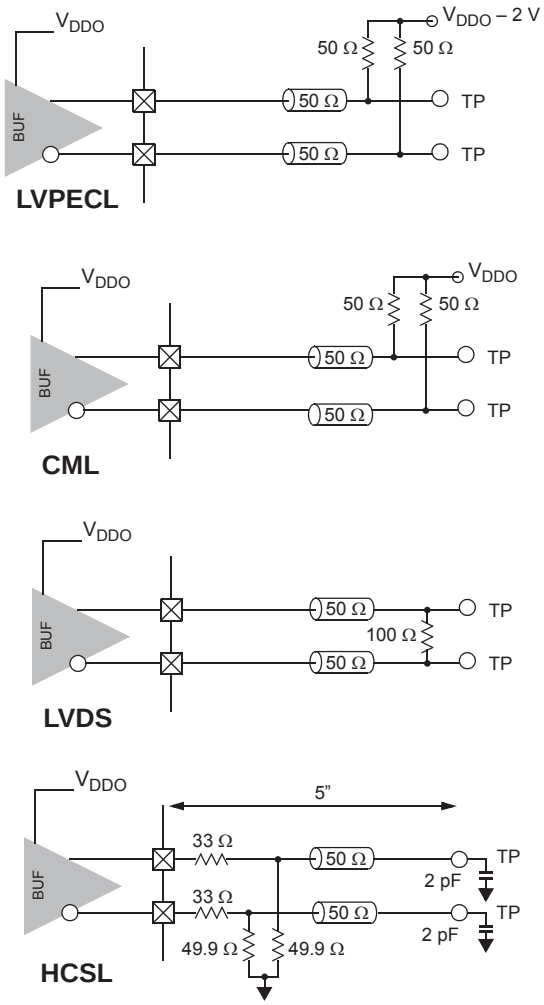
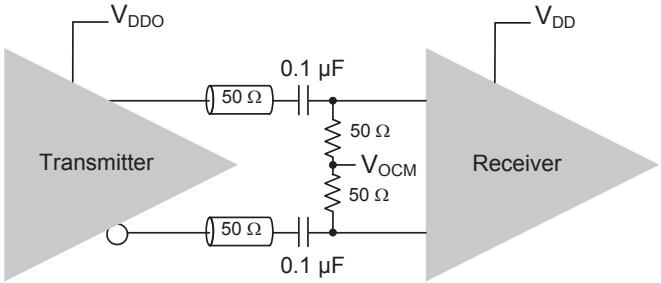


Figure 9. LVDS Termination for 1.8 V [17]



Note

17. The termination circuit shown in this figure is specific to the LVDS output standard for V_{DD} =1.8-V operation. This needs AC coupling (100-nF series capacitor). The 50-ohm termination resistors along with the bias voltage (V_{OCM}) is required to be set at the destination circuit as shown in the figure.

Figure 10. HCSL: Single-ended Measurement Points for Absolute Crossing Point

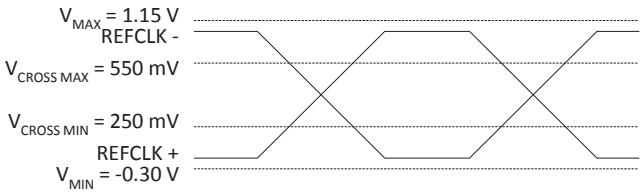


Figure 11. HCSL: Single-ended Measurement Points for Delta Crossing Point

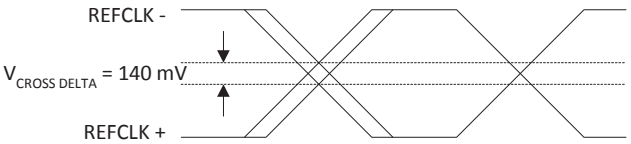


Figure 12. HCSL: Differential Measurement Points for Rise and Fall Time

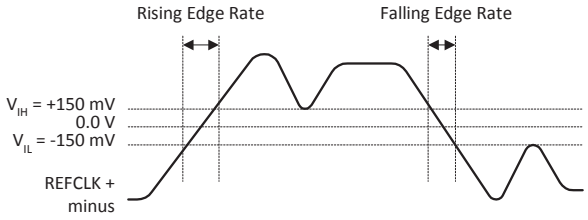


Figure 13. HCSL: Differential Measurement Points for Ringback

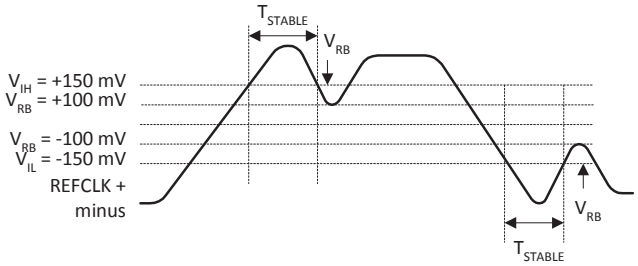
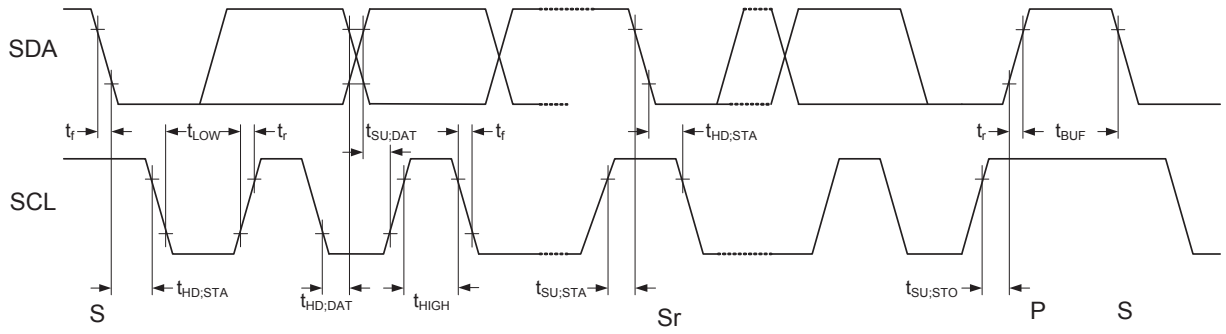


Figure 14. I²C Bus Timing Specifications



Phase Noise Plots

Figure 15. Typical Phase Noise at 156.25 MHz (12 kHz–20 MHz)

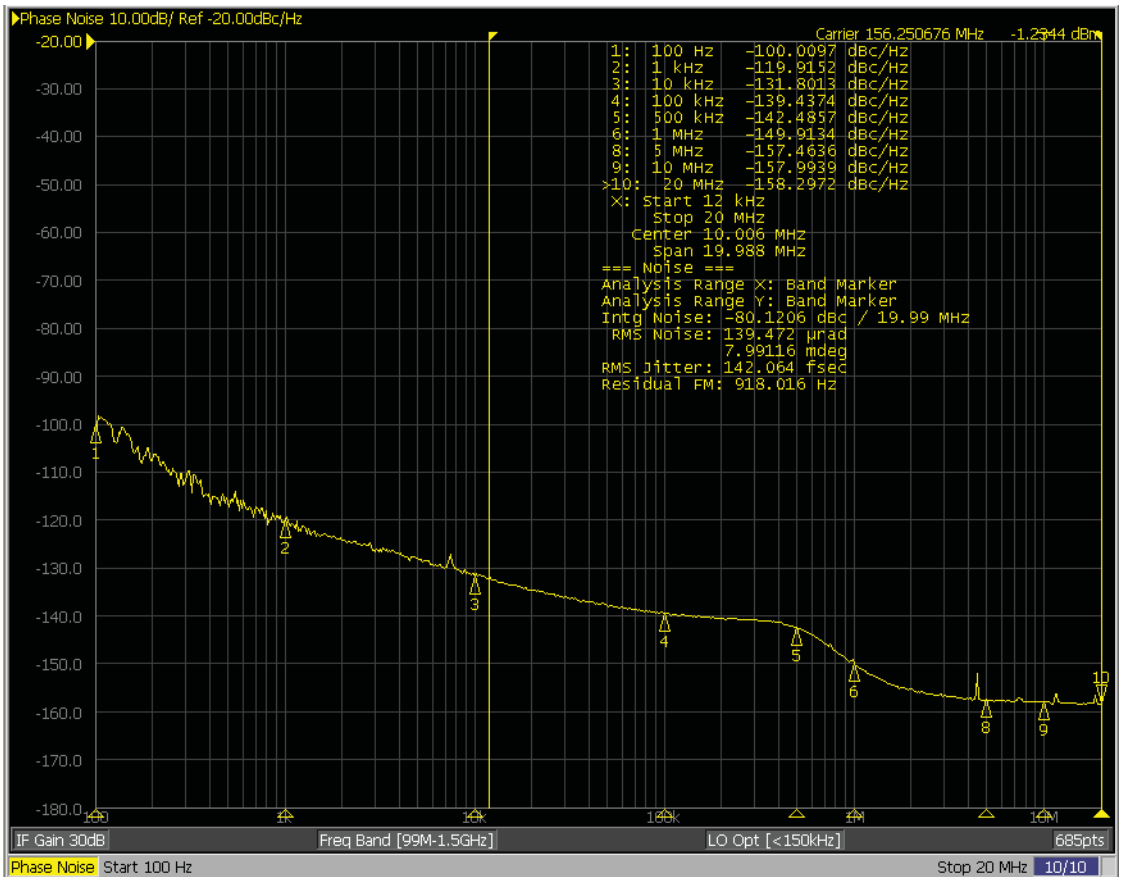


Figure 16. Typical Phase Noise at 622.08 MHz (12 kHz–20 MHz)

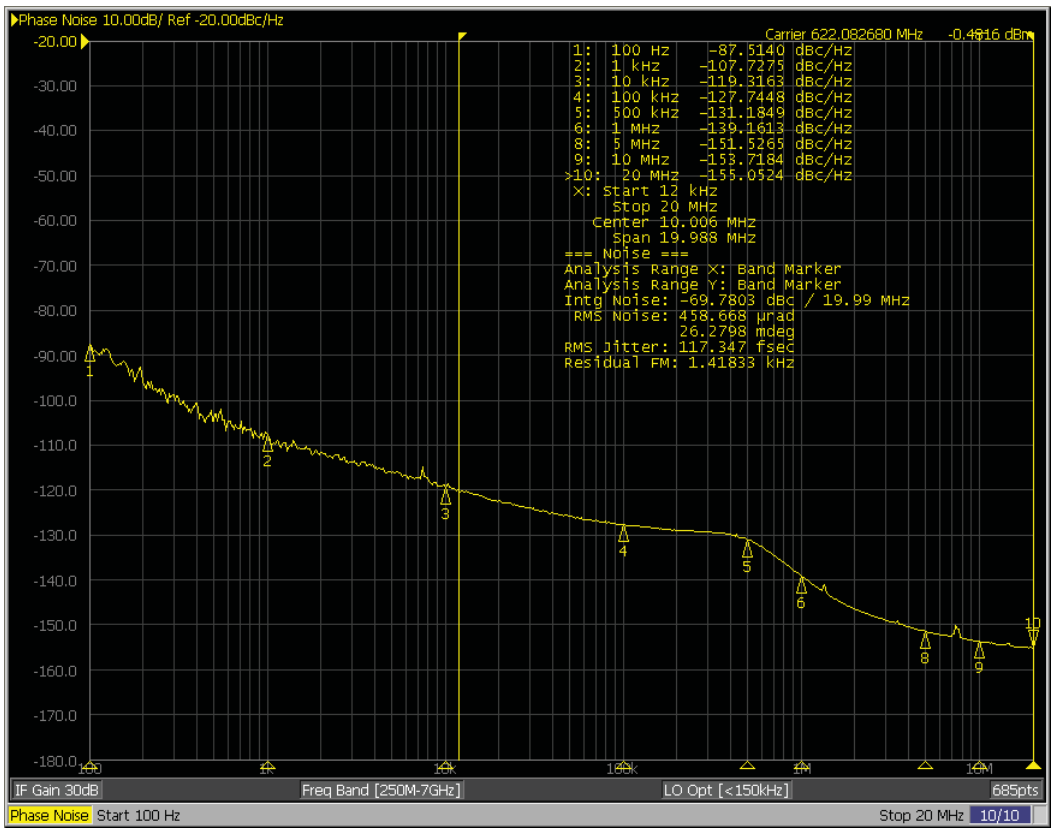
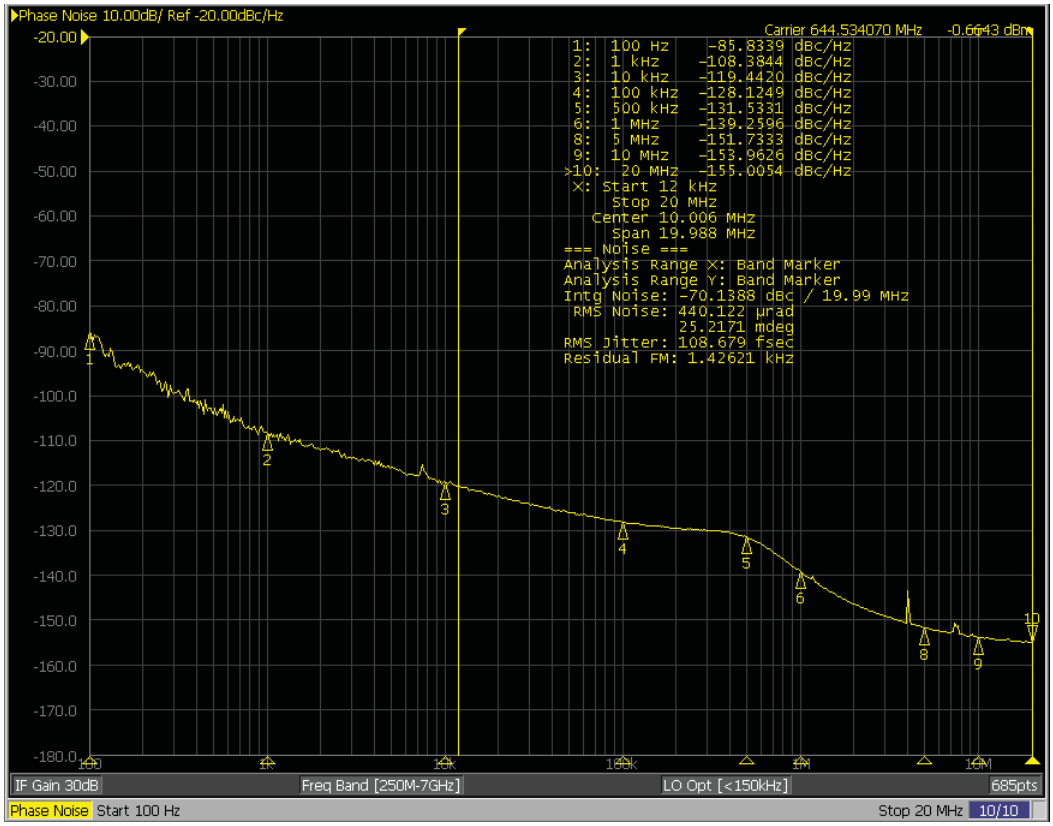


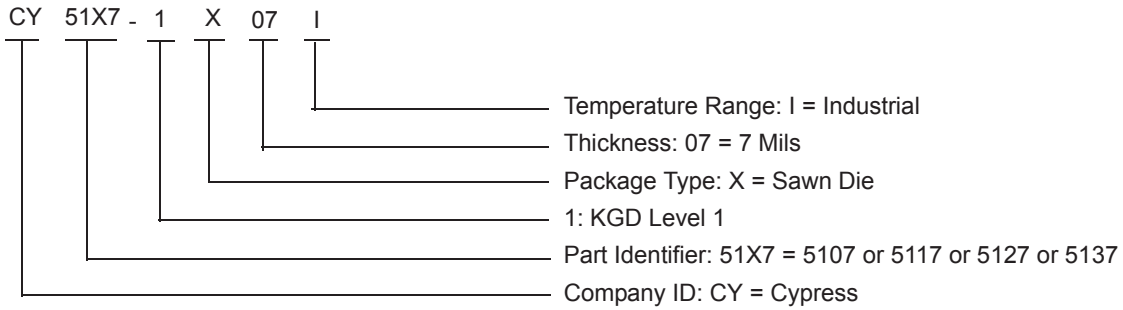
Figure 17. Typical Phase Noise at 644.53 MHz (12 kHz–20 MHz)



Ordering Information

Ordering Code	Type	Junction Temperature
CY5107-1X07I[18]	OT3 crystal input (frequency range of 114 MHz to 130 MHz) and differential output	–40 °C to +125 °C
CY5117-1X07I[19]	OT3 crystal input (frequency range of 114 MHz to 130 MHz) and single-ended output	–40 °C to +125 °C
CY5127-1X07I[18]	HFF crystal input (frequency range of 114 MHz to 130 MHz) and differential output	–40 °C to +125 °C
CY5137-1X07I[20]	Blank Die	–40 °C to +125 °C

Ordering Code Definitions

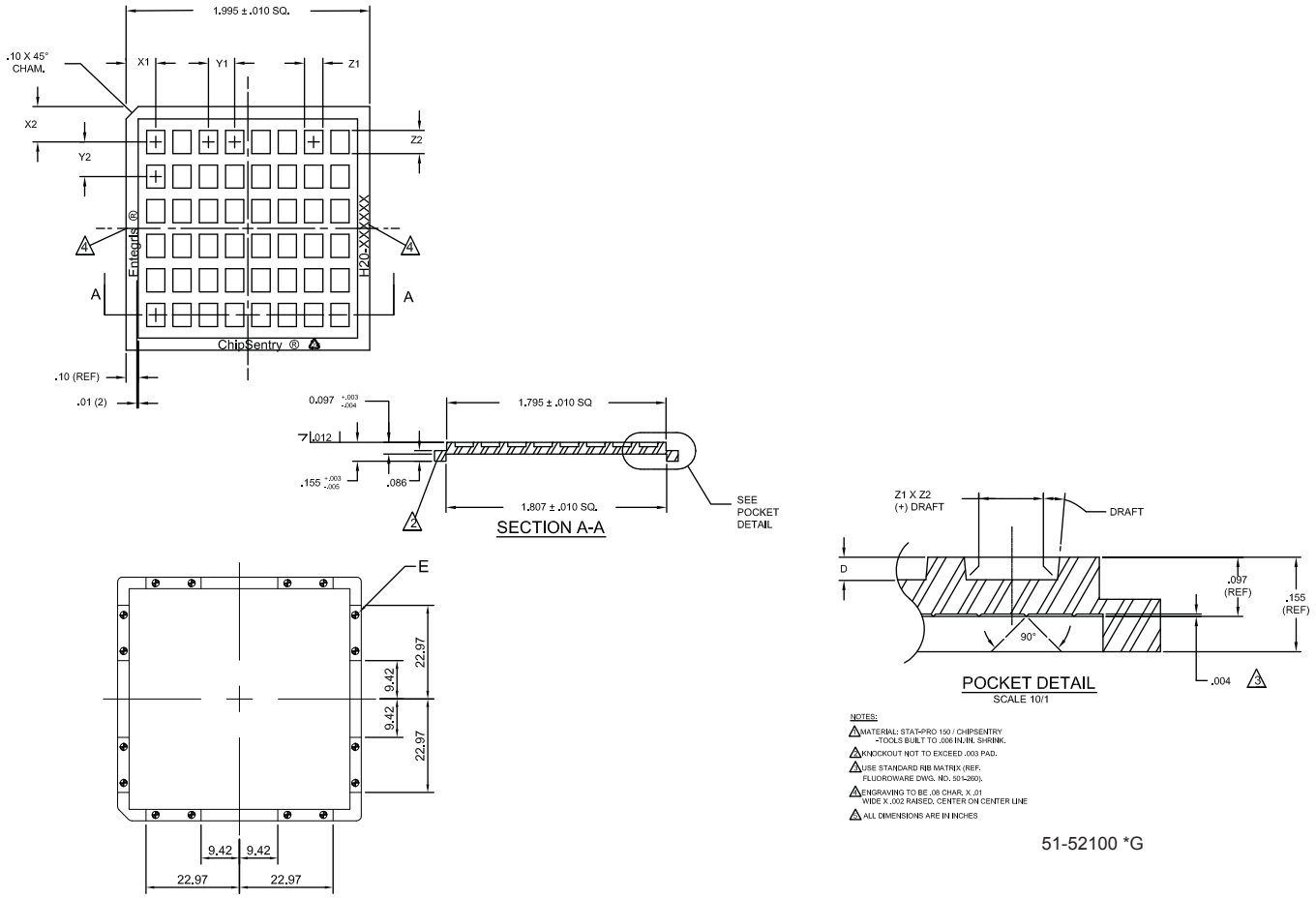


Notes

18. These dies are programmed to support the specified crystal input (either OT3 or HFF) and LVDS differential output type. The output standard can be changed to any other differential standard (LVPECL/CML/HCSL) or single-ended (LVCMOS) through software program.
19. These dies are programmed to support the OT3 single-ended (LVCMOS) output type. The crystal type and output standard cannot be changed through software program.
20. These dies are un-programmed and will not give any output until programmed. Contact the Cypress Technical team for programming support.

Packaging Information

Figure 18. Waffle Tray Drawing



Part No. H20-	X1 ±.005	X2 ±.005	Y1 ±.005	Y2 ±.005	Z1 ±.005	Z2 ±.005	D ±.005	DRAFT	No. per Row	No. per Tray	CY Part No.
N629507	0.170	0.164	.087	.093	.040	.060	.022	5°	20 × 19	380	155000100019

Acronyms

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
BSL	best-fit straight line
CML	current mode logic
DC	direct current
ESD	electrostatic discharge
FS	frequency select
HCSL	high-speed current steering logic
I^2C	inter-integrated circuit
JEDEC	Joint Electron Device Engineering Council
LDO	low dropout (regulator)
LVCMOS	low voltage complementary metal oxide semiconductor
LVDS	low-voltage differential signals
LVPECL	low-voltage positive emitter-coupled logic
NV	non-volatile
OE	output enable
PLL	phase-locked loop
POR	power-on reset
PSoC®	Programmable System-on-Chip
QFN	quad flat no-lead
RMS	root mean square
SCL	serial I^2C clock
SDA	serial I^2C data
VRB	voltage ring back
VCXO	voltage controlled crystal oscillator
XTAL	crystal

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	Degrees Celsius
fs	femtoseconds
GHz	gigahertz
kΩ	kilohms
kHz	kilohertz
MHz	megahertz
MΩ	megaohms
µA	microamperes
µm	micrometers
µs	microseconds
µW	microwatts
mA	milliamperes
mm	millimeters
mΩ	milliohms
ms	milliseconds
mV	millivolts
nH	nanohenry
ns	nanoseconds
Ω	ohms
ppm	parts per million
ppb	parts per billion
%	percent
pF	picofarads
ps	picoseconds
V	volts

Document History Page

Document Title: CY51X7, High-Performance PLL Die for Oscillators Document Number: 001-90233				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
*E	5320399	07/18/2016	MGPL	Changed status from Preliminary to Final.
*F	5429121	09/07/2016	MGPL	Updated Document Title as “CY51X7, High-Performance PLL Die for Oscillators”. Updated Absolute Maximum Ratings: Added “Supply Current for eFuse Programming”. Replaced “≥ 2000 V” with “2000 V” in value corresponding to “ESD HBM”. Replaced “> 200 V” with “200 V” in value corresponding to “ESD MM”. Updated Ordering Information: Updated part numbers. Updated Ordering Code Definitions. Updated to new template.
*G	5518357	11/15/2016	MGPL / PSR	Updated Functional Overview: Updated Frequency Configurations: Added Table 2. Updated DC Electrical Specifications: Removed Note “Parameters are guaranteed by design and characterization. Not 100% tested in production.” and its reference. Updated details in “Test Conditions” column corresponding to I_{DD} parameter. Updated DC Specifications for HCSL Output: Referred Note 7 in V_{MAX}, V_{MIN}, V_{CROSS} and $V_{CROSSDELTA}$ parameters. Updated VCXO Specific Parameters: Added Note 8 and referred the same note in “R_{VCIN}” parameter. Updated AC Electrical Specifications for LVCMOS Output: Referred Note 10 in “Parameter” column. Updated HFF Crystal Specifications: Added Note 12 and referred the same note in “Parameter” column. Updated OT3 Crystal Specifications: Referred Note 12 in “Parameter” column. Updated LFF Crystal Specifications: Referred Note 12 in “Parameter” column. Updated LF Low Frequency Reference: Referred Note 12 in “Parameter” column. Updated Phase Jitter Characteristics: Added Note 15 and referred the same note in “Parameter” column. Updated I2C Bus Timing Specifications: Referred Note 12 in “Parameter” column. Updated Voltage and Timing Definitions: Added Figure 9. Added Note 17 and referred the same note in Figure 9. Updated Ordering Information: Updated part numbers. Updated Note 18. Added Note 19 and referred the same note in “CY5117-1X07I”. Added Packaging Information. Updated to new template.
*H	5537710	11/30/2016	TAVA	Updated Ordering Code Definitions under Ordering Information.
*I	5613574	02/03/2017	PSR	Added links to ClockWizard 2.1 and technical support, and added reference to related documentation in Functional Description. Updated LVPECL specs in DC Electrical Specifications. Added note clarifying voltage range in AC Electrical Specifications for LVPECL, LVDS, CML Outputs. Updated Ordering Information.

Document History Page (continued)

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Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
*J	5682054	04/03/2017	PSR	Updated the template. Replaced the Waffle tray diagram with the Cypress drawing 51-52100. Added Clock Tree Services to Sales, Solutions, and Legal Information.
*K	5755392	06/01/2017	PSR	Updated Cypress logo and Sales information. Updated VCXO Specific Parameters. Updated Figure 18 (spec 51-52100 *F to *G) in Packaging Information.

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