

# Dual 25A or Single 50A μModule Regulator with 0.8% DC and 3% Transient Accuracy

## FEATURES

- **±0.8% Maximum Total DC Output Error Over Line and Load (LTM4650-1A)**
- **±3% Transient Output Error with Minimum Output Capacitance**
- Dual 25A or Single 50A Output
- 4.5V to 15V Input, 0.6V to 1.8V Output Voltage Range
- Differential Remote Sense Amplifier
- Current Mode Control/Fast Transient Response
- Current Sharing Up to 300A
- 16mm × 16mm × 5.01mm BGA Package

## APPLICATIONS

- FPGA, ASIC, μProcessor Core Voltage Regulation
- Information, Communication Systems

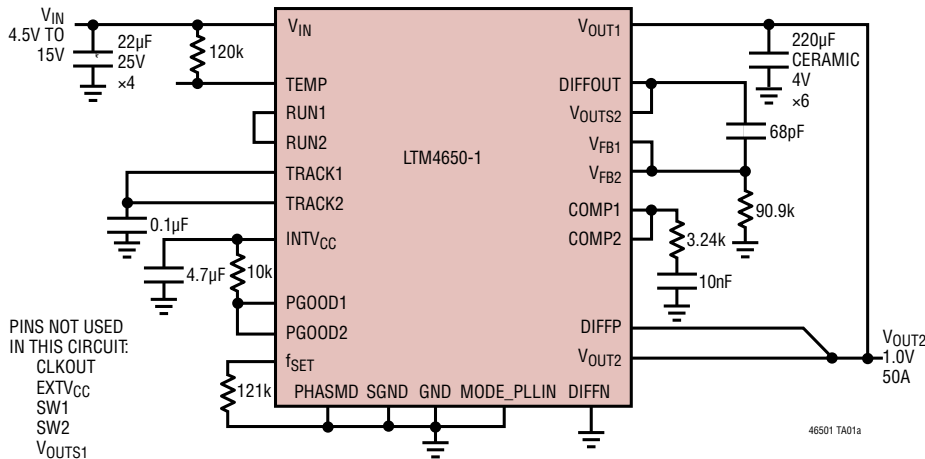
## DESCRIPTION

The **LTM®4650-1A/LTM4650-1B** is dual 25A or single 50A output step-down μModule® (power module) regulator with ±0.8% (LTM4650-1A) and ±1.5% (LTM4650-1B) total DC output error with ±3% transient output error. Included in the package are the switching controller, power FETs, inductors, and all supporting components. External compensation allows for fast transient response to minimize output capacitance when powering FPGAs, ASICs, and processors. With synchronized multiphase parallel current sharing, six LTM4650-1 devices can deliver up to 300A. The LTM4650-1 is offered in a 16mm × 16mm × 5.01mm BGA package, with SnPb (BGA) or RoHS compliant terminal finish.

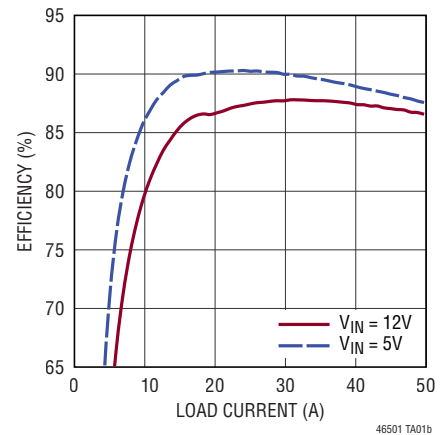
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## TYPICAL APPLICATION

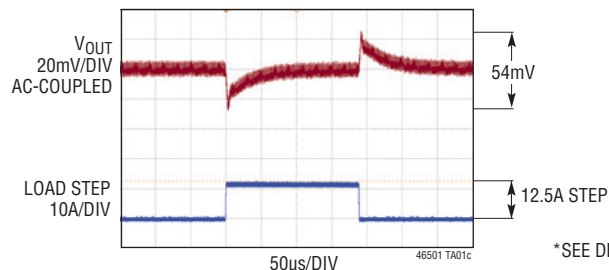
**50A, 1.0V Output DC/DC μModule Regulator**



**1.0V Output Efficiency,  $f_{SW} = 500kHz$**



**25% Load Step Transient Response, ±3% Output Regulation Window. 12VIN, 1.0VOUT, 50A with 6x 220μF Ceramic Cap**



\*SEE DEMO CIRCUIT DC2479A-B

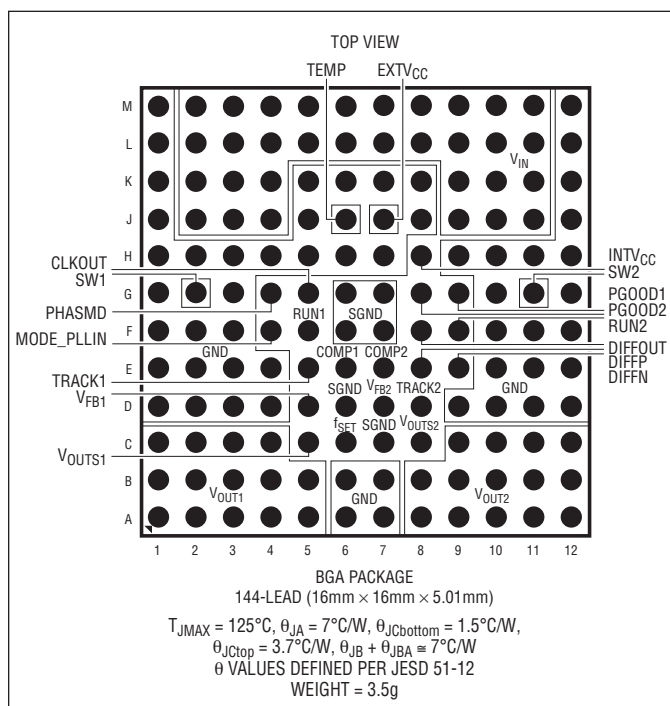
# LTM4650-1

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{IN}$	–0.3V to 16V
$V_{SW1}$ , $V_{SW2}$	–1V to 16V
PGOOD1, PGOOD2, RUN1, RUN2,	
INTV <sub>CC</sub> , EXTV <sub>CC</sub>	–0.3V to 6V
MODE_PLLIN, $f_{SET}$ , TRACK1, TRACK2,	
DIFFOUT, PHASMD	–0.3V to INTV <sub>CC</sub>
$V_{OUT1}$ , $V_{OUT2}$ , $V_{OUTS1}$ , $V_{OUTS2}$ (Note 6)	–0.3V to 6V
DIFFP, DIFFN	–0.3V to INTV <sub>CC</sub>
INTV <sub>CC</sub> Peak Output Current	100mA
Internal Operating Temperature Range	
(Note 2)	–40°C to 125°C
Storage Temperature Range	–55°C to 125°C
Peak Package Body Temperature	245°C

## PIN CONFIGURATION



## ORDER INFORMATION

<http://www.linear.com/product/LTM4650-1#orderinfo>

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TOTAL DC ACCURACY	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE				
LTM4650EY-1A#PBF	SAC305 (RoHS)	LTM4650Y-1	e1	BGA	3	±0.8%	–40°C to 125°C
LTM4650IY-1A#PBF	SAC305 (RoHS)	LTM4650Y-1	e1	BGA	3	±0.8%	–40°C to 125°C
LTM4650EY-1B#PBF	SAC305 (RoHS)	LTM4650Y-1	e1	BGA	3	±1.5%	–40°C to 125°C
LTM4650IY-1B#PBF	SAC305 (RoHS)	LTM4650Y-1	e1	BGA	3	±1.5%	–40°C to 125°C
LTM4650IY-1A	SnPb (63/37)	LTM4650Y-1	e0	BGA	3	±0.8%	–40°C to 125°C
LTM4650IY-1B	SnPb (63/37)	LTM4650Y-1	e0	BGA	3	±1.5%	–40°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. \*Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Terminal Finish Part Marking:  
[www.linear.com/leadfree](http://www.linear.com/leadfree)

- Recommended BGA PCB Assembly and Manufacturing Procedures:  
[www.linear.com/umodule/pcbassembly](http://www.linear.com/umodule/pcbassembly)
- BGA Package and Tray Drawings:  
[www.linear.com/packaging](http://www.linear.com/packaging)

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel.  $T_A = 25^\circ\text{C}$  (Note 2),  $V_{IN} = 12\text{V}$  and  $V_{RUN1}$ ,  $V_{RUN2}$  at 5V unless otherwise noted. Per the typical application in Figure 24.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN}$	Input DC Voltage	●	4.5		15	V
$V_{OUT}$	Output DC Voltage	●	0.6		1.8	V
$V_{OUT1(DC)}$ , $V_{OUT2(DC)}$	Output Voltage, Total Variation with Line and Load	$C_{IN} = 22\mu\text{F} \times 3$ , $C_{OUT} = 100\mu\text{F} \times 2$ Ceramic, 470 $\mu\text{F}$ POSCAP $V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ , $I_{OUT} = 0\text{A}$ to 25A A-Grade (0.8%) B-Grade (1.5%)	● ●	1.190 1.182	1.210 1.218	V V

#### Input Specifications

$V_{RUN1}$ , $V_{RUN2}$	RUN Pin On/Off Threshold	RUN Rising		1.1	1.25	1.40	V
$V_{RUN1HYS}$ , $V_{RUN2HYS}$	RUN Pin On Hysteresis				150		mV
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	$I_{OUT} = 0\text{A}$ , $C_{IN} = 22\mu\text{F} \times 3$ , $C_{SS} = 0.01\mu\text{F}$ , $C_{OUT} = 100\mu\text{F} \times 3$ , $V_{OUT} = 1.2\text{V}$			1		A
$I_Q(VIN)$	Input Supply Bias Current (Both Channel Running)	$V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ , Burst Mode Operation $V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ , Pulse-Skipping Mode $V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ , Switching Continuous Shutdown, RUN = 0, $V_{IN} = 12\text{V}$			4.5 25 240 35		mA mA mA $\mu\text{A}$
$I_S(VIN)$	Input Supply Current	$V_{IN} = 4.5\text{V}$ , $V_{OUT} = 1.2\text{V}$ , $I_{OUT} = 25\text{A}$ $V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ , $I_{OUT} = 25\text{A}$			8.4 3.2		A A

#### Output Specifications

$I_{OUT1(DC)}$ , $I_{OUT2(DC)}$	Output Continuous Current Range	$V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ (Note 6)		0		25	A
$\Delta V_{OUT1(LINE)}/V_{OUT1}$ $\Delta V_{OUT2(LINE)}/V_{OUT2}$	Line Regulation Accuracy	$V_{OUT} = 1.2\text{V}$ , $V_{IN}$ from 4.5V to 15V $I_{OUT} = 0\text{A}$ for Each Output,	●		0.01	0.1	%/V
$\Delta V_{OUT1}/V_{OUT1}$ $\Delta V_{OUT2}/V_{OUT2}$	Load Regulation Accuracy	For Each Output, $V_{OUT} = 1.2\text{V}$ , 0A to 25A $V_{IN} = 12\text{V}$ (Note 6) A-Grade B-Grade	● ●		0.1 0.2	0.4 0.75	% %
$V_{OUT1(AC)}$ , $V_{OUT2(AC)}$	Output Ripple Voltage	For Each Output, $I_{OUT} = 0\text{A}$ , $C_{OUT} = 100\mu\text{F} \times 3$ Ceramic, 470 $\mu\text{F}$ POSCAP, $V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ , Frequency = 500kHz			15		mV <sub>p-p</sub>
$f_S$ (Each Channel)	Output Ripple Voltage Frequency	$V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ , $f_{SET} = 1.25\text{V}$ (Note 4)			500		kHz
$f_{SYNC}$ (Each Channel)	SYNC Capture Range			400		780	kHz
$\Delta V_{OUTSTART}$ (Each Channel)	Turn-On Overshoot	$C_{OUT} = 100\mu\text{F}$ Ceramic, 470 $\mu\text{F}$ POSCAP, $V_{OUT} = 1.2\text{V}$ , $I_{OUT} = 0\text{A}$ , $V_{IN} = 12\text{V}$			10		mV
$t_{START}$ (Each Channel)	Turn-On Time	$C_{OUT} = 100\mu\text{F}$ Ceramic, 470 $\mu\text{F}$ POSCAP, No Load, TRACK/SS with 0.01 $\mu\text{F}$ to GND, $V_{IN} = 12\text{V}$			5		ms
$\Delta V_{OUT(LS)}$ (Each Channel)	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load $C_{OUT} = 22\mu\text{F} \times 3$ Ceramic, 470 $\mu\text{F}$ POSCAP $V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$			30		mV

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel.  $T_A = 25^\circ\text{C}$  (Note 2),  $V_{IN} = 12\text{V}$  and  $V_{RUN1}$ ,  $V_{RUN2}$  at 5V unless otherwise noted. Per the typical application in Figure 24.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{SETTLE}$ (Each Channel)	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, $V_{IN} = 12\text{V}$ , $C_{OUT} = 100\mu\text{F}$ , $470\mu\text{F}$ POSCAP		20		$\mu\text{s}$
$I_{OUT(PK)}$ (Each Channel)	Output Current Limit	$V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$		35		A

#### Control Section

$V_{FB1}$ , $V_{FB2}$	Voltage at $V_{FB}$ Pins	$I_{OUT} = 0\text{A}$ , $V_{OUT} = 1.2\text{V}$ A-Grade B-Grade	● ●	0.596 0.594	0.600 0.600	0.604 0.606	V V
$I_{FB}$		(Note 5)			-5	-20	nA
$V_{OVL}$	Feedback Overvoltage Lockout		●	0.64	0.66	0.68	V
TRACK1 (I), TRACK2 (I)	Track Pin Soft-Start Pull-Up Current	TRACK1 (I), TRACK2 (I) Start at 0V		1	1.3	1.5	$\mu\text{A}$
UVLO	Undervoltage Lockout (Falling)				3.3		V
UVLO Hysteresis					0.6		V
$t_{ON(MIN)}$	Minimum On-Time	(Note 5)			90		ns
$R_{FBH11}$ , $R_{FBH12}$	Resistor Between $V_{OUTS1}$ , $V_{OUTS2}$ and $V_{FB1}$ , $V_{FB2}$ Pins for Each Output			60.05	60.4	60.75	k $\Omega$
$V_{PGOOD1}$ , $V_{PGOOD2}$ Low	PGOOD Voltage Low	$I_{PGOOD} = 2\text{mA}$			0.1	0.3	V
$I_{PGOOD}$	PGOOD Leakage Current	$V_{PGOOD} = 5\text{V}$				$\pm 5$	$\mu\text{A}$
$V_{PGOOD}$	PGOOD Trip Level	$V_{FB}$ with Respect to Set Output Voltage $V_{FB}$ Ramping Negative $V_{FB}$ Ramping Positive			-10 10		% %

#### INTV<sub>CC</sub> Linear Regulator

$V_{INTVCC}$	Internal $V_{CC}$ Voltage	$6\text{V} < V_{IN} < 15\text{V}$		4.8	5	5.2	V
$V_{INTVCC}$ Load Regulation	INTV <sub>CC</sub> Load Regulation	$I_{CC} = 0\text{mA}$ to $50\text{mA}$			0.75	2	%
$V_{EXTVCC}$	EXTV <sub>CC</sub> Switchover Voltage	EXTV <sub>CC</sub> Ramping Positive		4.5	4.7		V
$V_{EXTVCC(DROP)}$	EXTV <sub>CC</sub> Dropout	$I_{CC} = 20\text{mA}$ , $V_{EXTVCC} = 5\text{V}$			50	100	mV
$V_{EXTVCC(HYST)}$	EXTV <sub>CC</sub> Hysteresis				220		mV

#### Oscillator and Phase-Locked Loop

Frequency Nominal	Nominal Frequency	$f_{SET} = 1.2\text{V}$		450	500	550	kHz
Frequency Low	Lowest Frequency	$f_{SET} = 0.93\text{V}$			400		kHz
Frequency High	Highest Frequency	$f_{SET} > 2.4\text{V}$ , Up to INTV <sub>CC</sub>			780		kHz
$f_{SET}$	Frequency Set Current			9	10	11	$\mu\text{A}$
$R_{MODE\_PLLIN}$	MODE_PLLIN Input Resistance				250		k $\Omega$
CLKOUT	Phase (Relative to $V_{OUT1}$ )	PHASMD = GND PHASMD = Float PHASMD = INTV <sub>CC</sub>			60 90 120		Deg Deg Deg
CLK High	Clock High Output Voltage			2			V
CLK Low	Clock Low Output Voltage					0.2	V

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel.  $T_A = 25^\circ\text{C}$  (Note 2),  $V_{IN} = 12\text{V}$  and  $V_{RUN1}$ ,  $V_{RUN2}$  at 5V unless otherwise noted. Per the typical application in Figure 24.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Differential Amplifier</b>						
$A_V$ Differential Amplifier	Gain			1		V/V
$R_{IN}$	Input Resistance	Measured at DIFFP Input		80		$k\Omega$
$V_{OS}$	Input Offset Voltage	$V_{DIFFP} = V_{DIFFOUT} = 1.2\text{V}$ , $I_{DIFFOUT} = 100\mu\text{A}$			3	mV
PSRR Differential Amplifier	Power Supply Rejection Ratio	$5\text{V} < V_{IN} < 15\text{V}$		90		dB
$I_{CL}$	Maximum Output Current			3		mA
$V_{OUT(MAX)}$	Maximum Output Voltage	$I_{DIFFOUT} = 300\mu\text{A}$	$INTV_{CC} - 1.4$			V
GBW	Gain Bandwidth Product			3		MHz
$V_{TEMP}$	Diode Connected PNP	$I = 100\mu\text{A}$		0.6		V
TC	Temperature Coefficient		●	-2.2		mV/C

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTM4650-1 is tested under pulsed load conditions such that  $T_J \approx T_A$ . The LTM4650-1E is guaranteed to meet specifications from  $0^\circ\text{C}$  to  $125^\circ\text{C}$  internal temperature. Specifications over the  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4650-1I is guaranteed over the full  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

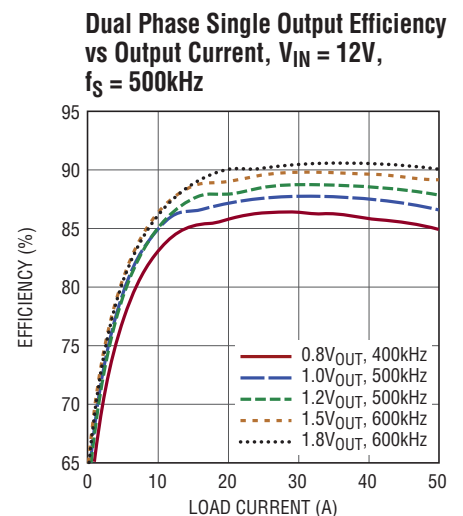
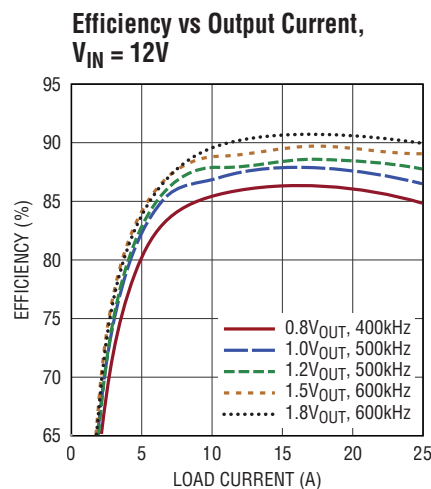
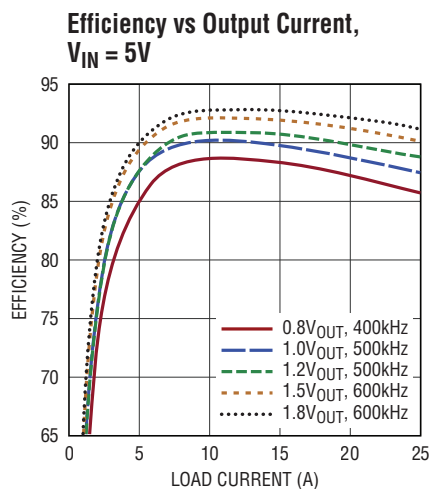
**Note 3:** Two outputs are tested separately and the same testing condition is applied to each output.

**Note 4:** LTM4650-1 device is designed to operate from 400kHz to 750kHz.

**Note 5:** These parameters are tested at wafer sort.

**Note 6:** See output current derating curves for different  $V_{IN}$ ,  $V_{OUT}$  and  $T_A$ .

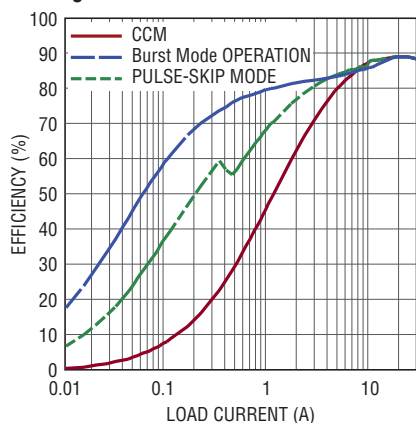
## TYPICAL PERFORMANCE CHARACTERISTICS



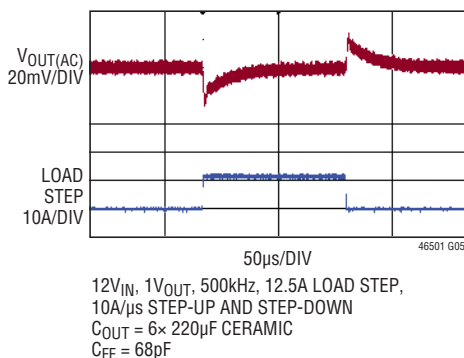
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## TYPICAL PERFORMANCE CHARACTERISTICS

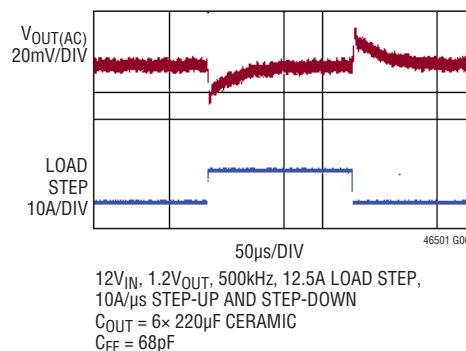
**Burst Mode and Pulse-Skip Mode Efficiency**  $V_{IN}=12V$ ,  $V_{OUT} = 1.2V$ ,  $f_s = 500kHz$



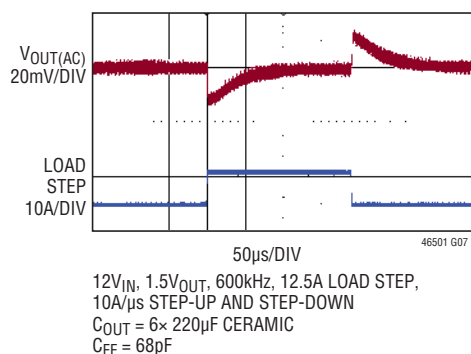
**1V Dual Phase Single Output Load Transient Response**



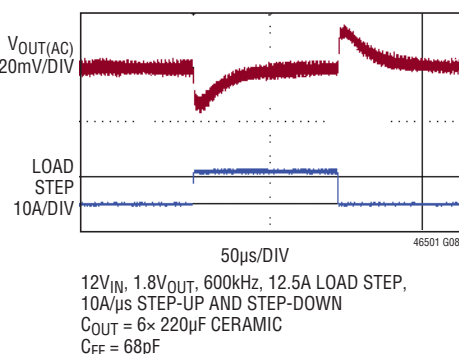
**1.2V Dual Phase Single Output Load Transient Response**



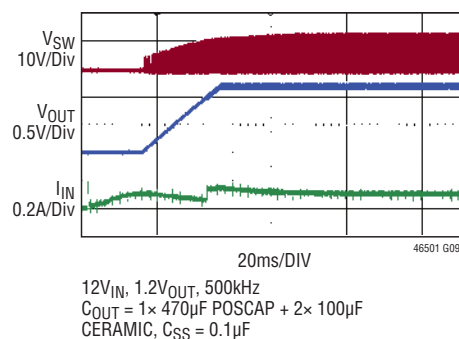
**1.5V Dual Phase Single Output Load Transient Response**



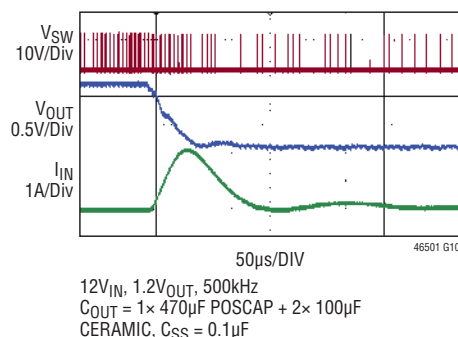
**1.8V Dual Phase Single Output Load Transient Response**



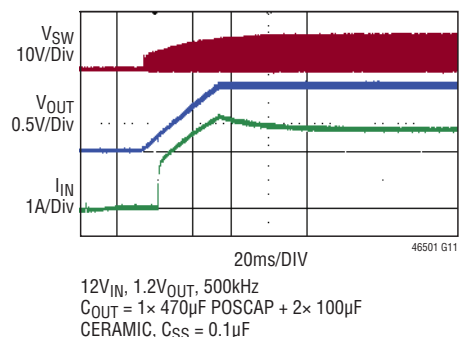
**Single Phase Start-Up with No load**



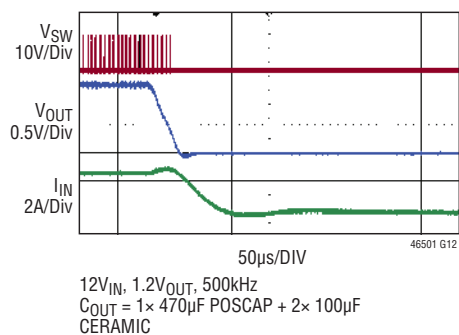
**Single Phase Start-up with 25A**



**Single Phase Short Circuit Protection with No load**



**Single Phase Short Circuit Protection with 25A**



## PIN FUNCTIONS (Recommended to Use Test Points to Monitor Signal Pin Connections.)



**PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.**

**$V_{OUT1}$  (A1-A5, B1-B5, C1-C4):** Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. Review Table 4.

**GND (A6-A7, B6-B7, D1-D4, D9-D12, E1-E4, E10-E12, F1-F3, F10-F12, G1, G3, G10, G12, H1-H7, H9-H12, J1, J5, J8, J12, K1, K5-K8, K12, L1, L12, M1, M12):** Power Ground Pins for Both Input and Output Returns.

**$V_{OUT2}$  (A8-A12, B8-B12, C9-C12):** Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. Review Table 4.

**$V_{OUTS1}$ ,  $V_{OUTS2}$  (C5, C8):** This pin is connected to the top of the internal top feedback resistor for each output. The pin can be directly connected to its specific output, or connected to DIFFOUT when the remote sense amplifier is used. In paralleling modules, one of the  $V_{OUTS}$  pins is connected to the DIFFOUT pin in remote sensing or directly to  $V_{OUT}$  with no remote sensing. It is very important to connect these pins to either the DIFFOUT or  $V_{OUT}$  since this is the feedback path, and cannot be left open. See the Applications Information section.

**$f_{SET}$  (C6):** Frequency Set Pin. A 10 $\mu$ A current is sourced from this pin. A resistor from this pin to ground sets a voltage that in turn programs the operating frequency. Alternatively, this pin can be driven with a DC voltage that can set the operating frequency. See the Applications Information section.

**SGND (C7, D6, G6-G7, F6-F7):** Signal Ground Pin. Return ground path for all analog and low power circuitry. Tie a single connection to the output capacitor GND in the application. See layout guidelines in Figure 13.

**$V_{FB1}$ ,  $V_{FB2}$  (D5, D7):** The Negative Input of the Error Amplifier for Each Channel. Internally, this pin is connected to  $V_{OUTS1}$  or  $V_{OUTS2}$  with a 60.4k $\Omega$  precision resistor. Different output voltages can be programmed with an additional resistor between  $V_{FB}$  and GND pins. In PolyPhase<sup>®</sup> operation, tying the  $V_{FB}$  pins together allows for parallel operation. See the Applications Information section for details.

**TRACK1, TRACK2 (E5, D8):** Output Voltage Tracking Pin and Soft-Start Inputs. Each channel has a 1.3 $\mu$ A pull-up current source. When one channel is configured to be master of the two channels, then a capacitor from this pin to ground will set a soft-start ramp rate. The remaining channel can be set up as the slave, and have the master's output applied through a voltage divider to the slave output's track pin. This voltage divider is equal to the slave output's feedback divider for coincidental tracking. See the Applications Information section.

**COMP1, COMP2 (E6, E7):** Current control threshold and error amplifier compensation point for each channel. The current comparator threshold increases with this control voltage. COMP pin internal has 10pF filter cap to SGND. An external RC filter circuit is required for control loop compensation. See Applications Information section. Tie the COMP pins together for parallel operation. Do not drive this pin.

**DIFFP (E8):** Positive input of the remote sense amplifier. This pin is connected to the remote sense point of the output voltage. See the Applications Information section.

**DIFFN (E9):** Negative input of the remote sense amplifier. This pin is connected to the remote sense point of the output GND. See the Applications Information section.



## PIN FUNCTIONS (Recommended to Use Test Points to Monitor Signal Pin Connections.)

**MODE\_PLLIN (F4):** Force Continuous Mode, Burst Mode Operation, or Pulse-Skipping Mode Selection Pin and External Synchronization Input to Phase Detector Pin. Connect this pin to SGND to force both channels into force continuous mode of operation. Connect to INTV<sub>CC</sub> to enable pulse-skipping mode of operation. Leaving the pin floating will enable Burst Mode operation. A clock on the pin will force both channels into continuous mode of operation and synchronized to the external clock applied to this pin.

**RUN1, RUN2 (F5, F9):** Run Control Pin. A voltage above 1.25V will turn on each channel in the module. A voltage below 1.25V on the RUN pin will turn off the related channel. Each RUN pin has a 1 $\mu$ A pull-up current, once the RUN pin reaches 1.2V an additional 4.5 $\mu$ A pull-up current is added to this pin.

**DIFFOUT (F8):** Internal Remote Sense Amplifier Output. Connect this pin to V<sub>OUTS1</sub> or V<sub>OUTS2</sub> depending on which output is using remote sense. In parallel operation connect one of the V<sub>OUTS</sub> pin to DIFFOUT for remote sensing.

**SW1, SW2 (G2, G11):** Switching node of each channel that is used for testing purposes. Also an R-C snubber network can be applied to reduce or eliminate switch node ringing, or otherwise leave floating. See the Applications Information section.

**PHASMD (G4):** Connect this pin to SGND, INTV<sub>CC</sub>, or floating this pin to select the phase of CLKOUT to 60 degrees, 120 degrees, and 90 degrees respectively.

**CLKOUT (G5):** Clock output with phase control using the PHASMD pin to enable multiphase operation between devices. See the Applications Information section.

**PGOOD1, PGOOD2 (G9, G8):** Output Voltage Power Good Indicator. Open drain logic output that is pulled to ground when the output voltage is not within  $\pm 10\%$  of the regulation point.

**INTV<sub>CC</sub> (H8):** Internal 5V Regulator Output. The control circuits and internal gate drivers are powered from this voltage. Decouple this pin to PGND with a 4.7 $\mu$ F low ESR tantalum or ceramic. INTV<sub>CC</sub> is activated when either RUN1 or RUN2 is activated.

**TEMP (J6):** Temperature Monitor. An internal diode connected NPN transistor between this pin and SGND with 10nF filtering capacitor. See the Applications Information section.

**EXTV<sub>CC</sub> (J7):** External power input that is enabled through a switch to INTV<sub>CC</sub> whenever EXTV<sub>CC</sub> is greater than 4.7V. Do not exceed 6V on this input, and connect this pin to V<sub>IN</sub> when operating V<sub>IN</sub> on 5V. An efficiency increase will occur that is a function of the (V<sub>IN</sub> – INTV<sub>CC</sub>) multiplied by power MOSFET driver current. Typical current requirement is 30mA. V<sub>IN</sub> must be applied before EXTV<sub>CC</sub>, and EXTV<sub>CC</sub> must be removed before V<sub>IN</sub>.

**V<sub>IN</sub> (M2-M11, L2-L11, J2-J4, J9-J11, K2-K4, K9-K11):** Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V<sub>IN</sub> pins and GND pins.



## SIMPLIFIED BLOCK DIAGRAM

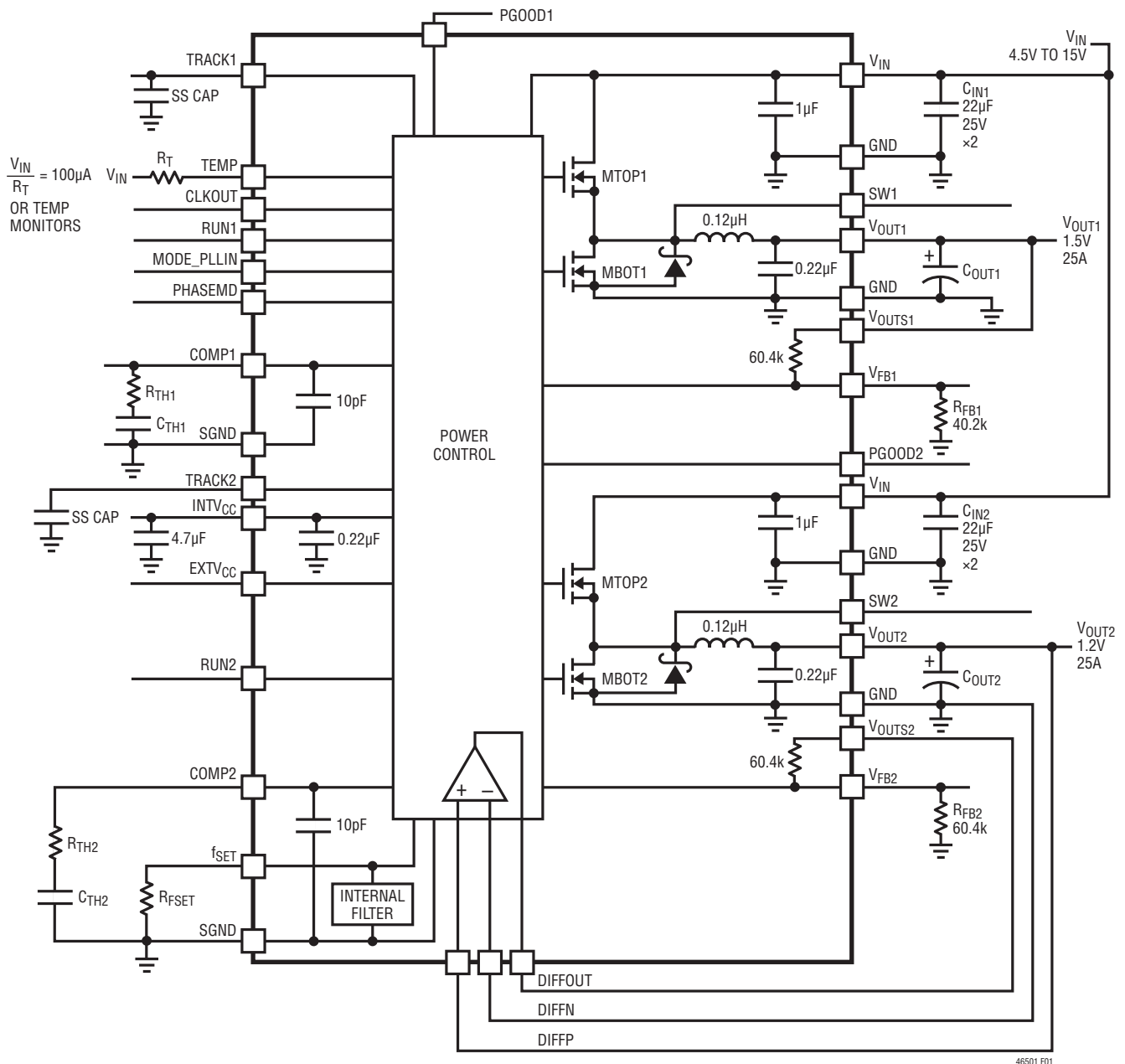


Figure 1. Simplified LTM4650-1 Block Diagram

DECOUPLING REQUIREMENTS  $T_A = 25^\circ\text{C}$ . Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$C_{IN1}, C_{IN2}$	External Input Capacitor Requirement ( $V_{IN1} = 4.5\text{V to }15\text{V}$ , $V_{OUT1} = 1.5\text{V}$ ) ( $V_{IN2} = 4.5\text{V to }15\text{V}$ , $V_{OUT2} = 1.0\text{V}$ )	$I_{OUT1} = 25\text{A}$ $I_{OUT2} = 25\text{A}$	44	66		$\mu\text{F}$
			44	66		$\mu\text{F}$
$C_{OUT1}$ $C_{OUT2}$	External Output Capacitor Requirement ( $V_{IN1} = 4.5\text{V to }15\text{V}$ , $V_{OUT1} = 1.5\text{V}$ ) ( $V_{IN2} = 4.5\text{V to }15\text{V}$ , $V_{OUT2} = 1.0\text{V}$ )	$I_{OUT1} = 25\text{A}$ $I_{OUT2} = 25\text{A}$	600	800		$\mu\text{F}$
			600	800		$\mu\text{F}$

46501fc

## OPERATION

### Power Module Description

The LTM4650-1 is a dual-output standalone nonisolated switching mode DC/DC power supply with  $\pm 0.8\%$  (A-Grade) total DC output error over line, load and temperature variation. It can provide two 25A outputs with few external input and output capacitors and setup components. This module provides precisely regulated output voltages programmable via external resistors from  $0.6V_{DC}$  to  $1.8V_{DC}$  over 4.5V to 15V input voltages. The typical application schematic is shown in Figure 24.

The LTM4650-1 has dual integrated constant-frequency current mode regulators and built-in power MOSFET devices with fast switching speed. The typical switching frequency is from 400kHz to 600kHz depending on output voltage. For switching-noise sensitive applications, it can be externally synchronized from 400kHz to 780kHz. A resistor can be used to program a free run frequency on the FSET pin. See the Applications Information section.

With current mode control, the LTM4650-1 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit and foldback current limit in an overcurrent condition. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD outputs low if the output feedback voltage exits a  $\pm 10\%$  window around the regulation point. As the output voltage exceeds 10% above regulation, the bottom MOSFET will turn on to clamp the output voltage. The top MOSFET will be turned off. This overvoltage protect is feedback voltage referred.

Pulling the RUN pins below 1.1V forces the regulators into a shutdown state, by turning off both MOSFETs. The TRACK pins are used for programming the output voltage ramp and voltage tracking during start-up or used for soft-starting the regulator. See the Applications Information section.

The LTM4650-1 has a built-in 10pF high frequency filter cap from COMP to SGND for each output. An external RC filtering circuit is required to achieve fast Type II control loop compensation. Table 4 provides a guide line for input, output capacitances and RC comp values for several operating conditions. The Linear Technology  $\mu$ Module Power Design Tool (LTpowerCAD<sup>®</sup>) will be provided for transient and stability analysis. The  $V_{FB}$  pin is used to program the output voltage with a single external resistor to ground. A differential remote sense amplifier is available for sensing the output voltage accurately on one of the outputs at the load point, or in parallel operation sensing the output voltage at the load point.

Multiphase operation can be easily employed with the MODE\_PLLIN, PHASMD, and CLKOUT pins. Up to 12 phases can be cascaded to run simultaneously with respect to each other by programming the PHASMD pin to different levels. See the Applications Information section.

High efficiency at light loads can be accomplished with selectable Burst Mode operation or pulse-skipping operation using the MODE\_PLLIN pin. These light load features will accommodate battery operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section. See the Applications Information section for details.

A general purpose temperature diode is included inside the module to monitor the temperature of the module. See the Applications Information section for details.

The switch pins are available for functional operation monitoring and a resistor-capacitor snubber circuit can be carefully placed on the switch pin to ground to dampen any high frequency ringing on the transition edges. See the Applications Information section for details.

## APPLICATIONS INFORMATION

The typical LTM4650-1 application circuit is shown in Figure 24. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 4 for specific external capacitor requirements for particular applications.

### OUTPUT TOTAL DC ACCURACY AND AC TRANSIENT PERFORMANCE

In modern ASIC and FPGA power supply designs, a tight total voltage regulation window,  $\pm 3\%$  for example, is required of the supply powering the core and periphery. To meet this requirement, the supply's DC voltage variance plus any AC voltage variation which may occur during any load step transient must fall within this allowed window. The DC voltage variance is determined by the accuracies of the supply's reference voltage, resistor divider, load regulation and line regulation over the operating temperature range. The AC voltage variance is determined by the supply's output voltage overshoot and undershoots in response to a load transient condition for a given output capacitor network.

Figure 2 shows a typical load step transient response waveform together with DC voltage accuracy variance. For a given allowable voltage regulation window, a tighter DC voltage accuracy allows more margin for the AC variation due to a load transient response. This increased margin for AC variation allows for a reduction in the total output capacitance required to meet the regulation window requirement. This allows for a reduced total solution cost and footprint area.

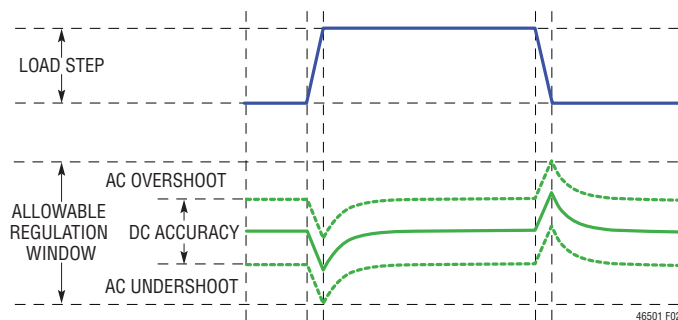


Figure 2. Typical Load Step Transient Response with DC Voltage Accuracy Variance

For example, in an FPGA core voltage application, for a 12V input, 0.9V output at 72A design, a total overall  $\pm 3\%$  total voltage regulation window is required in responding to a 25% load step transient. Figure 3 illustrates the benefit of overall output capacitor reduction versus improved total DC accuracy by using 100 $\mu$ F ceramic output capacitors.

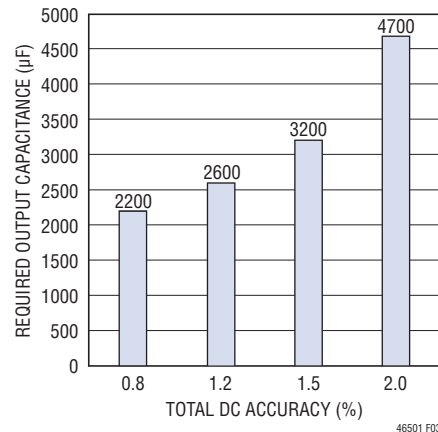


Figure 3. Overall Output Capacitor vs Total DC Accuracy

### $V_{IN}$ to $V_{OUT}$ Step-Down Ratios

There are restrictions in the maximum  $V_{IN}$  and  $V_{OUT}$  step-down ratio that can be achieved for a given input voltage. Each output of the LTM4650-1 is capable of 98% duty cycle, but the  $V_{IN}$  to  $V_{OUT}$  minimum dropout is still shown as a function of its load current and will limit output current capability related to high duty cycle on the top side switch. Minimum on-time  $t_{ON(MIN)}$  is another consideration in operating at a specified duty cycle while operating at a certain frequency due to the fact that  $t_{ON(MIN)} < D/f_{SW}$ , where  $D$  is duty cycle and  $f_{SW}$  is the switching frequency.  $t_{ON(MIN)}$  is specified in the electrical parameters as 90ns.

### Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 60.4k $\Omega$  internal feedback resistor connects between the  $V_{OUTS1}$  to  $V_{FB1}$  and  $V_{OUTS2}$  to  $V_{FB2}$ . It is very important that these pins be connected to their respective outputs for proper feedback regulation. Overvoltage can occur if these  $V_{OUTS1}$  and  $V_{OUTS2}$  pins are left floating when used as individual regulators, or at least one of them is used in paralleled regulators. The output voltage will default to 0.6V with no feedback resistor on

## APPLICATIONS INFORMATION

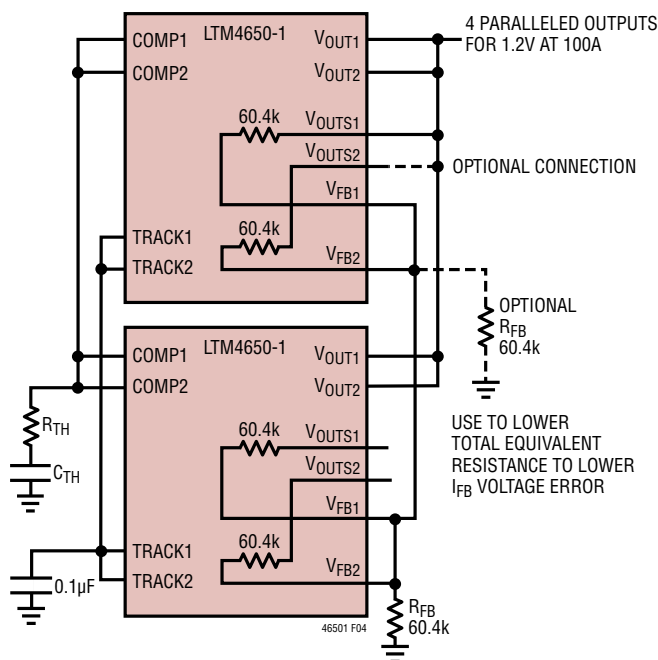
either  $V_{FB1}$  or  $V_{FB2}$ . Adding a resistor  $R_{FB}$  from  $V_{FB}$  pin to GND programs the output voltage:

$$V_{OUT} = 0.6V \cdot \frac{60.4k + R_{FB}}{R_{FB}}$$

### Table 1. $V_{FB}$ Resistor Table vs Various Output Voltages

<b>V<sub>OUT</sub></b>	0.6V	0.8V	0.9V	1.0V	1.2V	1.5V	1.8V
<b>R<sub>FB</sub></b>	Open	182k	121k	90.9k	60.4k	40.2k	30.2k

For parallel operation of multiple channels the same feedback setting resistor can be used for the parallel design. This is done by connecting the  $V_{OUTS1}$  to the output as shown in Figure 4, thus tying one of the internal 60.4k resistors to the output. All of the  $V_{FB}$  pins tie together with one programming resistor as shown in Figure 4.



### Figure 4. 4-Phase Parallel Configurations

In parallel operation, the  $V_{FB}$  pins have an  $I_{FB}$  current of 20nA maximum each channel. To reduce output voltage error due to this current, an additional  $V_{OUTS}$  pin can be tied to  $V_{OUT}$ , and an additional  $R_{FB}$  resistor can be used to lower the total Thevenin equivalent resistance seen by this current. For example in Figure 4, the total Thevenin equivalent resistance of the  $V_{FB}$  pin is  $(60.4k//R_{FB})$ , which is 30.2k where  $R_{FB}$  is

equal to 60.4k for a 1.2V output. Four phases connected in parallel equates to a worse case feedback current of  $4 \cdot I_{FB} = 80\text{nA}$  maximum. The voltage error is  $80\text{nA} \cdot 30.2\text{k} = 2.4\text{mV}$ . If  $V_{OUTS2}$  is connected, as shown in Figure 2, to  $V_{OUT}$ , and another 60.4k resistor is connected from  $V_{FB2}$  to ground, then the voltage error is reduced to 1.2mV. If the voltage error is acceptable then no additional connections are necessary. The onboard 60.4k resistor is 0.5% accurate and the  $V_{FB}$  resistor can be chosen by the user to be as accurate as needed. All COMP pins are tied together for current sharing between the phases. The TRACK/SS pins can be tied together and a single soft-start capacitor can be used to soft-start the regulator. The soft-start equation will need to have the soft-start current parameter increased by the number of paralleled channels. See Output Voltage Tracking section.

## Input Capacitors

The LTM4650-1 module should be connected to a low AC-impedance DC source. For the regulator input two 22 $\mu$ F input ceramic capacitors are required for each channel for RMS ripple current. A 47 $\mu$ F to 100 $\mu$ F surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty-cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor current ripple, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \cdot \sqrt{D \cdot (1-D)}$$

In the above equation,  $\eta\%$  is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor, Polymer capacitor.

## APPLICATIONS INFORMATION

### Output Capacitors

The LTM4650-1 is designed for low output voltage ripple noise and good transient response. The bulk output capacitors defined as  $C_{OUT}$  are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements.  $C_{OUT}$  can be a low ESR tantalum capacitor, the low ESR polymer capacitor or ceramic capacitor. The typical output capacitance range for each output is from 400 $\mu$ F to 600 $\mu$ F. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 4 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 12.5A (25%) and 25A (50%) load step transient. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 4 matrix, and the Linear Technology LTpowerCAD Design Tool will be provided for stability analysis. In multi LTM4650-1 paralleling applications, Table 4 RC compensation value is still valid in terms of having one set of RC filters on each of the paralleling modules while connecting all the COMP, FB and  $V_{OUT}$  pins together. See Figure 29 and Multiphase Operation section. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. The Linear Technology LTpowerCAD Design Tool can calculate the output ripple reduction as the number of implemented phases increases by N times. A small value 10 $\Omega$  to 50 $\Omega$  resistor can be placed in series from  $V_{OUT}$  to the  $V_{OUTS}$  pin to allow for a bode plot analyzer to inject a signal into the control loop and validate the regulator stability. The same resistor could be placed in series from  $V_{OUT}$  to DIFFP and a bode plot analyzer could inject a signal into the control loop and validate the regulator stability.

### Burst Mode Operation

The LTM4650-1 is capable of Burst Mode operation on each regulator in which the power MOSFETs operate intermittently based on load demand, thus saving quiescent current. For applications where maximizing the efficiency at very light loads is a high priority, Burst Mode operation should be applied. Burst Mode operation is enabled with the MODE\_PLLIN pin floating. During this operation, the peak current of the inductor is set to approximately one third of the maximum peak current value in normal operation even though the voltage at the COMP pin indicates a lower value. The voltage at the COMP pin drops when the inductor's average current is greater than the load requirement. As the COMP voltage drops below 0.5V, the BURST comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

In sleep mode, the internal circuitry is partially turned off, reducing the quiescent current to about 450 $\mu$ A for each output. The load current is now being supplied from the output capacitors. When the output voltage drops, causing COMP to rise above 0.5V, the internal sleep line goes low, and the LTM4650-1 resumes normal operation. The next oscillator cycle will turn on the top power MOSFET and the switching cycle repeats. Either regulator can be configured for Burst Mode operation.

### Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping mode should be used. Pulse-skipping operation allows the LTM4650-1 to skip cycles at low output loads, thus increasing efficiency by reducing switching loss. Tying the MODE\_PLLIN pin to INTV<sub>CC</sub> enables pulse-skipping operation. At light loads the internal current comparator may remain tripped for several cycles and force the top MOSFET to stay off for several cycles, thus skipping cycles. The inductor current does not reverse in this mode. This mode will maintain higher effective frequencies thus lower output ripple and lower noise than Burst Mode operation. Either regulator can be configured for pulse-skipping mode.



## APPLICATIONS INFORMATION

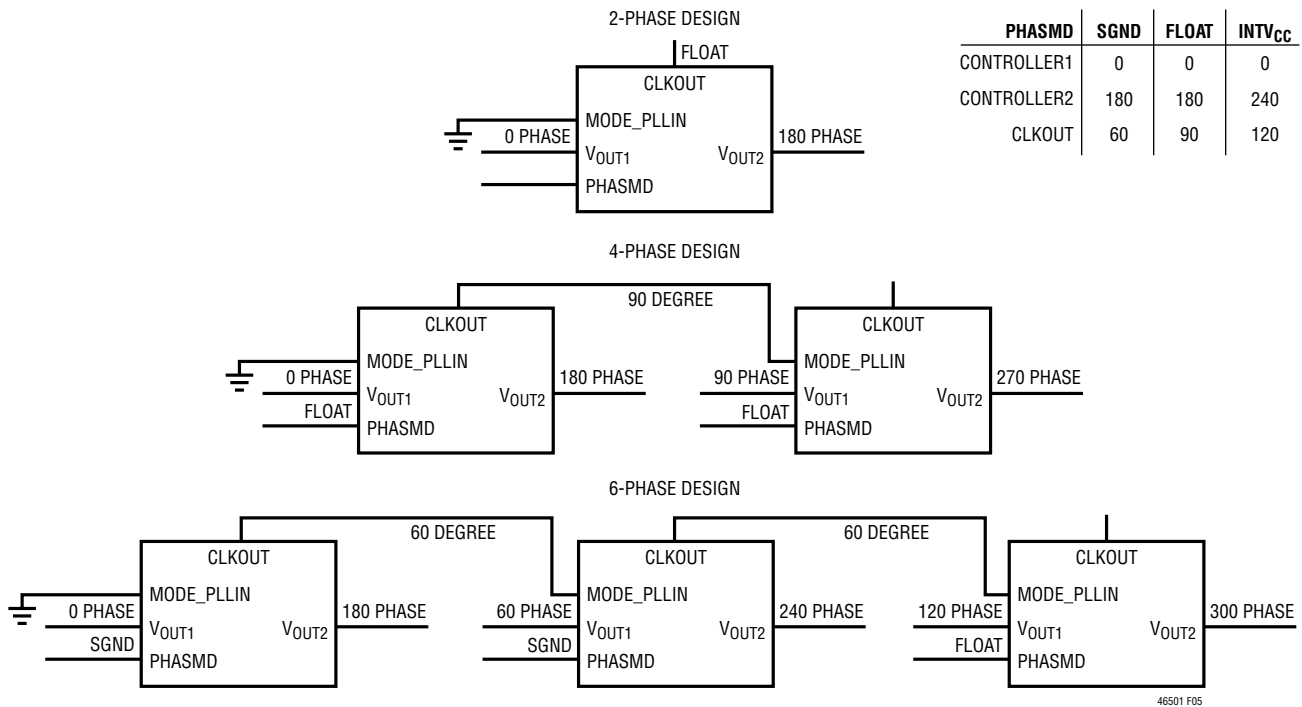


Figure 5. Examples of 2-Phase, 4-Phase, and 6-Phase Operation with PHASMD Table

## Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE\_PLLIN pin to GND. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4650-1's output voltage is in regulation. Either regulator can be configured for force continuous mode.

## Multiphase Operation

For output loads that demand more than 25A of current, two outputs in LTM4650-1 or even multiple LTM4650-1s can be paralleled to run out of phase to provide more output current without increasing input and output voltage ripples. The MODE\_PLLIN pin allows the LTM4650-1 to synchronize to an external clock (between 400kHz and 780kHz) and the internal phase-locked-loop allows the LTM4650-1 to lock onto incoming clock phase as well. The CLKOUT signal can be connected to the MODE\_PLLIN pin of the following stage to line up both the frequency and the phase of the entire system. Tying the PHASMD pin to INTV<sub>CC</sub>, SGND, or floating generates a phase difference (between MODE\_PLLIN and CLKOUT) of 120 degrees, 60 degrees, or 90 degrees respectively. A total of 12 phases can be cascaded to run simultaneously with respect to each other by programming the PHASMD pin of each LTM4650-1 channel to different levels. Figure 5 shows a 2-phase design, 4-phase design and a 6-phase design example for clock phasing with the PHASMD table.



## APPLICATIONS INFORMATION

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all of the outputs are tied together to achieve a single high output current design.

In multi LTM4650-1s parallel applications,  $C_{TH}$  and  $R_{TH}$  values in Table 4 are still valid to achieve a  $\pm 3\%$  transient response in a 25% load step. Connect one set of RC ( $R_{TH}$  and  $C_{TH}$ ) network to the COMP pin of each paralleling module like a dual phase single output setup. Then connect the COMP pins, FB pins, TRACK/SS pin and  $V_{OUT}$  pins from different modules together. See Figure 29 for an example of parallel operation. LTpowerCAD Power Design Tool can also be used to optimize loop compensation and transient performance if only one set of RC ( $R_{TH}$  and  $C_{TH}$ ) network is to be added to the common COMP pins.

The LTM4650-1 device is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. Figure 29 shows an example of parallel operation and pin connection.

### Input RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 6 shows this graph.

### Frequency Selection and Phase-Lock Loop (MODE\_PLLIN and $f_{SET}$ Pins)

The LTM4650-1 device is operated over a range of frequencies to improve power conversion efficiency. It is recommended to operate the module at 400kHz for output voltage below 1.0V, 500kHz for output voltage between 1.0V to 1.5V and 600kHz for output voltage above 1.5V, for the best efficiency and inductor current ripple.

The LTM4650-1 switching frequency can be set with an external resistor from the  $f_{SET}$  pin to SGND. An accurate 10 $\mu$ A current source into the resistor will set a voltage that programs the frequency or a DC voltage can be applied. Figure 7 shows a graph of frequency setting verses programming voltage. An external clock can be applied to the MODE\_PLLIN pin from 0V to  $INTV_{CC}$  over a frequency range of 400kHz to 780kHz. The clock input high threshold is 1.6V and the clock input low threshold is 1V. The LTM4650-1 has the PLL loop filter components on board. The frequency setting resistor should always be present to set the initial switching frequency before locking to an external clock. Both regulators will operate in continuous mode while being externally clock.

The output of the PLL phase detector has a pair of complementary current sources that charge and discharge the internal filter network. When the external clock is applied then the  $f_{SET}$  frequency resistor is disconnected with an internal switch, and the current sources control the frequency adjustment to lock to the incoming external clock. When no external clock is applied, then the internal switch is on, thus connecting the external  $f_{SET}$  frequency set resistor for free run operation.

APPLICATIONS INFORMATION

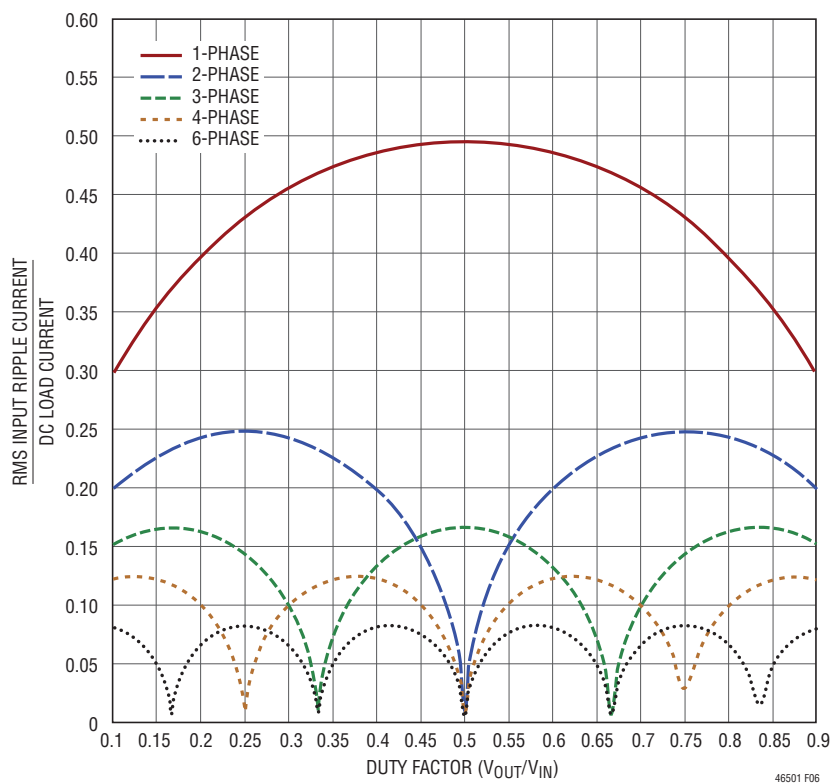


Figure 6. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle

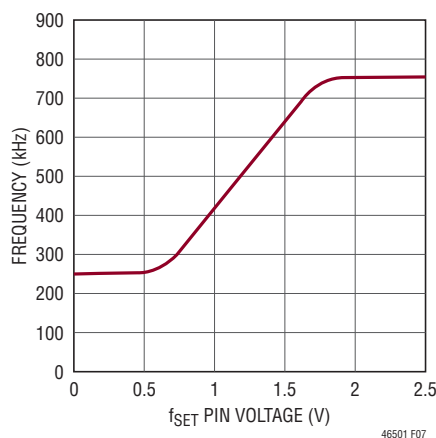


Figure 7. Operating Frequency vs  $f_{SET}$  Pin Voltage



## APPLICATIONS INFORMATION

output, then the slave will coincident track with the master until it reaches its final value. The master will continue to its final value from the slave's regulation point. Voltage tracking is disabled when  $V_{\text{TRACK}}$  is more than 0.6V.  $R_{\text{TA}}$  in Figure 8 will be equal to the  $R_{\text{FB}}$  for coincident tracking. Figure 9 shows the coincident tracking waveforms.

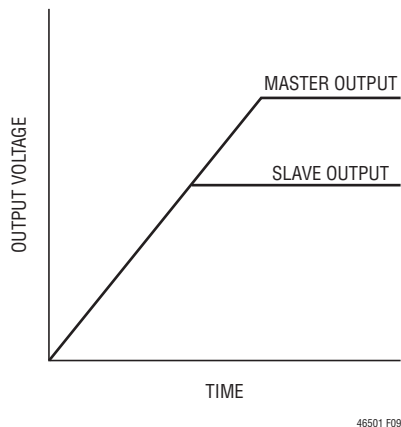


Figure 9. Output Coincident Tracking Waveform

The TRACK pin of the master can be controlled by a capacitor placed on the master regulator TRACK pin to ground. A 1.3μA current source will charge the TRACK pin up to the reference voltage and then proceed up to  $\text{INTV}_{\text{CC}}$ . After the 0.6V ramp, the TRACK pin will no longer be in control, and the internal voltage reference will control output regulation from the feedback divider. Foldback current limit is disabled during this sequence of turn-on during tracking or soft-starting. The TRACK pins are pulled low when the RUN pin is below 1.2V. The total soft-start time can be calculated as:

$$t_{\text{SOFT-START}} = \left( \frac{C_{\text{SS}}}{1.3\mu\text{A}} \right) \cdot 0.6$$

Regardless of the mode selected by the MODE\_PLLIN pin, the regulator channels will always start in pulse-skipping mode up to  $\text{TRACK} = 0.5\text{V}$ . Between  $\text{TRACK} = 0.5\text{V}$  and 0.54V, it will operate in forced continuous mode and revert to the selected mode once  $\text{TRACK} > 0.54\text{V}$ . In order to track with another channel once in steady state operation, the LTM4650-1 is forced into continuous mode operation

as soon as  $V_{\text{FB}}$  is below 0.54V regardless of the setting on the MODE\_PLLIN pin.

Ratiometric tracking can be achieved by a few simple calculations and the slew rate value applied to the master's TRACK pin. As mentioned above, the TRACK pin has a control range from 0 to 0.6V. The master's TRACK pin slew rate is directly equal to the master's output slew rate in Volts/Time. The equation:

$$\frac{\text{MR}}{\text{SR}} \cdot 60.4\text{k} = R_{\text{TB}}$$

where MR is the master's output slew rate and SR is the slave's output slew rate in Volts/Time. When coincident tracking is desired, then MR and SR are equal, thus  $R_{\text{TB}}$  is equal to the 60.4k.  $R_{\text{TA}}$  is derived from equation:

$$R_{\text{TA}} = \frac{0.6\text{V}}{\frac{V_{\text{FB}}}{60.4\text{k}} + \frac{V_{\text{FB}} - V_{\text{TRACK}}}{R_{\text{TB}}}}$$

where  $V_{\text{FB}}$  is the feedback voltage reference of the regulator, and  $V_{\text{TRACK}}$  is 0.6V. Since  $R_{\text{TB}}$  is equal to the 60.4k top feedback resistor of the slave regulator in equal slew rate or coincident tracking, then  $R_{\text{TA}}$  is equal to  $R_{\text{FB}}$  with  $V_{\text{FB}} = V_{\text{TRACK}}$ . Therefore  $R_{\text{TB}} = 60.4\text{k}$ , and  $R_{\text{TA}} = 60.4\text{k}$  in Figure 8.

In ratiometric tracking, a different slew rate maybe desired for the slave regulator.  $R_{\text{TB}}$  can be solved for when SR is slower than MR. Make sure that the slave supply slew rate is chosen to be fast enough so that the slave output voltage will reach its final value before the master output.

For example,  $\text{MR} = 1.5\text{V}/1\text{ms}$ , and  $\text{SR} = 1.2\text{V}/1\text{ms}$ . Then  $R_{\text{TB}} = 76.8\text{k}$ . Solve for  $R_{\text{TA}}$  to equal to 49.9k.

Each of the TRACK pins will have the 1.3μA current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK pin input. Smaller values resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 60.4k is used then a 6.04k can be used to reduce the TRACK pin offset to a negligible value.

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### Power Good

The PGOOD pins are open drain pins that can be used to monitor valid output voltage regulation. This pin monitors a 10% window around the regulation point. A resistor can be pulled up to a particular supply voltage no greater than 6V maximum for monitoring.

### Stability Compensation

The LTM4650-1 has a built-in 10pF high frequency filter capacitor from COMP to SGND on each output channel. An external RC filtering circuit is required to add from COMP to SGND to achieve fast Type II control loop compensation. Table 4 is provided for most application requirements. The Linear Technology  $\mu$ Module Power Design Tool (LTpowerCAD) will be provided for other control loop optimization.

### Run Enable

The RUN pins have an enable threshold of 1.4V maximum, typically 1.25V with 150mV of hysteresis. They control the turn on each of the channels and INTV<sub>CC</sub>. These pins can be pulled up to V<sub>IN</sub> for 5V operation, or a 5V Zener diode can be placed on the pins and a 10k to 100k resistor can be placed up to higher than 5V input for enabling the channels. The RUN pins can also be used for output voltage sequencing. In parallel operation the RUN pins can be tie together and controlled from a single control. See the Typical Application circuits in Figure 24.

### INTV<sub>CC</sub> and EXTV<sub>CC</sub>

The LTM4650-1 module has an internal 5V low dropout regulator that is derived from the input voltage. This regulator is used to power the control circuitry and the power MOSFET drivers. This regulator can source up to 70mA, and typically uses ~30mA for powering the device at the maximum frequency. This internal 5V supply is enabled by either RUN1 or RUN2.

EXTV<sub>CC</sub> allows an external 5V supply to power the LTM4650-1 and reduce power dissipation from the internal low dropout 5V regulator. The power loss savings can be calculated by:

$$(V_{IN} - 5V) \cdot 30mA = P_{LOSS}$$

EXTV<sub>CC</sub> has a threshold of 4.7V for activation, and a maximum rating of 6V. When using a 5V input, connect this 5V input to EXTV<sub>CC</sub> also to maintain a 5V gate drive level. EXTV<sub>CC</sub> must sequence on after V<sub>IN</sub>, and EXTV<sub>CC</sub> must sequence off before V<sub>IN</sub>.

### Differential Remote Sense Amplifier

An accurate differential remote sense amplifier is provided to sense low output voltages accurately at the remote load points. This is especially true for high current loads. The amplifier can be used on one of the two channels, or on a single parallel output. It is very important that the DIFFP and DIFFN are connected properly at the output, and DIFFOUT is connected to either V<sub>OUTS1</sub> or V<sub>OUTS2</sub>. In parallel operation, the DIFFP and DIFFN are connected properly at the output, and DIFFOUT is connected to one of the V<sub>OUTS</sub> pins. Review the parallel schematics in Figure 25 and review Figure 4.

### SW Pins

The SW pins are generally for testing purposes by monitoring these pins. These pins can also be used to dampen out switch node ringing caused by LC parasitic in the switched current paths. Usually a series R-C combination is used called a snubber circuit. The resistor will dampen the resonance and the capacitor is chosen to only affect the high frequency ringing across the resistor. If the stray inductance or capacitance can be measured or approximated then a somewhat analytical technique can be used to select the snubber values. The inductance is usually easier to predict. It combines the power path board inductance in combination with the MOSFET interconnect bond wire inductance.

First the SW pin can be monitored with a wide bandwidth scope with a high frequency scope probe. The ring frequency can be measured for its value. The impedance Z can be calculated:

$$Z_L = 2\pi fL,$$

where f is the resonant frequency of the ring, and L is the total parasitic inductance in the switch path. If a resistor is selected that is equal to Z, then the ringing should be dampened. The snubber capacitor value is chosen so that

## APPLICATIONS INFORMATION

its impedance is equal to the resistor at the ring frequency. Calculated by:  $ZC = 1/(2\pi fC)$ . These values are a good place to start with. Modification to these components should be made to attenuate the ringing with the least amount of power loss.

### Temperature Monitoring

Measuring the absolute temperature of a diode is possible due to the relationship between current, voltage and temperature described by the classic diode equation:

$$I_D = I_S \cdot e^{\left(\frac{V_D}{\eta \cdot V_T}\right)}$$

or

$$V_D = \eta \cdot V_T \cdot \ln \frac{I_D}{I_S}$$

where  $I_D$  is the diode current,  $V_D$  is the diode voltage,  $\eta$  is the ideality factor (typically close to 1.0) and  $I_S$  (saturation current) is a process dependent parameter.  $V_T$  can be broken out to:

$$V_T = \frac{k \cdot T}{q}$$

where  $T$  is the diode junction temperature in Kelvin,  $q$  is the electron charge and  $k$  is Boltzmann's constant.  $V_T$  is approximately 26mV at room temperature (298K) and scales linearly with Kelvin temperature. It is this linear temperature relationship that makes diodes suitable temperature sensors. The  $I_S$  term in the previous equation is the extrapolated current through a diode junction when the diode has zero volts across the terminals. The  $I_S$  term varies from process to process, varies with temperature,

and by definition must always be less than  $I_D$ . Combining all of the constants into one term:

$$K_D = \frac{\eta \cdot k}{q}$$

where  $K_D = 8.62 \cdot 10^{-5}$ , and knowing  $\ln(I_D/I_S)$  is always positive because  $I_D$  is always greater than  $I_S$ , leaves us with the equation that:

$$V_D = T(\text{KELVIN}) \cdot K_D \cdot \ln \frac{I_D}{I_S}$$

where  $V_D$  appears to increase with temperature. It is common knowledge that a silicon diode biased with a current source has an approximate  $-2\text{mV}/^\circ\text{C}$  temperature relationship (Figure 10), which is at odds with the equation. In fact, the  $I_S$  term increases with temperature, reducing the  $\ln(I_D/I_S)$  absolute value yielding an approximate  $-2\text{mV}/^\circ\text{C}$  composite diode voltage slope.

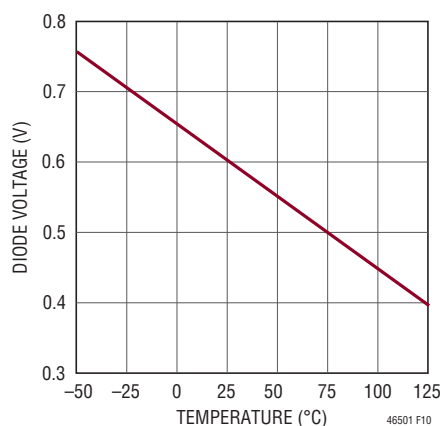


Figure 10. Diode Voltage  $V_D$  vs Temperature  $T(^{\circ}\text{C})$



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To obtain a linear voltage proportional to temperature we cancel the  $I_S$  variable in the natural logarithm term to remove the  $I_S$  dependency from the equation 1. This is accomplished by measuring the diode voltage at two currents  $I_1$ , and  $I_2$ , where  $I_1 = 10 \cdot I_2$  and subtracting we get:

$$\Delta V_D = T(\text{KELVIN}) \cdot K_D \cdot \ln \frac{I_1}{I_S} - T(\text{KELVIN}) \cdot K_D \cdot \ln \frac{I_2}{I_S}$$

Combining like terms, then simplifying the natural log terms yields:

$$\Delta V_D = T(\text{KELVIN}) \cdot K_D \cdot \ln(10)$$

and redefining constant

$$K'_D = K_D \cdot \ln(10) = \frac{198\mu\text{V}}{\text{K}}$$

yields

$$\Delta V_D = K'_D \cdot T(\text{KELVIN})$$

Solving for temperature:

$$T(\text{KELVIN}) = \frac{\Delta V_D}{K'_D} (\text{°CELSIUS}) = T(\text{KELVIN}) - 273.15$$

where

$$300^\circ\text{K} = 27^\circ\text{C}$$

means that is we take the difference in voltage across the diode measured at two currents with a ratio of 10, the resulting voltage is 198 $\mu\text{V}$  per Kelvin of the junction with a zero intercept at 0 Kelvin.

The diode connected PNP transistor at the TEMP pin can be used to monitor the internal temperature of the LTM4650-1. See Figure 25 for an example.

### Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation,

and correlation to hardware evaluation performed on a  $\mu\text{Module}$  package mounted to a hardware test board—also defined by JESD51-9 (“Test Boards for Area Array Surface Mount Package Thermal Measurements”). The motivation for providing these thermal coefficients is found in JESD 51-12 (“Guidelines for Reporting and Using Electronic Package Thermal Information”).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the  $\mu\text{Module}$  regulator’s thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one’s application-usage, and can be adapted to correlate thermal performance to one’s own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

1.  $\theta_{JA}$ , the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as “still air” although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
2.  $\theta_{JCbottom}$ , the thermal resistance from junction to the bottom of the product case, is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical  $\mu\text{Module}$ , the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don’t generally match the user’s application.

## APPLICATIONS INFORMATION

3.  $\theta_{JC\text{TOP}}$ , the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical  $\mu$ Module are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of  $\theta_{JC\text{BOTTOM}}$ , this value may be useful for comparing packages but the test conditions don't generally match the user's application.
4.  $\theta_{JB}$ , the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the  $\mu$ Module and into the board, and is really the sum of the  $\theta_{JC\text{bottom}}$  and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

A graphical representation of the aforementioned thermal resistances is given in Figure 11; blue resistances are contained within the  $\mu$ Module regulator, whereas green resistances are external to the  $\mu$ Module.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal

operating conditions of a  $\mu$ Module. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the  $\mu$ Module—as the standard defines for  $\theta_{JC\text{top}}$  and  $\theta_{JC\text{bottom}}$ , respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the  $\mu$ Module and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model

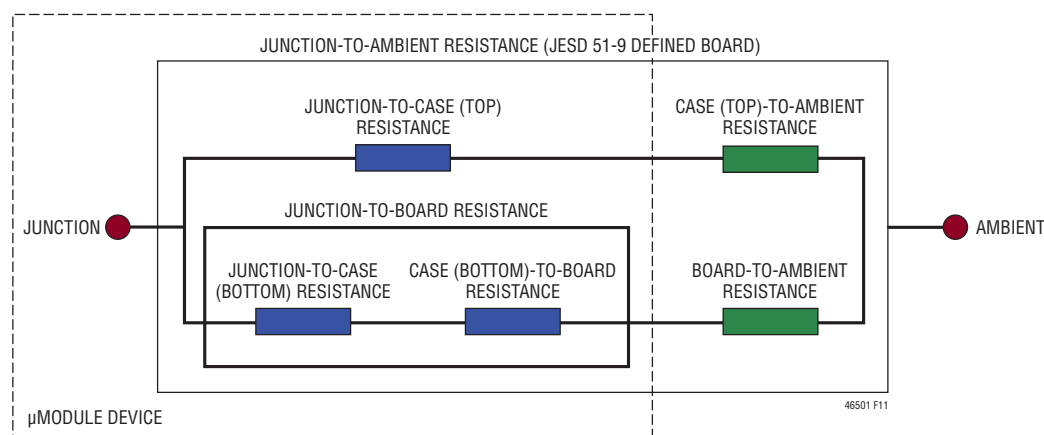


Figure 11. Graphical Representation of JESD51-12 Thermal Coefficients

## APPLICATIONS INFORMATION

and FEA software is used to evaluate the  $\mu$ Module with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due-diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory test have been performed and correlated to the  $\mu$ Module model, then the  $\theta_{JB}$  and  $\theta_{BA}$  are summed together to correlate quite well with the  $\mu$ Module model with no airflow or heat sinking in a properly define chamber. This  $\theta_{JB} + \theta_{BA}$  value is shown in the Pin Configuration section and should accurately equal the  $\theta_{JA}$  value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink. Each system has its own thermal characteristics, therefore thermal analysis must be performed by the user in a particular system.

The LTM4650-1 module has been designed to effectively remove heat from both the top and bottom of the package. The bottom substrate material has very low thermal resistance to the printed circuit board. An external heat sink can be applied to the top of the device for excellent heat sinking with airflow.

Figure 12 shows a temperature plot of the LTM4650-1 with 12V input, 1.0V output at 50A without heat sink and a no airflow condition.

### Safety Considerations

The LTM4650-1 modules do not provide isolation from  $V_{IN}$  to  $V_{OUT}$ . There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support over current protection. A temperature diode is provided for monitoring internal temperature, and can be used to detect the need for thermal shutdown that can be done by controlling the RUN pin.

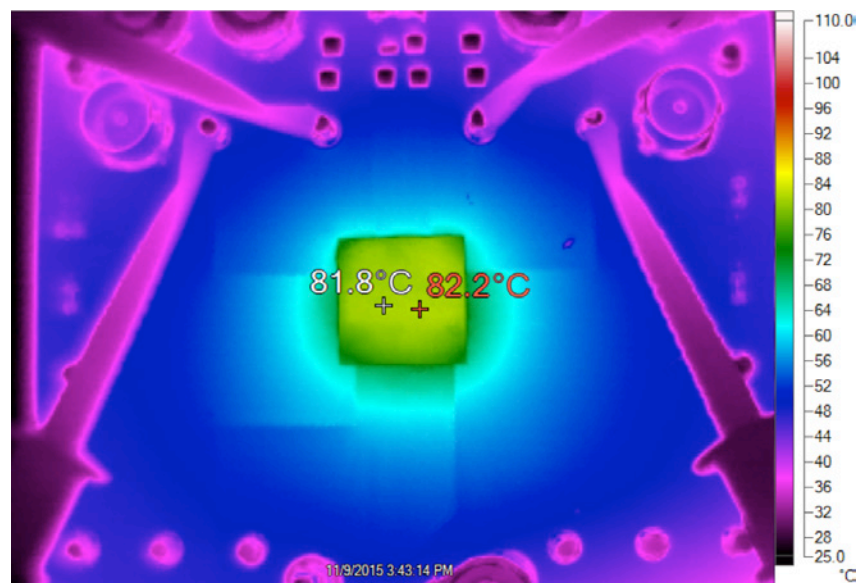


Figure 12. Thermal Image 12V to 1V, 50A with No Air Flow and No Heat Sink (Based on 4-Layer 101mm  $\times$  114mm PCB Board Containing 2oz Copper on the Top, Bottom and All Internal Layers)

## APPLICATIONS INFORMATION

### Power Derating

The 0.9V and 1.5V power loss curves in Figure 14 and Figure 15 can be used in coordination with the load current derating curves in Figure 16 to Figure 23 for calculating an approximate  $\theta_{JA}$  thermal resistance for the LTM4650-1 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with a 1.2 multiplicative factor at 120°C.

The derating curves are plotted with CH1 and CH2 in parallel single output operation starting at 50A of load with low ambient temperature. The output voltages are 0.9V and 1.5V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis.

The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at ~120°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased.

The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 17, the load current is derated to ~35A at ~90°C with 200LFM air but not heat sink and the power loss for the 12V to 0.9V at 35A output is a ~5.6W loss. The 5.6W loss is calculated with the ~4.7W room temperature loss from the 12V to 0.9V power loss curve at 35A, and the 1.20 multiplying factor at 120°C junction temperature. If the 90°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 30°C divided 5.5W equals a 5.4°C/W  $\theta_{JA}$  thermal resistance. Table 2 specifies a 5.5°C/W value which is pretty close. Tables 2 and 3 provide equivalent thermal resistances for 0.9V and 1.5V outputs with and without airflow and heat sinking.

The derived thermal resistances in Tables 2 and 3 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick 4-layer board with 2oz copper on each layer. The PCB dimensions are 101mm × 114mm. The BGA heat sinks are listed in Table 3.

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### Layout Checklist/Example

The high integration of LTM4650-1 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including  $V_{IN}$ , GND,  $V_{OUT1}$  and  $V_{OUT2}$ . It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the  $V_{IN}$ , PGND and  $V_{OUT}$  pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the  $V_{OUT}$ ,  $V_{FB}$ , and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK pin can be tied a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

Figure 13 gives a good example of the recommended layout. LGA and BGA PCB layouts are identical with the exception of circle pads for BGA (see Package Description).

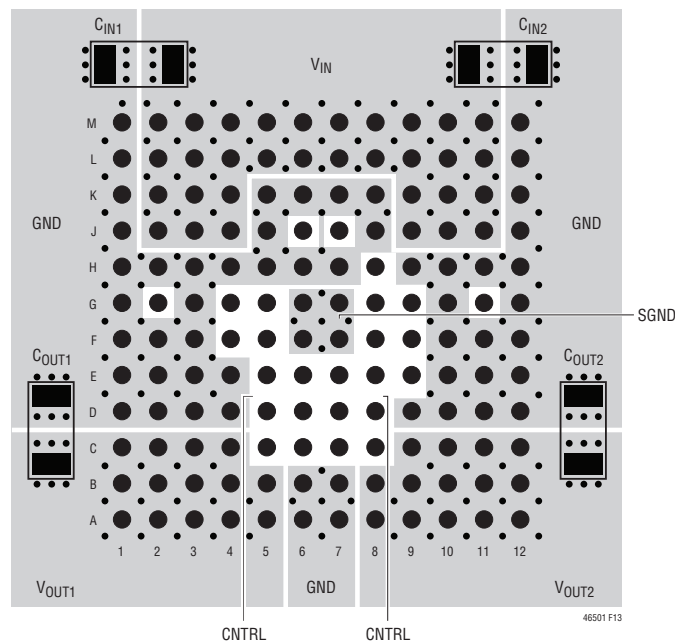


Figure 13. Recommended PCB Layout

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**Table 2. 0.9V Output**

DERATING CURVE	V <sub>IN</sub> (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ <sub>JA</sub> (°C/W)
Figures 16, 17	5, 12	Figure 14	0	None	7.5
Figures 16, 17	5, 12	Figure 14	200	None	5.5
Figures 16, 17	5, 12	Figure 14	400	None	5
Figures 18, 19	5, 12	Figure 14	0	BGA Heat Sink	7
Figures 18, 19	5, 12	Figure 14	200	BGA Heat Sink	4.5
Figures 18, 19	5, 12	Figure 14	400	BGA Heat Sink	4

**Table 3. 1.5V Output**

DERATING CURVE	V <sub>IN</sub> (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ <sub>JA</sub> (°C/W)
Figures 20, 21	5, 12	Figure 15	0	None	7.5
Figures 20, 21	5, 12	Figure 15	200	None	5.5
Figures 20, 21	5, 12	Figure 15	400	None	5
Figures 22, 23	5, 12	Figure 15	0	BGA Heat Sink	7
Figures 22, 23	5, 12	Figure 15	200	BGA Heat Sink	4.5
Figures 22, 23	5, 12	Figure 15	400	BGA Heat Sink	4

**HEAT SINK MANUFACTURER**
**PART NUMBER**
**WEBSITE**

Wakefield

LTN20069-T5

wakefield-vette.com

**Table 4. Output Voltage Response vs Component Matrix (Refer to Figure 23) Load Step Typical Measured Values**
**2-Phase Single Output Solution**

C <sub>IN</sub> (CERAMIC)			C <sub>OUT</sub> (CERAMIC)			C <sub>OUT</sub> (BULK)		
VENDORS	VALUE	PART NUMBER	VENDORS	VALUE	PART NUMBER	VENDORS	VALUE	PART NUMBER
Murata	22μF, 16V, X5R, 1210	GRM32ER61C226KE20L	Murata	100μF, 6.3V, X5R, 1210	GRM32ER60J107ME20L	Panasonic	680μF, 2.5V, 6mΩ	2R5TPF680M6L
Murata	22μF, 16V, X5R, 1206	GRM31CR61C226KE15K	Murata	220μF, 4V, X5R, 1206	GRM31CR60G227M	Panasonic	470μF, 2.5V, 3mΩ	EEFGX0E471R
TDK	22μF, 16V, X5R, 1210	C3225X5R1C226M250AA	Taiyo Yuden	100μF, 6.3V, X5R, 1210	JMK325BJ107MM-T			
			Taiyo Yuden	220μF, 4V, X5R, 1210	AMK325ABJ227MM-T			



## APPLICATIONS INFORMATION

### 25% Load Step (0A to 12.5A) Ceramic Output Capacitor Only Solutions

PEAK-PEAK DEVIATION PERCENTAGE	V <sub>IN</sub>	V <sub>OUT</sub>	C <sub>IN</sub> * (BULK)	C <sub>IN</sub> (CERAMIC)	C <sub>OUT</sub> (BULK)	C <sub>OUT</sub> (CERAMIC)	COMP PIN PARALLEL CAPACITOR (CTHP)	COMP PIN RESISTOR (R <sub>TH</sub> )	COMP PIN CAPACITOR (C <sub>TH</sub> )	FEED-FORWARD CAPACITOR (C <sub>FF</sub> )	PEAK-PEAK DEVIATION (V <sub>PK-PK</sub> )	SETTLING TIME (t <sub>SETTLE</sub> )	CTRL LOOP BANDWIDTH (BW)	CTRL LOOP PHASE MARGIN (PM)	LOAD STEP (A)	LOAD STEP SLEW RATE	R <sub>FB</sub> (kΩ)	FREQ (kHz)
±3% (<60mV)	12V	1V	150μF	22μF x 2	None	220μF x 6	33pF	3.24kΩ	10nF	68pF	53mV	80μs	88kHz	47 Deg	12.5	10A/μs	90.9	500
±3% (<72mV)	12V	1.2V	150μF	22μF x 2	None	220μF x 5	33pF	3.24kΩ	10nF	68pF	56mV	80μs	89kHz	49 Deg	12.5	10A/μs	60.4	500
±3% (<90mV)	12V	1.5V	150μF	22μF x 2	None	220μF x 4	33pF	3.24kΩ	10nF	68pF	58mV	80μs	91kHz	58 Deg	12.5	10A/μs	40.2	600
±3% (<108mV)	12V	1.8V	150μF	22μF x 2	None	220μF x 4	33pF	3.24kΩ	10nF	68pF	64mV	90μs	98kHz	65 Deg	12.5	10A/μs	30.2	600

### 25% Load Step (0A to 9A) Bulk + Ceramic Output Capacitor Solutions

PEAK-PEAK DEVIATION PERCENTAGE	V <sub>IN</sub>	V <sub>OUT</sub>	C <sub>IN</sub> * (BULK)	C <sub>IN</sub> (CERAMIC)	C <sub>OUT</sub> (BULK)	C <sub>OUT</sub> (CERAMIC)	COMP PIN PARALLEL CAPACITOR (CTHP)	COMP PIN RESISTOR (R <sub>TH</sub> )	COMP PIN CAPACITOR (C <sub>TH</sub> )	FEED-FORWARD CAPACITOR (C <sub>FF</sub> )	PEAK-PEAK DEVIATION (V <sub>PK-PK</sub> )	SETTLING TIME (t <sub>SETTLE</sub> )	CTRL LOOP BANDWIDTH (BW)	CTRL LOOP PHASE MARGIN (PM)	LOAD STEP (A)	LOAD STEP SLEW RATE	R <sub>FB</sub> (kΩ)	FREQ (kHz)
±3% (<60mV)	12V	1V	150μF	22μF x 2	470μF x 2	100μF x 4	33pF	3.16kΩ	3300pF	68pF	55mV	30μs	82kHz	68 Deg	12.5	10A/μs	90.9	500
±3% (<72mV)	12V	1.2V	150μF	22μF x 2	470μF x 2	100μF x 4	33pF	3.16kΩ	3300pF	68pF	55mV	30μs	82kHz	73 Deg	12.5	10A/μs	60.4	500
±3% (<90mV)	12V	1.5V	150μF	22μF x 2	470μF x 2	100μF x 4	82pF	4.12kΩ	3300pF	None	64mV	30μs	59kHz	53 Deg	12.5	10A/μs	40.2	600
±3% (<108mV)	12V	1.8V	150μF	22μF x 2	470μF x 2	100μF x 4	82pF	4.12kΩ	3300pF	None	75mV	30μs	51kHz	58 Deg	12.5	10A/μs	30.2	600

### 50% Load Step (0A to 25A) Ceramic Output Capacitor Only Solutions

PEAK-PEAK DEVIATION PERCENTAGE	V <sub>IN</sub>	V <sub>OUT</sub>	C <sub>IN</sub> * (BULK)	C <sub>IN</sub> (CERAMIC)	C <sub>OUT</sub> (BULK)	C <sub>OUT</sub> (CERAMIC)	COMP PIN PARALLEL CAPACITOR (CTHP)	COMP PIN RESISTOR (R <sub>TH</sub> )	COMP PIN CAPACITOR (C <sub>TH</sub> )	FEED-FORWARD CAPACITOR (C <sub>FF</sub> )	PEAK-PEAK DEVIATION (V <sub>PK-PK</sub> )	SETTLING TIME (t <sub>SETTLE</sub> )	CTRL LOOP BANDWIDTH (BW)	CTRL LOOP PHASE MARGIN (PM)	LOAD STEP (A)	LOAD STEP SLEW RATE	R <sub>FB</sub> (kΩ)	FREQ (kHz)
±3% (<60mV)	12V	1V	150μF	22μF x 2	None	220μF x 12	33pF	6.81kΩ	4.7nF	100pF	58mV	80μs	76kHz	45 Deg	25	10A/μs	90.9	500
±3% (<72mV)	12V	1.2V	150μF	22μF x 2	None	220μF x 12	33pF	6.81kΩ	4.7nF	100pF	61mV	80μs	77kHz	50 Deg	25	10A/μs	60.4	500
±3% (<90mV)	12V	1.5V	150μF	22μF x 2	None	220μF x 14	33pF	5.90kΩ	4.7nF	None	90mV	80μs	47kHz	45 Deg	25	10A/μs	40.2	600
±3% (<108mV)	12V	1.8V	150μF	22μF x 2	None	220μF x 14	33pF	5.90kΩ	4.7nF	None	105mV	90μs	43kHz	50 Deg	25	10A/μs	30.2	600

### 50% Load Step (0A to 25A) Bulk + Ceramic Output Capacitor Solutions

PEAK-PEAK DEVIATION PERCENTAGE	V <sub>IN</sub>	V <sub>OUT</sub>	C <sub>IN</sub> * (BULK)	C <sub>IN</sub> (CERAMIC)	C <sub>OUT</sub> (BULK)	C <sub>OUT</sub> (CERAMIC)	COMP PIN PARALLEL CAPACITOR (CTHP)	COMP PIN RESISTOR (R <sub>TH</sub> )	COMP PIN CAPACITOR (C <sub>TH</sub> )	FEED-FORWARD CAPACITOR (C <sub>FF</sub> )	PEAK-PEAK DEVIATION (V <sub>PK-PK</sub> )	SETTLING TIME (t <sub>SETTLE</sub> )	CTRL LOOP BANDWIDTH (BW)	CTRL LOOP PHASE MARGIN (PM)	LOAD STEP (A)	LOAD STEP SLEW RATE	R <sub>FB</sub> (kΩ)	FREQ (kHz)
±3% (<60mV)	12V	1V	150μF	22μF x 2	470μF x 6	100μF x 4	33pF	12.0kΩ	3300pF	47pF	47mV	30μs	70kHz	57 Deg	25	10A/μs	90.9	500
±3% (<72mV)	12V	1.2V	150μF	22μF x 2	470μF x 6	100μF x 4	33pF	12.0kΩ	3300pF	47pF	48mV	30μs	67kHz	65 Deg	25	10A/μs	60.4	500
±3% (<90mV)	12V	1.5V	150μF	22μF x 2	470μF x 6	100μF x 4	68pF	10.2kΩ	3300pF	None	56mV	40μs	50kHz	49 Deg	25	10A/μs	40.2	600
±3% (<108mV)	12V	1.8V	150μF	22μF x 2	470μF x 6	100μF x 4	82pF	14.5kΩ	3300pF	None	58mV	50μs	51kHz	46 Deg	25	10A/μs	30.2	600

\*Bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads.

## APPLICATIONS INFORMATION

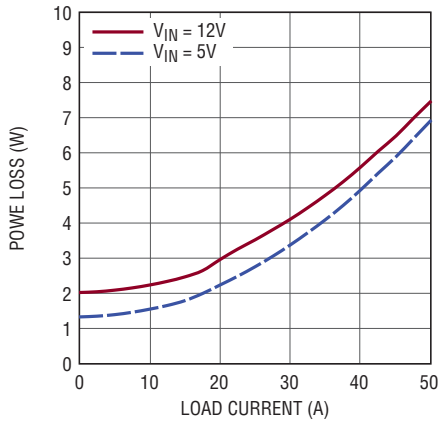


Figure 14. 0.9V Output Power Loss Curve

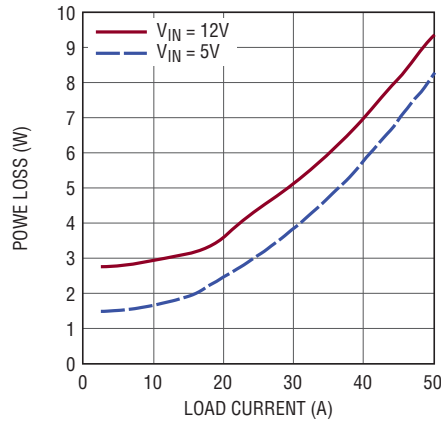


Figure 15. 1.5V Output Power Loss Curve

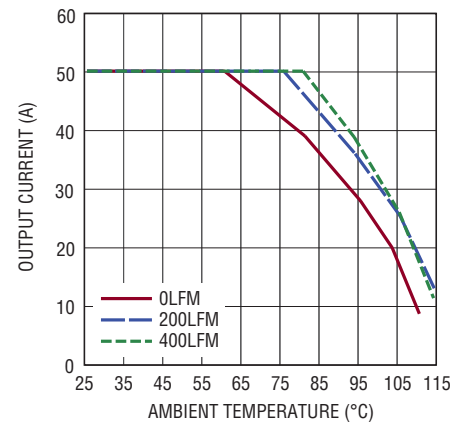


Figure 16. 5V to 0.9V Derating Curve, No Heat Sink

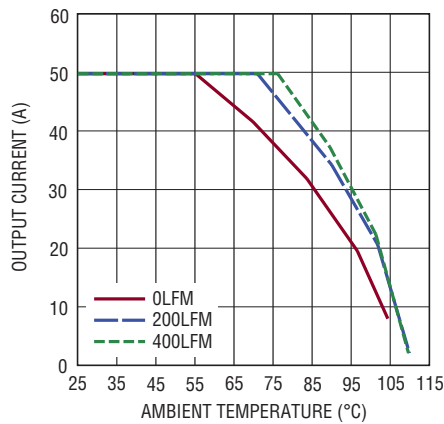


Figure 17. 12V to 0.9V Derating Curve, No Heat Sink

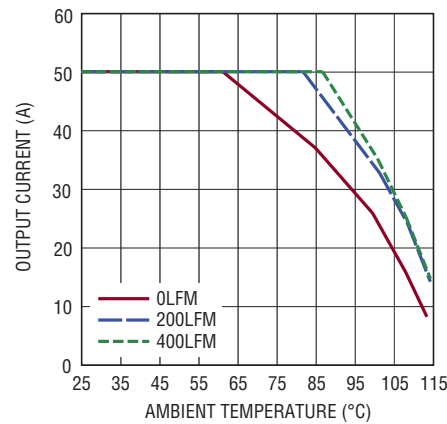


Figure 18. 5V to 0.9V Derating Curve, BGA Heat Sink

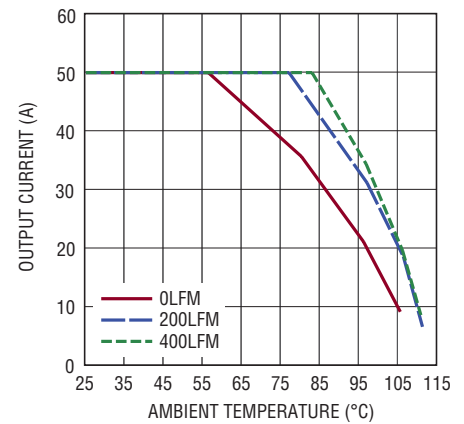


Figure 19. 12V to 0.9V Derating Curve, BGA Heat Sink

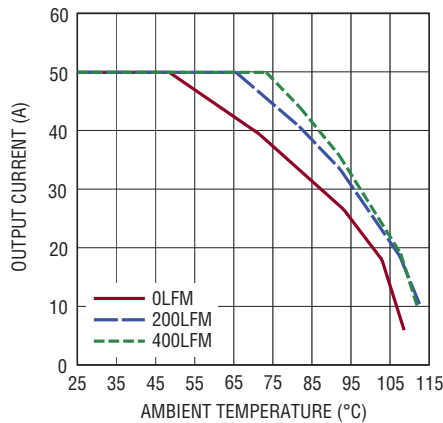


Figure 20. 5V to 1.5V Derating Curve, No Heat Sink

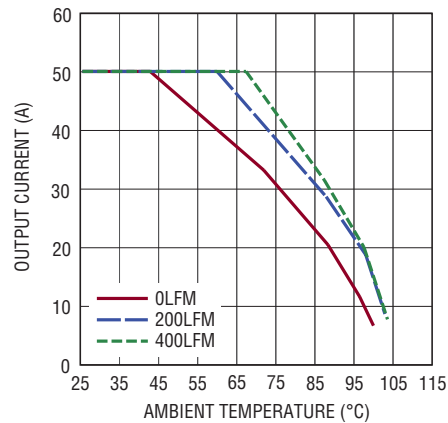


Figure 21. 12V to 1.5V Derating Curve, No Heat Sink

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## APPLICATIONS INFORMATION

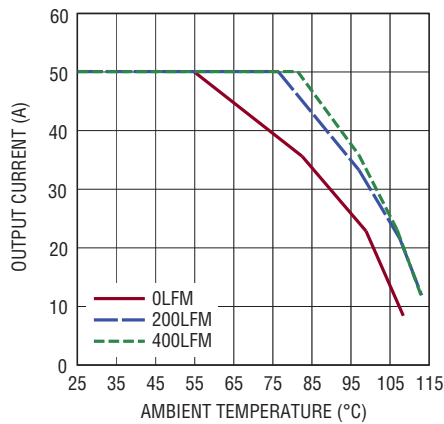


Figure 22. 5V to 1.5V Derating Curve, BGA Heat Sink

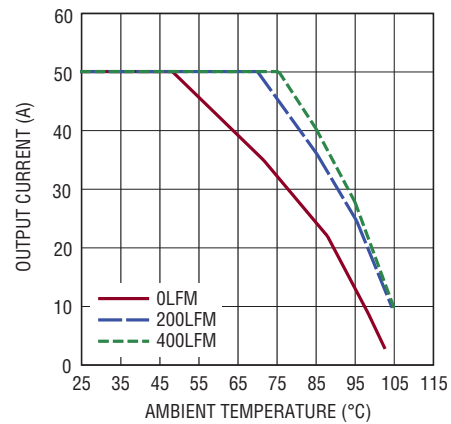


Figure 23. 12V to 1.5V Derating Curve, BGA Heat Sink

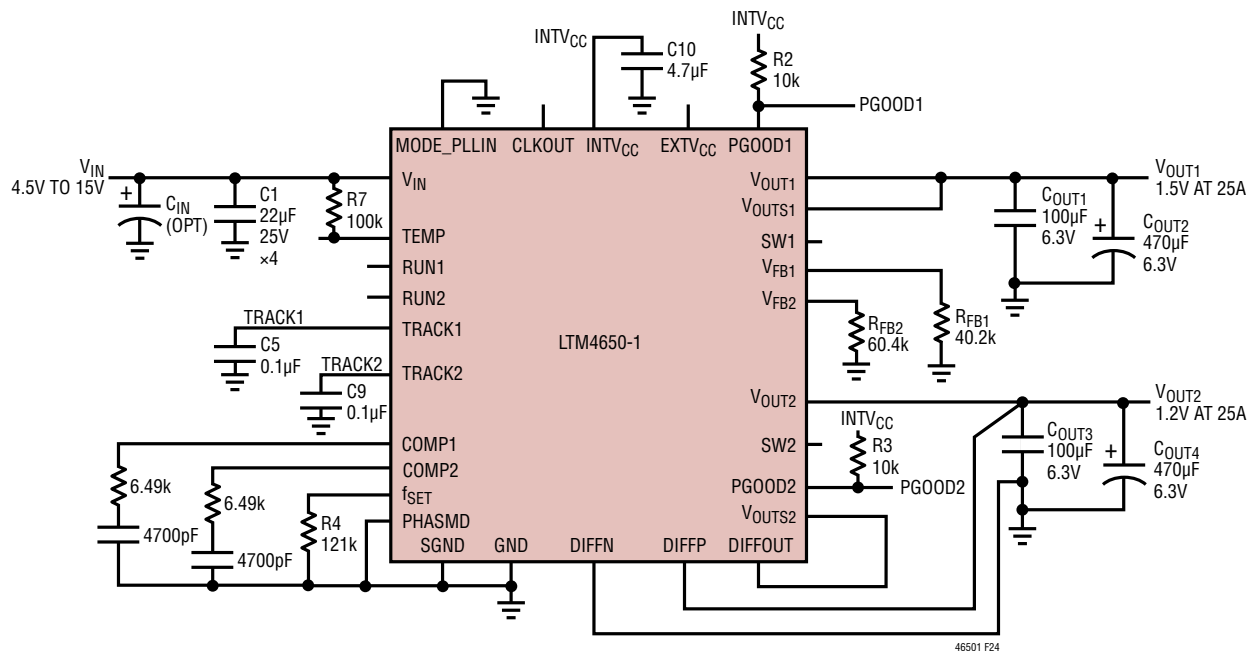
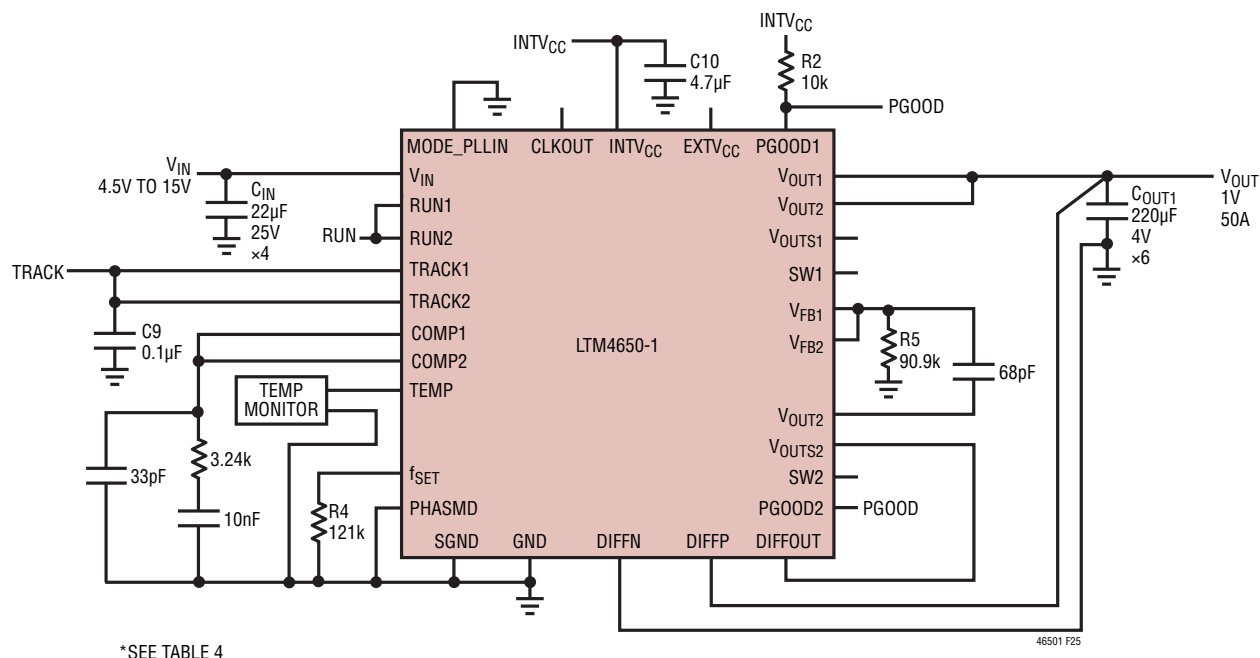
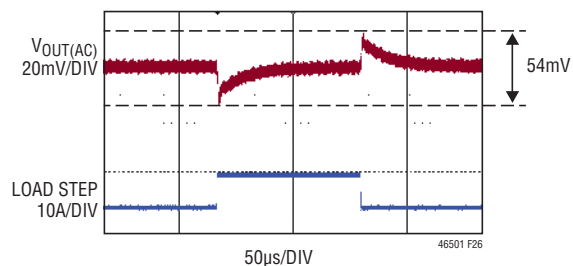


Figure 24. Typical 4.5V<sub>IN</sub> to 15V<sub>IN</sub>, 1.5V and 1.2V at 25A Outputs

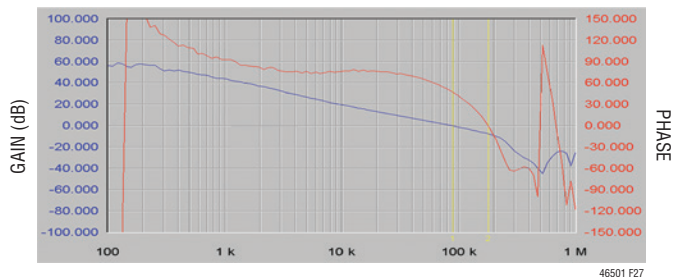
## TYPICAL APPLICATIONS



**Figure 25. LTM4650-1 2-Phase, 1V at 50A Design**



**Figure 26. 25%, 12.5A Load Step Transient Waveform of Figure 23 Circuit**



**Figure 27. Bode Plot of Figure 23 Circuit**

## TYPICAL APPLICATIONS

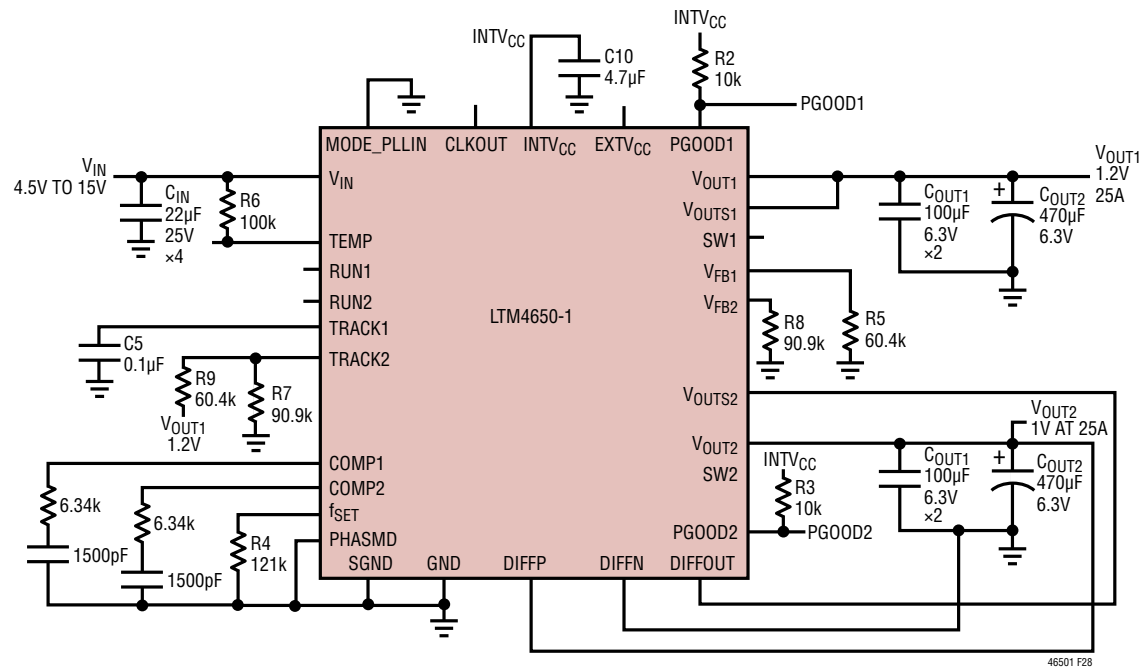


Figure 28. LTM4650-1 1.2V and 1V Output Tracking

## TYPICAL APPLICATIONS

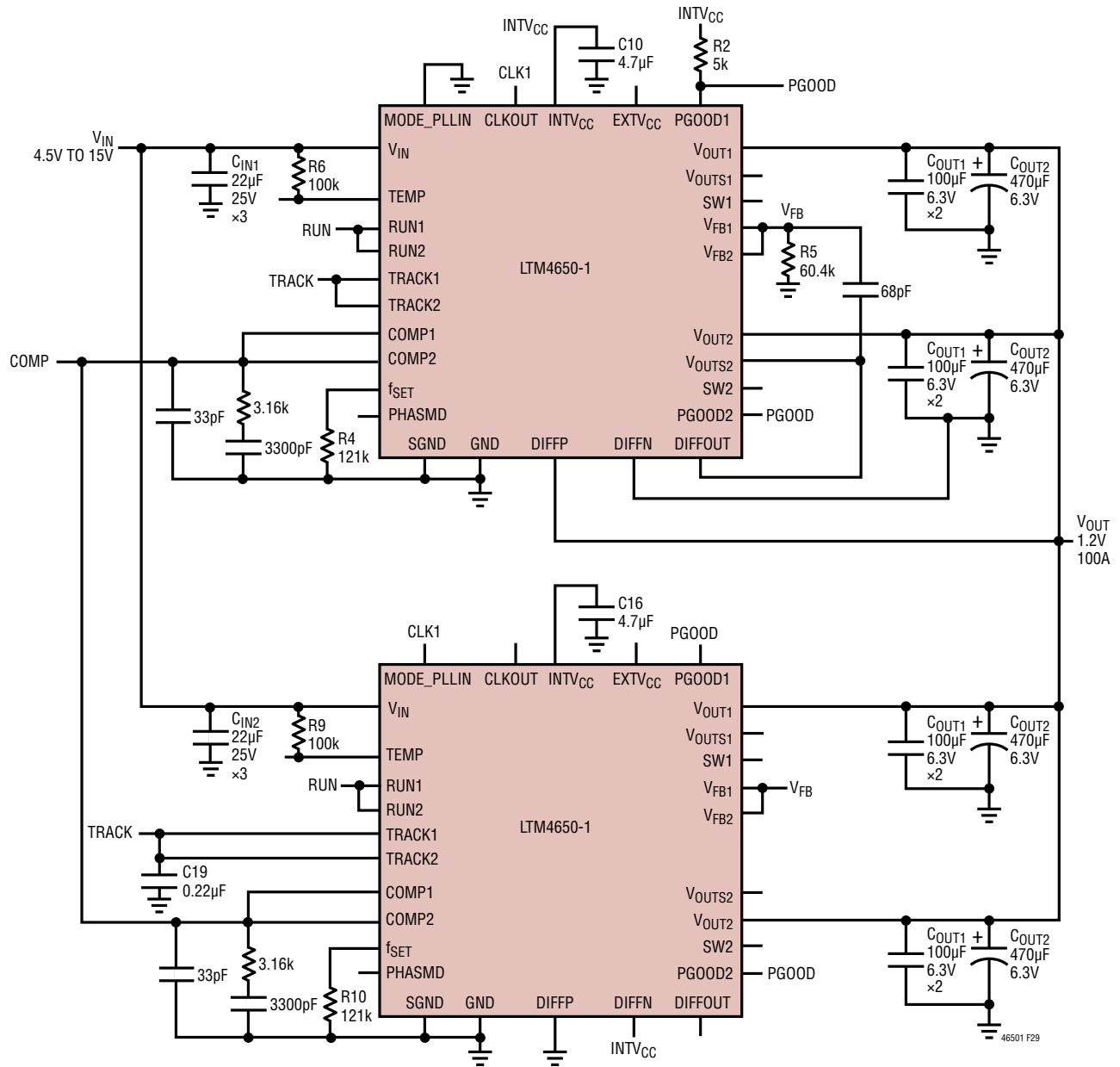


Figure 29. LTM4650-1 4-Phase, 1.2V at 100A



## PACKAGE DESCRIPTION

LTM4650-1 Component BGA Pinout

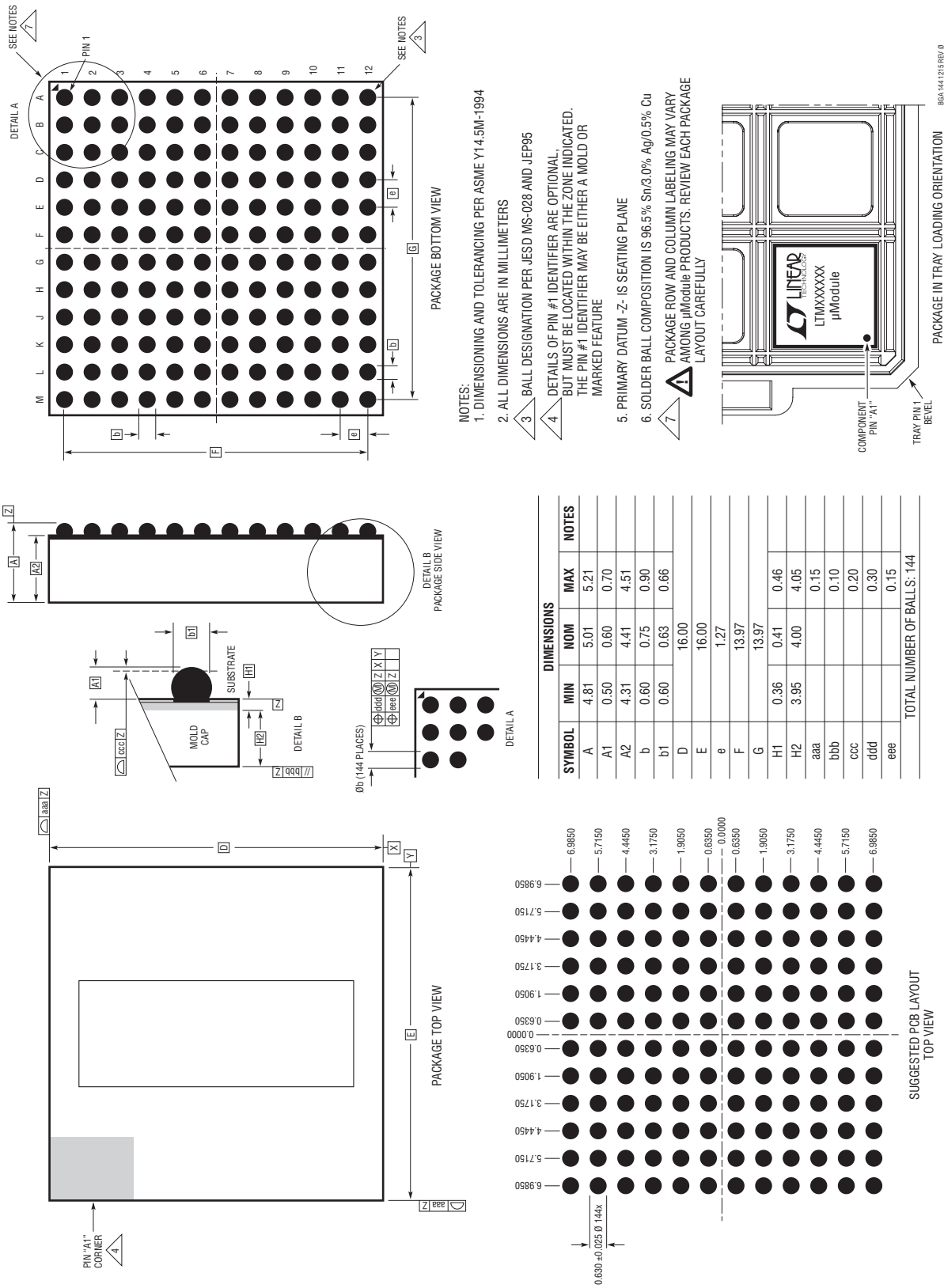
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V <sub>OUT1</sub>	B1	V <sub>OUT1</sub>	C1	V <sub>OUT1</sub>	D1	GND	E1	GND	F1	GND
A2	V <sub>OUT1</sub>	B2	V <sub>OUT1</sub>	C2	V <sub>OUT1</sub>	D2	GND	E2	GND	F2	GND
A3	V <sub>OUT1</sub>	B3	V <sub>OUT1</sub>	C3	V <sub>OUT1</sub>	D3	GND	E3	GND	F3	GND
A4	V <sub>OUT1</sub>	B4	V <sub>OUT1</sub>	C4	V <sub>OUT1</sub>	D4	GND	E4	GND	F4	MODE_PLLIN
A5	V <sub>OUT1</sub>	B5	V <sub>OUT1</sub>	C5	V <sub>OUT1S</sub>	D5	V <sub>FB1</sub>	E5	TRACK1	F5	RUN1
A6	GND	B6	GND	C6	f <sub>SET</sub>	D6	SGND	E6	COMP1	F6	SGND
A7	GND	B7	GND	C7	SGND	D7	V <sub>FB2</sub>	E7	COMP2	F7	SGND
A8	V <sub>OUT2</sub>	B8	V <sub>OUT2</sub>	C8	V <sub>OUT2S</sub>	D8	TRACK2	E8	DIFFP	F8	DIFFOUT
A9	V <sub>OUT2</sub>	B9	V <sub>OUT2</sub>	C9	V <sub>OUT2</sub>	D9	GND	E9	DIFFN	F9	RUN2
A10	V <sub>OUT2</sub>	B10	V <sub>OUT2</sub>	C10	V <sub>OUT2</sub>	D10	GND	E10	GND	F10	GND
A11	V <sub>OUT2</sub>	B11	V <sub>OUT2</sub>	C11	V <sub>OUT2</sub>	D11	GND	E11	GND	F11	GND
A12	V <sub>OUT2</sub>	B12	V <sub>OUT2</sub>	C12	V <sub>OUT2</sub>	D12	GND	E12	GND	F12	GND

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND	H1	GND	J1	GND	K1	GND	L1	GND	M1	GND
G2	SW1	H2	GND	J2	V <sub>IN</sub>	K2	V <sub>IN</sub>	L2	V <sub>IN</sub>	M2	V <sub>IN</sub>
G3	GND	H3	GND	J3	V <sub>IN</sub>	K3	V <sub>IN</sub>	L3	V <sub>IN</sub>	M3	V <sub>IN</sub>
G4	PHASEMD	H4	GND	J4	V <sub>IN</sub>	K4	V <sub>IN</sub>	L4	V <sub>IN</sub>	M4	V <sub>IN</sub>
G5	CLKOUT	H5	GND	J5	GND	K5	GND	L5	V <sub>IN</sub>	M5	V <sub>IN</sub>
G6	SGND	H6	GND	J6	TEMP	K6	GND	L6	V <sub>IN</sub>	M6	V <sub>IN</sub>
G7	SGND	H7	GND	J7	EXTV <sub>CC</sub>	K7	GND	L7	V <sub>IN</sub>	M7	V <sub>IN</sub>
G8	PGOOD2	H8	INTV <sub>CC</sub>	J8	GND	K8	GND	L8	V <sub>IN</sub>	M8	V <sub>IN</sub>
G9	PGOOD1	H9	GND	J9	V <sub>IN</sub>	K9	V <sub>IN</sub>	L9	V <sub>IN</sub>	M9	V <sub>IN</sub>
G10	GND	H10	GND	J10	V <sub>IN</sub>	K10	V <sub>IN</sub>	L10	V <sub>IN</sub>	M10	V <sub>IN</sub>
G11	SW2	H11	GND	J11	V <sub>IN</sub>	K11	V <sub>IN</sub>	L11	V <sub>IN</sub>	M11	V <sub>IN</sub>
G12	GND	H12	GND	J12	GND	K12	GND	L12	GND	M12	GND

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTM4650-1#packaging> for the most recent package drawings.

BGA Package  
144-Lead (16mm × 16mm × 5.01mm)  
(Reference LTC DWG # 05-08-1523 Rev 0)

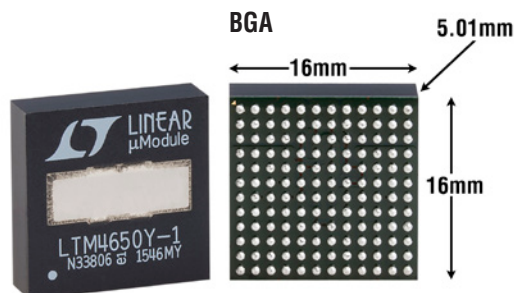


## REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/16	Added SnPb Ball Finish	1, 2
B	07/16	Added LTM4650-1A Connected COMP pin of Master and Slave devices	1, 2, 3, 4, 10 30
C	12/16	Corrected Part Marking and Finished Code	2

# LTM4650-1

## PACKAGE PHOTO



## DESIGN RESOURCES

SUBJECT	DESCRIPTION
<a href="#">μModule Design and Manufacturing Resources</a>	<div>Design:<ul style="list-style-type: none"><li>• Selector Guides</li><li>• Demo Boards and Gerber Files</li><li>• Free Simulation Tools</li></ul></div> <div>Manufacturing:<ul style="list-style-type: none"><li>• Quick Start Guide</li><li>• PCB Design, Assembly and Manufacturing Guidelines</li><li>• Package and Board Level Reliability</li></ul></div>
<a href="#">μModule Regulator Products Search</a>	<div>1. Sort table of products by parameters and download the result as a spread sheet.</div> <div>2. Search using the Quick Power Search parametric table.</div> <div><div>Quick Power Search</div><div><div>Input</div><div><div><math>V_{in}</math> (Min)</div><div><input type="text"/></div><div>V</div></div><div><div><math>V_{in}</math> (Max)</div><div><input type="text"/></div><div>V</div></div></div><div><div>Output</div><div><div><math>V_{out}</math></div><div><input type="text"/></div><div>V</div></div><div><div><math>I_{out}</math></div><div><input type="text"/></div><div>A</div></div></div><div><input type="button" value="Search"/></div></div>

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<a href="#">LTM4650</a>	LTM4650-1 with Internal Compensation	$4.5V \leq V_{IN} \leq 15V$ , Dual 25A or Single 50A
<a href="#">LTM4630</a>	Lower Current than LTM4650; Dual 18A or Single 36A	Pin Compatible with LTM4650; $4.5V \leq V_{IN} \leq 15V$ , $0.6V \leq V_{OUT} \leq 1.8V$ , 15mm × 15mm × 4.41mm LGA and 15mm × 15mm × 5.01mm BGA Packages
<a href="#">LTM4630A</a>	Lower Current and Higher $V_{OUT}$ than LTM4650; Up to 5.3V <sub>OUT</sub> , Dual 18A or Single 26A	Pin Compatible with LTM4650; $4.5V \leq V_{IN} \leq 15V$ , $0.6V \leq V_{OUT} \leq 5.3V$ , 15mm × 15mm × 4.41mm LGA Package
<a href="#">LTM4630-1</a>	Lower Current than LTM4650 with External Compensation and ±0.8% (–1A) or ±1.5% (–1B) $V_{OUT}$ Accuracy	Pin Compatible with LTM4650; $4.5V \leq V_{IN} \leq 15V$ , $0.6V \leq V_{OUT} \leq 1.8V$ , 15mm × 15mm × 5.01mm BGA Package
<a href="#">LTM4620</a>	Lower Current than LTM4650; Dual 13A or Single 26A.	Pin Compatible with LTM4650; $4.5V \leq V_{IN} \leq 16V$ , $0.6V \leq V_{OUT} \leq 2.5V$ , 15mm 15mm × 4.41mm LGA and 15mm × 15mm × 5.01mm BGA Packages
<a href="#">LTM4620A</a>	Lower Current and Higher $V_{OUT}$ than LTM4650; Up to 5.3V <sub>OUT</sub> , Dual 13A or Single 26A.	Pin Compatible with LTM4650; $4.5V \leq V_{IN} \leq 16V$ , $0.6V \leq V_{OUT} \leq 2.5V$ , 15mm 15mm × 4.41mm LGA and 15mm × 15mm × 5.01mm BGA Packages
<a href="#">LTM4628</a>	Lower Current, Higher $V_{IN}$ and $V_{OUT}$ than LTM4650; Dual 8A or Single 16A	Pin Compatible with LTM4650; $4.5V \leq V_{IN} \leq 26.5V$ , $0.6V \leq V_{OUT} \leq 5.5V$ , 15mm 15mm × 4.32mm LGA and 15mm × 15mm × 4.92mm BGA Packages
<a href="#">LTM4677</a>	Dual 18A or Single 36A with PSM	$4.5V \leq V_{IN} \leq 16V$ , $0.5V \leq V_{OUT} \leq 1.8V$ . 16mm × 16mm × 5.01mm BGA Package
<a href="#">LTM4639</a>	Lower $V_{IN}$ ( $2.375V \leq V_{IN} \leq 7V$ ), 20A	$0.6V \leq V_{OUT} \leq 5.5V$ . 15mm × 15mm × 4.92mm BGA Package

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